[Technical Paper]

Thermal Transient Test Based Thermal Structure Function Analysis of IGBT Package

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Abstract

In this article an IGBT package is measured using thermal transient test method following JESD 51-14 standard. In order to study the thermal structure in the package, a detailed CFD (Computational Fluid Dynamics) simulation model is also created and calibrated against the physical device using structure function. By the calibrated CFD model the package's thermal behavior is studied. The purpose of this paper is to illustrate the process of calibrating CFD model to get a "thermally identical" representation of physical devices.

Keywords: Thermal Analysis, Power IGBT, Measurement and Instrumentation, Thermal Transient Test, Structure Function, Thermal CFD Simulation, Thermal Model Calibration

Background

For decades IGBT device has being asked for higher power density and higher reliability to meet serious application requirements. Power cycling is known to be one of the most serious reasons of device delamination because die temperature swings the largest scale up to $\Delta T_j > 150$ degC. This temperature swing causes Large heat expansion and results in the physical delamination which impacts the reliability. Die-attach, the closest adhesive layer to the IGBT die, must be designed and manufactured to survive the temperature rise and fall. The challenges to the die-attach material and manufacture process is big and request effective and accurate methodology which is able to investigate the thermal structure in a physical device.

Using structure functions[1] to do measurement based thermal analysis for electrical components has been proven accurate and effective. In former paper[2] isothermal surface way to understand structure function has been discussed and proven available by experiment.[4] In this article, we also adopt structure function method and use model calibration technique[3, 4] for thermal structural analysis on a commercial device sample.

Experiment

SOT-227 package IGBT component is chosen as experimental sample. As shown in Fig. 1 the device capability is rated to 100 A @ T_c = 25 degC and designed for high speed switching application.

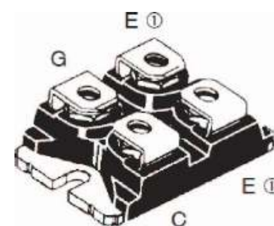

Fig. 1 Outline of SOT-227 package IGBT.

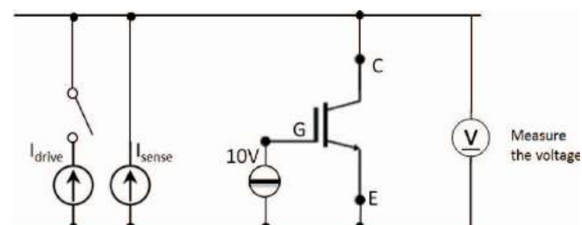

Fig. 2 Test circuit for the measurement.

Test circuit is shown in Fig. 2. Constant voltage is applied to IGBT's gate terminal to keep the device open to allow current flow through during the measurement. Two separate current sources provide heating current and sensing current respectively. High speed switch turns on/off the high-current source in several micro seconds and a

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dedicated high-speed high-accuracy measurement channel is used to record the temperature change during cooling phase. The test sequence is illustrated in Fig. 3. The measurement follows the static test method standardized in JEDEC JESD 51-1 and JESD 51-14. Test conditions are shown in Table 1.

TSP measurement

TSP (Temperature sensitive parameter) is also measured following JESD 51-1. 1 A sensing current is adopted to suppress electrical noise providing highly repeatable measurement result. Temperature sensitivity result is shown in Fig. 4, we can see high linearity in its sensitivity of 1.024 mV/degC in normal temperature range.

Thermal transient measurement

The measured temperature response and thermal transient resistance Zth curve is shown in Fig. 5 and Fig. 6. The electric transient noise at the beginning 0 ~ 50 us is compensated using "square-root" correction method standardized in JESD 51-14.

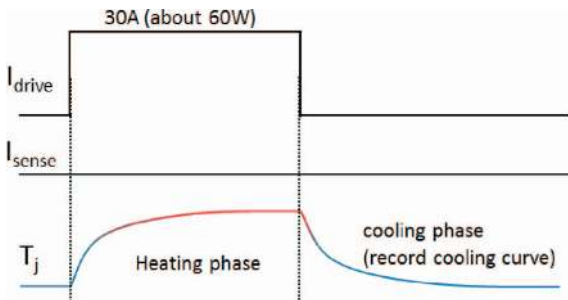


Fig. 3 Thermal transient test sequence.

Table 1 Measurement conditions.

Heating current	30	A
Heating power	58.5	W
Sensing current	1	A
Gate Voltage	10	V
Heating time	30	Second
Cooling time	30	Second

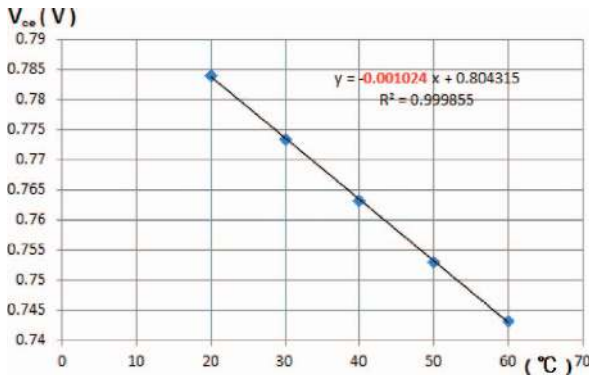


Fig. 4 IGBT sensitivity calibration result @ 1 A.

Thermal Analysis

For structural analysis purpose the sample was investigated in CT (Computed Tomography) scanner and then sliced at the center of IGBT die to obtain accurate die size and thickness of all composing layers. See Fig. 7.

There is another die of a diode on the other side next to IGBT die as can be seen in CT picture in Fig. 7. Obviously this diode does not affect IGBT's thermal structure so that it will not be discussed in this article.

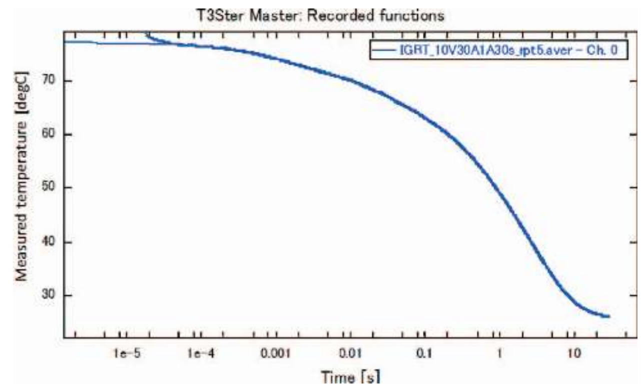


Fig. 5 Raw measurement data.

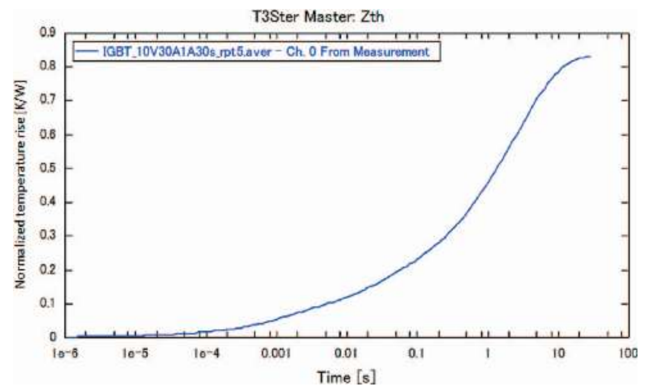


Fig. 6 Zth curve.

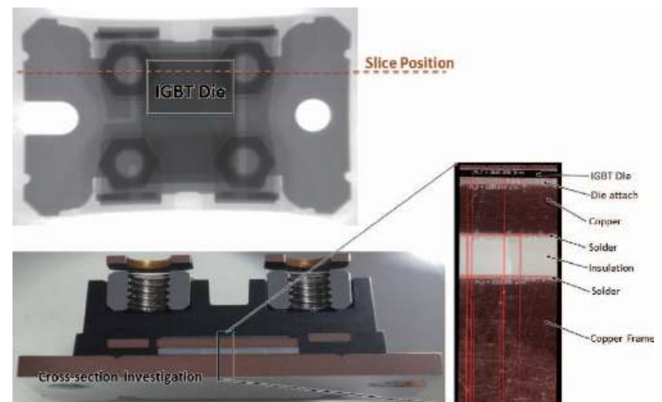


Fig. 7 CT and cross-section investigation picture.

Table 2 Dimension of all composing layers in the package.

IGBT Die size	7.0 × 11.5	mm
IGBT Die	140	μm
Die attach	100	μm
Copper	900	μm
Solder	50	μm
Insulation	650	μm
Copper Frame	2,050	μm

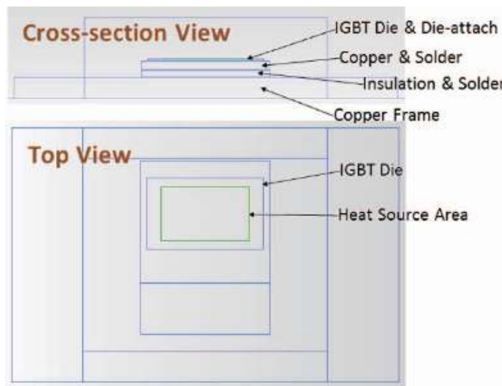


Fig. 8 Cross-section and Top view of CFD model.

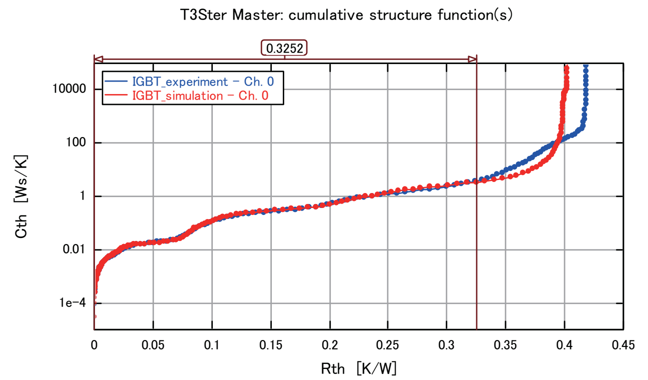


Fig. 9 Experiment and simulation structure function.

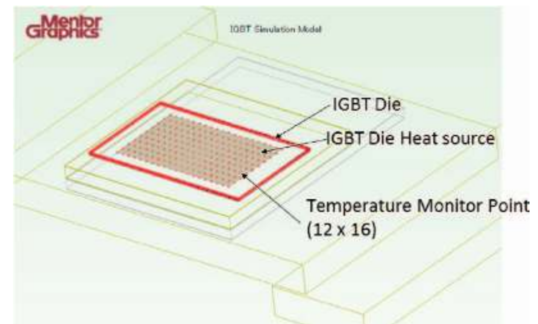


Fig. 10 Heat source area and its temperature monitor points.

According to the dimensional information in Table 2, a detailed CFD model is built for this IGBT package. See Fig. 8.

The next step is to calibrate detailed thermal CFD model against transient measurement result based on structure function. There is delicate discussion about model calibration methodology in other papers.[2, 3]

In the experiment environment, IGBT sample is mounted to a large cold-plate using 3.4 W/mK thermal grease as thermal interface material and constant pressure is also applied. The cold plate is liquid cooled driven by a circulator to fix its plate temperature at 25 degC (same as room temperature). In the simulation environment, IGBT model is also attached to a similar cold plate with fixed plate temperature of 25 degC and ambient air temperature is also set to the same 25 degC.

The final calibrated structure functions of simulation model and the experiment result are shown in Fig. 9. We can observe good match before 0.32 K/W which is supposed to be inside IGBT package. After 0.32 K/W two structure functions differs because boundary condition in simulation is ideal while not in reality. Anyway, the difference in cold plate after 0.32 K/W is not what we are interested in, so it can be ignored here in this article.

To make simulation model match experimental structure function, heat source area is reduced by about 25% from die area.

Figure 10 shows heat source area locating in the center of die of dimension of 5.25 mm × 8.63 mm × 30 μm.

In the measurement, die temperature is monitored by sampling V_{ce} voltage from external pin of the package, therefore the value is actually weighted average temperature on the whole heating area. So far there is no test method to capture accurate junction temperature distribution inside the die, so we need to “simulate” the measured die temperature to make simulation results match experimental results. The way of using “averaged” temperature for model calibration is necessary and was also discussed in former paper.[4]

The approach adopted in this article is to put 12 × 16 monitor points in an array uniformly in heat source area then average all 196 points after transient simulation. This averaging method does not necessarily behave in exactly the same way as physical phenomenon, but it does reproduce the same thermal transient response which is just what we want.

Heat source area discussion

During the model calibration process, we found size of heat source area has great impact upon thermal structure inside device package.

Figure 11 shows the structure functions of three differ-

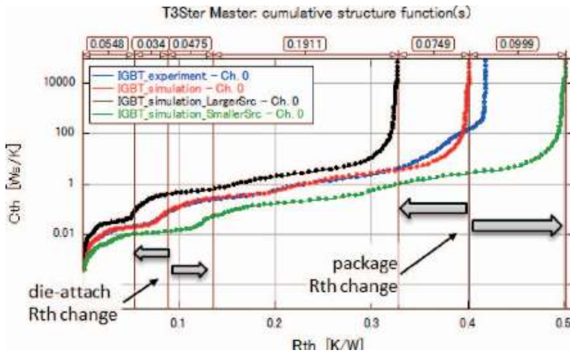


Fig. 11 Structure function if heat source is of the same size as die.

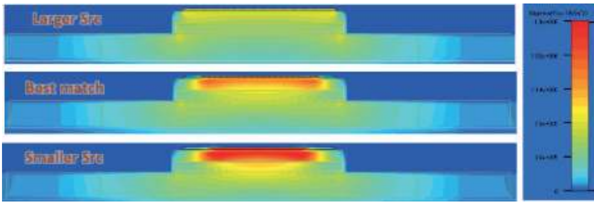
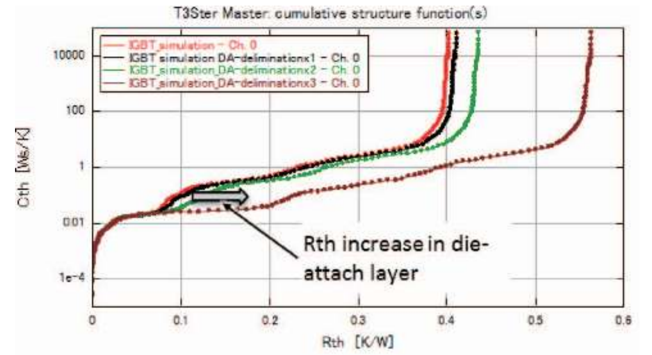


Fig. 12 Heat flux distribution of "LargerSrc," "Best Match" and "SmallerSrc" simulation model.



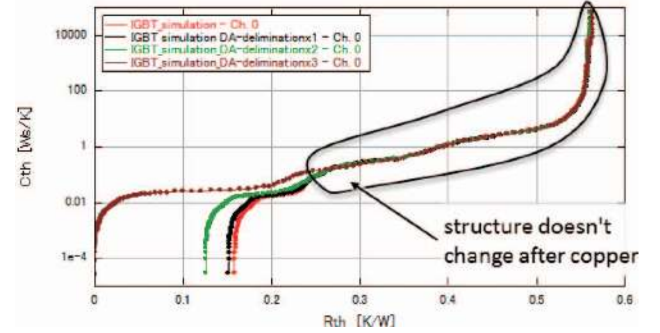


Fig. 13 Structure functions of die-attach delamination model.

ent heat source sizes.

"LargerSrc": 7.0 mm × 11.5 mm = 80.5 mm^2

"BestMatch": 5.3 mm × 8.6 mm = 45.6 mm^2

"SmallerSrc": 4.2 mm × 6.9 mm = 29.0 mm^2

Die size: 7.0 mm × 11.5 mm = 80.5 mm^2

We can easily find both R_{th} (Thermal resistance) and C_{th} (Thermal capacitance) of die-region in structure function changes in proportion to active heat source area. This can be again confirmed in heat flux view as shown in Fig. 12. The larger the heat source area the wider heat flux spreads then results in more active C_{th}. On the opposite, smaller heat source area produces higher heat flux in a smaller region and results in larger R_{th}.

In Fig. 12 we can also see heat source area has impact on die-attached region and further on copper layer and insulation layer. Heat flux concentrates significantly in all there layers in the package as heat source area becomes smaller, this makes it harder to remove heat from die and results in larger R_{th} which can be observed again in structure function in Fig. 11.

Die-attach delamination discussion

Die-attach delamination is often caused by power cycling and increases thermal resistance of this layer finally destroy the component. In the calibrated simulation, we can easily increase die-attach thermal resistance without destroy a real sample. This is the advantage to use calibrated thermal model to study a physical phenomenon.

We tried to add contact thermal resistance between die-attach and copper layer by 5e-7 Km^2/W, 2e-6 Km^2/W and 1e-5 Km^2/W. The structure functions are shown in Fig. 13.

We can see after die region in structure function, die-attach thermal resistance increases as the contact thermal resistance increases. From structure function we can read the increase in R_{th} is 0.0076 K/W, 0.0332 K/W, 0.1597 K/W respectively, which is just in proportion to the contact thermal resistance added. Further, we can also see less significant impact on the copper layer's while no effect in after copper layer.

Conclusion

In this article, we demonstrated how to do transient thermal test on an IGBT device and how to build calibrated thermal CFD model basing on measurement result.

To do accurate structural analysis correct dimensions of the sample are important. For multi- layer structure package like IGBT, X-ray scanning is not enough, it can be used to identify the position and size of target die but destructive investigation is also necessary to obtain accurate thickness information of all layers. Once the CFD simulation model is calibrated successfully, we can use this model to study any thermal characteristics of the device package.

As discussed, heat source area has great impact on the whole thermal structure of the package, while die-attach delamination affects adjacent neighbor layers much more significant than others.

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