Thermal Transport in Silicon Nanowires at High Temperature up to 700 K

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Thermal transport in silicon nanowires[1] has captured the attention of theoretical scientists for understanding phonon transport at the nanoscale, and the thermoelectric figure-of-merit (*ZT*) reported in rough nanowires[2,3] has inspired engineers to develop cost-effective waste heat recovery systems. Thermoelectric power generators composed of silicon target high-temperature applications due to improved efficiency beyond 550 K[4]. However, there have been no studies of thermal transport in silicon nanowires beyond room temperature[1–3]. Moreover, high-temperature thermal transport measurements enable studies of unanswered questions regarding the impact of surface boundaries and varying mode contributions as the highest vibrational modes are activated (Debye temperature of silicon is 645 K). Here we develop a technique to investigate thermal transport in nanowires up to 700 K. Our thermal conductivity measurements on smooth silicon nanowires show a diameter dependence from 40 nm to 120 nm in accordance with classical predictions[5], and rough nanowires show a significant reduction throughout the temperature range, demonstrating a potential for efficient power generation (e.g. *ZT* = 1 at 700 K).

Thermoelectric power generators create electrical energy from waste heat. This environmentally friendly solid-state energy conversion technology has attracted broad attention for many years[6], but the material efficiency has been a bottleneck for practical applications. The thermoelectric figure-of-merit used to benchmark material efficiency is expressed as $ZT = S^2\sigma T/(k_e+k_p)$, where S is the Seebeck coefficient, σ is the electrical conductivity, T is the temperature in degrees Kelvin, k_e is the thermal conductivity by electrons, and k_p is the thermal conductivity by phonons. While increasing ZT has proven challenging due to cross-coupled material properties, one established strategy is to employ nanostructuring to impede phonon transport while minimally disturbing electron transport. Among various thermoelectric materials, silicon nanostructures have shown great promise for combining the attributes of energy efficiency and cost effectiveness. Silicon (Si) is an earth-abundant inorganic material that has long established manufacturing infrastructures due to the microelectronics industry. While the excellent electrical properties of Si have paved ways for revolutionary electronic applications, the high thermal conductivity has limited its consideration for thermoelectric devices. The perception had held until recently when Si nanostructures showed significant thermal conductivity reduction without altering the electronic properties[2,3,7] and low thermal conductivity values even below the classical limit[5,8].

Past studies on thermal transport in Si nanostructures have explored various geometries including thin films[9], smooth nanowires[1,10], rough nanowires[2,3,11], nanotubes[12], nanomesh[13], and holey structures in the in-plane[7] and the cross-plane[14] directions. Li *et al.*[1] first demonstrated the size dependent thermal conductivity in Si nanowires (Si NWs) by utilizing Vapor-Liquid-Solid (VLS) synthesis technique, which produced high-purity and smooth-surface nanowires with the diameter in the range of 22 nm and 115 nm. The thermal conductivity of VLS Si NWs was measured in the temperature range of 20 K to 320 K, and the values at 300 K were ranging between 7 $Wm^{-1}K^{-1}$ and 40 $Wm^{-1}K^{-1}$, which are about an order of magnitude smaller than the known values of bulk silicon (145 $Wm^{-1}K^{-1}$)[15]. Many theoretical studies followed the VLS Si NWs data[1], modeling the size dependence in various numerical methods including the Boltzmann Transport Equation (BTE) calculations[8,16–19], Monte Carlo (MC) simulations[20,21], and Molecular Dynamics (MD) simulations[22,23]. Despite the large attention by

theoretical scientists, the experimental work of thermal transport in VLS Si NWs has been limited to only a few reports[1,10]. Experimental researchers engaged in observing unique thermal transport in rough Si NWs have utilized various etching techniques such as electroless-etching (EE)[2] and metal-assisted etching[11,24]. The surface roughness has been observed to have a dramatic impact on thermal transport; the thermal conductivity of a 50 nm EE rough Si NW is as low as 1.6 $Wm^{-1}K^{-1}$ at room temperature[2], which is close to the theoretical limit of amorphous Si (1 $Wm^{-1}K^{-1}$)[25]. Promisingly, the large thermal conductivity reduction did not detract from the electrical transport properties because of the large difference in average mean free paths between phonons and electrons in silicon. Furthermore, synthetic Si nanostructures with proper doping conditions[2,3,7] have demonstrated bulk-like electrical conductivity and Seebeck coefficient, which are great assets for thermoelectric applications.

Thermoelectric power generators may harvest waste heat from automobile exhausts and large-scale power plants where the surface temperature can be often higher than 500 K. As high-temperature operations are desirable for heat engines governed by Carnot efficiency, many thermoelectric materials including Si show increasing energy conversion efficiency at high temperatures[26]. LeBlanc *et al.*[4] reported cost consideration results indicating that thermoelectric material costs may become reasonable (< $1/W) for typical thermoelectric power generation applications at mean temperatures above 550 K. However, the thermoelectric properties of Si NWs above room temperature have not been accessible due to experimental challenges such as temperature variations caused by radiation heat loss, and unstable sample materials and device constituents at high temperature. Thermal transport research in other nanomaterials has also been limited to near room temperature, with few exceptions to 500 K (e.g., BiTe nanowires[27] and carbon nanotubes[28]). In addition, due to the lack of experimental data, there remain fundamental questions regarding phonon transport at high temperature. Some known characteristics of high-temperature phonons include strong Umklapp scattering, increased contributions of high-frequency modes and optical phonons, and a possibility of multi-phonon process. Their interplay with surface boundaries in Si nanowires is unknown. Moreover, the effect of roughness of Si NWs on phonon transport at high temperature still remains elusive. Here we develop a technique to

investgiate high-temperature thermal transport in nanomaterials including one-dimensional and two-dimensional structures and present thermal conductivity characterization of smooth VLS Si NWs and rough Si NWs in the temperature range from 20 K up to 700 K. We custom-designed a sample stage with improved thermal contacts and a radiation shield. Using transmission electron microscopy and spectroscopy, we verify the material integrity over this temperature range, particularly through the length of nanowires and near thermal contacts. We studied VLS Si NWs whose diamter varies from 40 nm to 130 nm, and the diameter dependence that agrees with computational results based on Boltzmann Transport Equation (BTE) in the relaxation time approximation. We also used BTE to access the unique features of high-temperature phonons including the optical mode contribution. We measured temperature-dependent thermal conductivity in rough NWs prepared by two versions of established synthesis techniques, which allow investigation of surface roughness effects with respect to vertical and lateral roughness length scales using each version of rough NWs. The measurement of thermal conductivity at high temperature can not only extend the available knowledge in phonon transport of nanomaterials to temperature regime that has been inaccessible, but can also provide new insight into unresolved phenomena from the past research that only explored up to room temperature. The metrology that we develop can also open up opportunities to study electrical and thermal transport at high-temperature in other nanomaterials including one- and two-dimensional structures. New findings may make significant advances in high-temperature relevant energy conversion systems such as thermoelectric power generators.

To enable thermal conductivity measurement of individual nanowires up to 700 K, we developed a high temperature system including a custom-designed sample mount stage (Fig. 1a and b). The thermally optimized design overcomes experimental challenges of temperature variations and heat losses at high temperature. In particular, radiation heat losses becomes substantial with increasing temperature, as Stefan–Boltzmann law dictates that heat loss is proportional to (T^4_{sample}-T^4_{sur}), where T_{sample} is the sample temperature and T_{sur} is the surrounding temperature. To minimize radiative heat loss, we implemented a radiation shield made of Copper that has low emissivity ~0.07[29]. The optimized thermal design can reach a higher temperature with a smaller time constant compared to a conventional stage that is commercially available (Fig. 1c and Supplementary

Information (SI)). The key differences in the optimized design are improved thermal contacts and radiation shielding. The finite element method (FEM) simulations also show that the incorporation of a radiation shield effectively reduces radiation heat losses (Fig. 1d and e). Furthermore, the settling time of sample temperature within a deviation of 1 K from the steady-state temperature is ~70 mins for the optimized stage, which is in contrast to the settling time of ~170 mins for the conventional stage (Fig. S1d in SI). The improvement of settling time provides great stability of sample temperature during the measurement at each temperature, and also significantly reduces the measurement time and the sample exposure to high temperatures. To improve the sample temperature measurement, a platinum resistive temperature detector (RTD) is positioned on the same chip carrier and in proximity to the sample. The local temperature detector accurately monitors the sample temperature change during the thermal transport measurements.

Thermal conductivity measurement is based on a well-established single NW thermometry technique[30], in which microfabricated structures are suspended from a substrate to force heat flux across a nanowire. Two symmetric island structures are each equipped with Pt electrodes, which can act as a thermometer and a heater, and supported by thin and long SiN_x beams. Individual silicon nanowires are transferred in-between the two islands by a manipulator such that the nanowire bridges the two islands (SI). The nanowire is then mechanically and thermally anchored on the Pt electrode by electron beam induced deposition (EBID) of Pt inside the SEM chamber. Subsequently, under a high vacuum ($<10^{-6}$ torr) one island is heated and the bridged nanowire transports heat by conduction to the other island. During this process, the temperature of each membrane is monitored simultaneously. The temperature difference between the two islands is used to extract the thermal conductivity of individual nanowires. Knowing the temperature of each membrane and the amount of heat dissipation, the thermal conductance of single nanowires can be quantified. Then, the length and diameter of NWs are measured using Scanning Electron Microscope (SEM) and thermal conductivity is calculated using the obtained dimensions.

We measured thermal conductivity of VLS Si NWs ranging from 20 K up to 700 K with taking thermal contact resistances into account. Careful characterization of thermal contact resistance is essential to quantify thermal conductivity of VLS Si NWs and details are provided in SI. In order to examine diameter-dependent phonon transport, thermal conductivity of VLS Si NWs whose diameter varying from 40 nm to 120 nm at room temperature is shown in Fig. 2a. Compared to bulk silicon (145 $Wm^{-1}K^{-1}$) at room temperature [15], the thermal conductivity of VLS Si NWs with diameter 120 nm, 70 nm, and 40 nm at room temperature is 36 $Wm^{-1}K^{-1}$, 28 $Wm^{-1}K^{-1}$, and 22 $Wm^{-1}K^{-1}$ respectively. Reduced characteristic length, diameter in this case, shortens the mean free path due to boundary scattering and hence impedes phonon transport, as observed in previous studies[1,19]. Diameter-dependent VLS Si NW thermal conductivity values at room temperature calculated based on two BTE models (see Method and SI) are in good agreement with measured diameter-dependent thermal conductivity values. While the gray model (see Method and SI) is consistent with BTE models for Si VLS NWs with a diameter less than 100 nm, it overestimates thermal conductivity values for VLS Si NWs with a diameter larger than 100 nm. These results suggest that gray model could be used under limited conditions. In addition, temperature-dependent thermal conductivity of VLS Si NWs is shown in Fig. 2b. The agreement between experiment and BTE model with full phonon dispersion up to 700K suggests that the classical model with boundary scattering mechanism and full phonon dispersion captures the phonon transport well for the nanowires whose diameter is from 40 nm to 120 nm. Thermal conductivity increases as temperature is elevated and decreases after reaching certain temperature in crystalline solids. Phonon transport is dominated by boundary and interface scattering at low temperature[31]. Umklapp processes, *i.e.* phonon-phonon scattering, become dominant at high temperature, resulting in decreasing thermal conductivity trend at high temperature. The temperature dependent thermal conductivity of VLS Si nanowires with diameter 40-120 nm exhibits a similar trend with an almost identical temperature of ~175 K where the thermal conductivity maximum is. The temperature of Bulk Si where thermal conductivity is maximum is ~ 20K[35]. Comparison of temperature dependent thermal conductivity between bulk Si and VLS Si NWs also suggests that boundary scattering is dominant mechanism in reduction of thermal conductivity, since temperature where thermal conductivity maximum is shifted toward higher temperature. As

the diameter of the VLS Si NWs is reduced, thermal conductivity in all temperature range decreases due to more effective boundary scattering.

During experiments, Si NWs undergo electron beam exposure at 1kV in SEM, potential Pt deposition on NWs in EBID process, and large temperature excursions (20 K – 700 K). To verify the integrity of Si NWs, we obtained transmission electron microscope (TEM) images of the VLS Si NWs after experiment is conducted (Fig. 2c and d). VLS Si NW shown was exposed to more than four hours of the EBID Pt bonding process while most other nanowires experienced about two hours of the EBID Pt bonding process in average. Fig. 2c shows some bright contrast at the surface of the NW near the Pt contact end and homogeneous contrast near the center of the NW. The bright contrast implies a preferential deposition of heavy elements (i.e. Pt) near the contact due to the EBID process. HRTEM image shown in Fig. 2d in the same area further supports this observation by showing the strong presence of Pt nanoparticles (NPs) at the surface of the Si NW near the contact and much-less-to-negligible presence of Pt NPs away from the contact. In order to further prove the crystallinity of Si NWs, core-loss electron energy-loss spectroscopy (EELS) was performed, which provides chemical fingerprints of the elements and their oxidation states. Fig. 2e shows the results of EELS line profile as indicated in Fig. 2c. Specifically, beginning from the contact end towards the center, 10 successive Si-L core-loss EELS spectra were acquired. For all 10 spectra, the energy onsets (~100eV) as well as the energy-loss near edge structures (ELNES), agree well with the bulk Si spectrum[32–34]. Observing no energy shift in the Si-L edge suggests that the Pt NPs are physically absorbed on the surface of the Si NW and no Pt-Si alloy is formed

High temperature phonon physics had received much attention in 1960s and 1970s based on bulk silicon measurement results for developing phonon transport models in crystalline solids[35,36]. While room-temperature thermal conductivity is commonly explained by three-phonon process, some predicted multiple phonon processes as well as optical phonons may become important at high temperatures[35]. Josh *et al*.[36] investigated a four-phonon process model for thermal transport and showed that a quartic term occurring in the crystal potential function due to the increased atomic vibrations which, at higher temperatures, may become appreciable. We can infer from the temperature dependence of the relaxation time (τ^{-1}~T^2) in the four-phonon

model that the thermal conductivity at very high temperatures may lead to $k \sim T^{-2}$ due to high-order processes. In carbon nanotubes, Pop *et al*.[37] showed a temperature-dependent thermal conductivity deviating from $k \sim T^{-1}$ starting from 500 K, and the deviation was attributed to a higher-order phonon process. For bulk silicon, the multiple phonon process for thermal transport may become important at temperatures greater than 700 K[36]. Our measured data in VLS Si NWs show $k \sim T^{-1}$ however, which indicates a common expected form of three phonon process is still valid in VLS Si NWs up to 700 K. The optical phonons are often neglected in modeling Si thermal conductivity because of their small group velocity, as indicated in the phonon band structure (Fig. 3a). However, the contribution of optical phonons for thermal transport is expected to become more important as temperature increases, because dominant phonon frequency increases. Therefore, we chose BTE model with full phonon dispersion, which includes optical phonon branches, to investigate high temperature phonon physics in VLS Si NWs. Fig. 3b shows that for Si 80 % of heat conduction is carried by phonons with frequency 1 THz or less at 20 K, while 80 % of heat conduction is carried by phonons with frequency 4 THz or less at 700 K. This result clearly demonstrates that dominant phonon frequency increases with increasing temperature. Fig. 3a shows that the optical phonons have a frequency range of 12-16 THz, which is higher than acoustic phonons that are known to be responsible for majority of heat conduction. As the size becomes smaller, the acoustic phonons scatter strongly with boundaries, and the relative contribution of optical phonons to thermal transport increases. Thus, the nanowires have relatively important heat conduction contributions from optical phonons at high temperatures. Fig. 3d demonstrates that optical phonon contribution of VLS Si NW with a diameter of 10 nm can be as large as ~23 %, while that of VLS Si NW with a diameter of 500 nm is ~10 % at elevated temperature. In addition, even for the bulk Si the contribution of optical phonons at 700 K is estimated to be 5 %. Fig. 3c describes the contribution of each branch to VLS Si NW thermal conductivity. We compare our experimental results of 70 nm diameter VLS Si NW with BTE models. As clearly seen, the contribution of optical branches becomes appreciable at high temperature. This result suggests that the contribution of optical phonons for VLS Si NWs needs to be taken into account for better understanding of thermal transport at high

temperature. Identical BTE model parameters are used for thermal conductivity of bulk Si and other VLS Si NWs and results are in excellent agreements (SI).

Next, we investigated thermal transport in two versions of rough Si NWs: electroless etched Si nanowires (EE NWs) and roughned Vapor-Liquid-Solid Si nanowires (RVLS NWs). Fig. 4a and b show the measured thermal conductivity of rough NWs from 20 K to 700 K, which is substantially lower than that of VLS Si NWs for the entire temperature range. The observed thermal conductivity reduction in rough NWs is attributed to surface roughness effects, as intensively investigated in experimental[2,11,24] and theoretical[5,16,24,38] studies in the past. The inset of Fig. 4a shows TEM images and root mean square (rms) values of the three EE wires (2.6, 1.7, and 0.7 nm), which match well with the inversely related trend of the thermal conductivity. The demonstrated effect of rms values in EE wires agrees with theoretical models[38], in which higher rms roughness value leads to lower thermal conductivity due to increased phonon boundary scattering. The correlation length of these EE wires was challenging to extract and analyze due to extensive statistical requirements along the nanowire length. Instead, the impact of correlation length effect on thermal transport was clearly demonstrated using RVLS NWs, in which the roughness along the entire length of nanowires (2-5 μm) was fully captured[11]. While the rms values of the three RVLS NWs were similar at 3.3 ± 0.5 nm, the correlation lengths were considerably different: 13.1 nm, 6.4 nm, and 5.3 nm, as shown in Fig. 4b. The diameters of rough nanowires have small variations in each type (120 nm for EE_1, 100 nm for EE_2, 103 nm for EE_3, 78 nm for RVLS_1, 70 nm for RVLS_2, and 62 nm for RVLS_3), and we assume the impact of these diameter variations is smaller than that of the roughness parameters, in accordance with observations of earlier studies[2,11]. Based on the experimental results, we can infer that the correlation length, which captures a lateral length scale of surface roughness, is a significant factor for thermal transport. In a coherent phonon transport picture, the correlation length that is close to the phonon wavelength may result in increased interference with phonon waves and lead to multiple scattering at surface boundaries[39,40]. The coherent scattering description may also explain the consistent effect of the correlation length at high temperature because changes in the dominant wavelength of phonons are not significant from 300 K to 700 K according to the first principles study[22]. These results verify that the thermal conductivity

reduction mechanisms by surface roughness effects, which were first observed in earlier our studies with limited temperature ranges[2,11], are effective up to 700 K. The persistent trend of thermal conductivity reduction at high temperatures is a promising sign for thermoelectric applications targeting low- to mid-grade waste heat sources.

The best thermoelectric figure of merit (ZT) reported for silicon is 0.6[2], which is comparable to commercial thermoelectric materials and some complex semiconductors[41]. While recent laboratory findings in novel materials are encouraging, most of them are not practical for large-scale implementation because they are composed of rare, toxic, or expensive elements. *ZT* of Si is expected to increase at high temperature up to 700 K, unlike other thermoelectric materials such as BiTe. We estimated thermoelectric efficiency of rough Si NWs based on the experimental thermal conductivity results and theoretically obtained Seebeck coefficient and electrical conductivity[26]. The Seebeck coefficient and electrical conductivity are optimal values from a heavily doped n-type silicon and calculated considering non-parabolicity and a temperature-dependent band structure[26]. The *ZT* of EE NW increases up to 1 at 700 K, and the maximum energy conversion efficiency reaches 13 % (assuming the cold side temperature remains at 300 K, see SI). This estimation strongly suggests that rough Si NWs can be an efficient thermoelectric material particularly at high temperatures.

We developed the experimental platform that enabled thermal conductivity characterization of Si NWs at high temperature up to 700 K. The TEM and elemental analysis verify that Si NWs do not form platinum-silicide alloys even after high temperature excursions. Thermal contact resistance obtained from measured length-dependent thermal resistance allows accurate measurements of thermal conductivity in Si NWs. Measured thermal conductivity of VLS Si nanowires are in good agreement with BTE model with full phonon dispersion relation. Our BTE model with experimental results suggests that the contribution of optical phonons to thermal conductivity of VLS Si NWs should not be neglected at elevated temperature up to 700 K. We also show that roughness factors, rms roughness as vertical length scales and correlation length as lateral length scales, play an important role in the reduction of thermal conductivity in EE and RVLS NWs. The estimation based on the measured thermal conductivity of rough Si nanowires with theoretically estimated thermoelectric properties predicts ZT value of 1 at 700 K, which adds a credential to developing cost-effective thermoelectric devices using

Si nanostructures. The metrology we developed may open up opportunities to study nanoscale transport phenomena at a broad range of temperature, which could be relevant for novel energy conversion applications.

Methods

Nanowire Synthesis: High purity single-crystalline silicon nanowires (NWs) are synthesized based on the VLS method[5] while using gold nanoparticles (NPs) as a catalyst. The VLS nanowires have uniform diameter with the standard deviation of 3 % across the entire length. The high aspect ratio, smooth surface areas, and well-distributed diameters are desirable for studying the size dependence. Gold colloids are known to produce well-dispersed and diameter-controlled Si NWs[42]. However, the Au-catalyzed silicon NWs synthesized by the VLS method may suffer from tapering from one end to another end because of high diffusion rate of Au catalysts under growth conditions.[43] Here, we synthesized high-quality Si NWs with the length greater than 10 um and with the diameter as thin as 40 nm by using Au colloids as the seed and $SiCl_4$ as the vapor-phase reactant. The substrate was p-type Si in the <111> orientation with the resistivity of 1.7~2.8 Ohm-cm. After cleaning sequentially in acetone and isopropanol, the substrate was etched in 10:1 buffered hydrofluoric acid for about 10s to remove the oxide. The substrate was placed 1-2 cm downstream from the furnace center in a quartz tube. We used pure H_2 gas instead of H_2/Ar (volume ratio 1:10) mixture gas in order to improve the growth rate and resultant synthesized nanowires have a uniform diameter along the growth direction.

Rough Nanowire Synthesis: Rough Si NWs are synthesized using two independent methods: EE nanowires[2] and roughened VLS (RVLS) nanowires[11,44], as demonstrated in the past. The EE nanowires are synthesized by employing galvanic displacement of silver onto silicon wafers. Clean boron doped <100> silicon wafers were immersed in mixture of aqueous 0.02M $AgNO_3$ and 5M HF solution. Ag+ ion reduces onto a silicon surface by injection holes into silicon valence band. The silver deposit acts as a cathode on which more Ag+ reduce and form silver dendrite by oxidizing surrounding silicon, which is subsequently removed by HF. As silver dendrite etch down the wafer, vertical single crystalline nanowire arrays form. After the synthesis, the silver dendrite is

washed off by DI water and the Si NW arrays are immersed in the concentrated nitric acid solution to remove residual silver nanoparticles. After soaking into IPA, nanowire arrays were released by critical point dryer to minimize adhesion among surrounding nanowires. The vertically aligned nanowire arrays are oriented the same as wafer direction. The surface texture can be affected by the doping concentration of the starting wafer, and lower resistivity increases the surface roughness[45,46].

The RVLS nanowires are synthesized from the VLS nanowires by subsequently roughening at a controllable manner. Before introducing the roughness to as-grown VLS Si nanowires, the gold catalyst on the tip was removed in KI/I_2 solution and then the native oxide was etched in vapor HF. Then nanowires were roughened by either of the two processes, which produces distinctly unique surface roughness features and enables us to study a variety of surface roughness effect. In the first process, immediately after removing native oxide, NW suspension was prepared by sonicating NW array chip in DI water. Then this suspension was added to a mixture of $AgNO_3$ (1.74×10^{-3}M) and HF (3.53M) to introduce roughness. The galvanic displacement between silver ions and silicon take place, similar to the EE wire growth. After 2 minutes, excessive DI was added to quench the reaction, and the solution was centrifuged to collect NWs. The NW pellets were redispersed in the concentrated nitric acid to remove residual silver particles. Rough NWs were isolated again after repeating centrifuge and rinsing process. In the second process, immediately after removing native oxide, NW chip was immersed in the premixed etchant solution (mixture of 10mL HF (3.53M)/H_2O_2 (5.57M) with 100µL $AgNO_3$ (1.74×10^{-3}M) added). After rinsing in DI water, residual silver particles were removed in nitric acid. The surface roughness is primarily affected by the doping concentration of wafers. Higher doping levels lead to rougher or more porous surfaces[11]. Higher concentration of impurities or defects may play as nucleation sites for pore formation. Increased dopant concentration lowers the barrier for hole injection and increases the current flow, creating rougher surfaces. The low resistivity wafers that are reported to be porous are not studied here.

TEM and Elemental Analysis: HRTEM, high-angle annular dark field scanning transmission electron microscopy (HAADF-STEM) and electron energy-loss spectroscopy (EELS) were performed using the 200 kV Tecnai F20 UT.

The point resolution of HRTEM was 0.19 nm. For the STEM-EELS, the energy resolution was about 0.5 eV and the energy dispersion was 0.05 eV per channel. The camera length was 42 mm, and the entrance aperture of the GIF system was 2.5 mm in diameter. The convergence and collection angles were 21 mrad and 47 mrad, respectively.

BTE Modeling: To better understand the temperature- and diameter-dependence of the VLS Si NW thermal conductivity, we invoke a Boltzmann Transport Equation (BTE) within the relaxation time approximation[16],

$$\boldsymbol{k} = \frac{\mathbf{1}}{\mathbf{3}} \sum_{\boldsymbol{n}} \int \boldsymbol{C}(\boldsymbol{\omega}) \boldsymbol{v}_{\boldsymbol{g}}(\boldsymbol{\omega}) \boldsymbol{\tau}(\boldsymbol{\omega})\, \boldsymbol{d\omega},$$

where n is the phonon mode polarization, C is the volumetric phonon heat capacity, v_g is the phonon group velocity, and τ is the phonon relaxation time. The phonon relaxation time can be expressed via Matthiessen's rule as $\tau = (\tau_b + \tau_i + \tau_u)^{-1}$, where τ_b is boundary scattering, τ_i is impurity scattering, and τ_u is umkapp scattering. We have employed two BTE models, one with full phonon dispersion relation[21] and the other with sinusoidal phonon dispersion relation, so called Born von Karman (BvKS) model. [8,19] to compare sophisticated models with all six independent branches and a relatively simple standardized single branch approximation. In the first approach, we use quadratic fits, which track known acoustic and optical phonon dispersion branches of bulk silicon obtained from neutron scattering experiments[47]. Modeling silicon nanostructures using bulk silicon dispersions is known to provide an accurate description of phonon states in silicon as thin as 5 nm[16]. We consider the phonon dispersion in silicon along the (100) direction and assume each phonon dispersion branch is isotropic. Then the group velocity at each wave vector is used to calculate thermal conductivity of VLS Si nanowires. In the second approach (BvKS model), the three acoustic branches are approximated to a single effective branch and the phonon transport due to optical branches is assumed to be neglegible. In the BvKS model, we used parameters provided by Yang *et al.*[8]. We also used a gray body approximation, as a quick analysis tool, to capture the size dependent thermal conductivity of VLS Si NWs. The gray model is expressed as $k_{gray} = k_{bulk}(D/(D+\lambda))$, where k_{bulk} is the thermal conductivity of bulk Si, D is the diameter of VLS Si NW, and λ is the average mean free path of bulk Si (=300 nm in Fig. 2a).

References

1. Li, D. *et al.* Thermal conductivity of individual silicon nanowires. *Appl. Phys. Lett.* **83,** 2934–2936 (2003).

2. Hochbaum, A. I. *et al.* Enhanced thermoelectric performance of rough silicon nanowires. *Nature* **451,** 163–167 (2008).

3. Boukai, A. I. *et al.* Silicon nanowires as efficient thermoelectric materials. *Nature* **451,** 168–171 (2008).

4. Leblanc, S., Yee, S. K., Scullin, M. L., Dames, C. & Goodson, K. E. Material and manufacturing cost considerations for thermoelectrics. *Renew. Sustain. Energy Rev.* **32,** 313–327 (2014).

5. Mingo, N., Yang, L., Li, D. & Majumdar, A. Predicting the Thermal Conductivity of Si and Ge Nanowires. *Nano Lett.* **3,** 1713–1716 (2003).

6. Hicks, L. D. & Dresselhaus, M. S. Effect of Quantum-Well Structures on the Thermoelectric Figure of Merit. *Phys. Rev. B* **47,** 12727–12731 (1993).

7. Tang, J. *et al.* Holey silicon as an efficient thermoelectric material. *Nano Lett.* **10,** 4279–4283 (2010).

8. Yang, F. & Dames, C. Mean free path spectra as a tool to understand thermal conductivity in bulk and nanostructures. *Phys. Rev. B - Condens. Matter Mater. Phys.* **87,** 1–12 (2013).

9. Asheghi, M., Leung, Y. K., Wong, S. S. & Goodson, K. E. Phonon-boundary scattering in thin silicon layers. *Appl. Phys. Lett.* **71,** 1798–1800 (1997).

10. Chen, R. *et al.* Thermal Conductance of Thin Silicon Nanowires. *Phys. Rev. Lett.* **101,** 1–4 (2008).

11. Lim, J., Hippalgaonkar, K., Andrews, S. C. & Majumdar, A. Quantifying Surface Roughness E ff ects on Phonon Transport in Silicon Nanowires. *Nano Lett.* **12,** 2475–2482 (2012).

12. Wingert, M. C. *et al.* Sub-Amorphous Thermal Conductivity in Ultra-Thin Crystalline Silicon Nanotubes. *Nano Lett.* 150310203815000 (2015). doi:10.1021/acs.nanolett.5b00167

13. Yu, J.-K., Mitrovic, S., Tham, D., Varghese, J. & Heath, J. R. Reduction of thermal conductivity in phononic nanomesh structures. *Nat. Nanotechnol.* **5,** 718–721 (2010).

14. Lee, J., Lim, J. & Yang, P. Ballistic Phonon Transport in Holey Silicon. *Nano Lett.* 150410123418004 (2015).

doi:10.1021/acs.nanolett.5b00495

15. Ho, C. Y., Powell, R. W. & Liley, P. E. Thermal Conductivity of the Elements. *J. Phys. Chem. Ref. Data* **1,** 279–421 (1972).

16. Mingo, N. Calculation of nanowire thermal conductivity using complete phonon dispersion relations. 4 (2003). doi:10.1103/PhysRevB.68.113308

17. McGaughey, A. J. H., Landry, E. S., Sellan, D. P. & Amon, C. H. Size-dependent model for thin film and nanowire thermal conductivity. *Appl. Phys. Lett.* **99,** 3–5 (2011).

18. Yang, R., Chen, G. & Dresselhaus, M. S. Thermal conductivity of simple and tubular nanowire composites in the longitudinal direction. *Phys. Rev. B - Condens. Matter Mater. Phys.* **72,** 1–7 (2005).

19. Dames, C. & Chen, G. Theoretical phonon thermal conductivity of Si/Ge superlattice nanowires. *J. Appl. Phys.* **95,** 682–693 (2004).

20. Chen, Y., Li, D., Lukes, J. R. & Majumdar, A. Monte Carlo Simulation of Silicon Nanowire Thermal Conductivity. *J. Heat Transfer* **127,** 1129 (2005).

21. Pop, E., Dutton, R. W. & Goodson, K. E. Analytic band Monte Carlo model for electron transport in Si including acoustic and optical phonon dispersion. *J. Appl. Phys.* **96,** 4998–5005 (2004).

22. Henry, A. S. & Chen, G. Spectral Phonon Transport Properties of Silicon Based on Molecular Dynamics Simulations and Lattice Dynamics. *J. Comput. Theor. Nanosci.* **5,** 1–12 (2008).

23. He, Y. & Galli, G. Microscopic origin of the reduced thermal conductivity of silicon nanowires. *Phys. Rev. Lett.* **108,** 1–5 (2012).

24. Ghossoub, M. G. *et al.* Spectral phonon scattering from sub-10 nm surface roughness wavelengths in metal-assisted chemically etched Si nanowires. *Nano Lett.* **13,** 1564–1571 (2013).

25. Cahill, D. G., Watson, S. K. & Pohl, R. O. Lower limit to the thermal conductivity of disordered crystals. *Phys. Rev. B* **46,** 6131–6140 (1992).

26. Chen, G. *et al.* Increased Phonon Scattering by Nanograins and Point Defects in Nanostructured Silicon with a Low Concentration of Germanium. *Phys. Rev. Lett.* **102,** 2–5 (2009).

27. Hsin, C.-L. *et al.* Phase transformation and thermoelectric properties of bismuth-telluride nanowires. *Nanoscale* **5,** 4669–72 (2013).

28. Pettes, M. T. & Shi, L. Thermal and structural characterizations of individual single-, double-, and multi-walled carbon nanotubes. *Adv. Funct. Mater.* **19,** 3918–3925 (2009).

29. Incropera, F. & Dewitt, D. Introduction to heat transfer. *John Wiley Sons Inc* **19,** 704 (1985).

30. Shi, L. *et al.* Measuring Thermal and Thermoelectric Properties of One-Dimensional Nanostructures Using a Microfabricated Device. *J. Heat Transfer* **125,** 881 (2003).

31. Bellis, L. De, Phelan, P. E. & Prasher, R. S. Variations of Acoustic and Diffuse Mismatch Models in Predicting Thermal-Boundary Resistance. *J. Thermophys. Heat Transf.* **14,** 144–150 (2000).

32. Ercius, P. & Muller, D. Si Bulk. (2003). at <http://muller.research.engineering.cornell.edu/sites/WEELS/View/Si_bulk.html.>

33. Ahn, C. C. & Krivanek, O. L. Eels atlas. *Gatan* (1983).

34. Botton, G. & L'Espérance, G. Effect of accelerating voltage and thickness on an effective signal-to-noise ratio in electron energy loss spectroscopy. *Ultramicroscopy* **41,** 287–290 (1992).

35. Holland, M. Analysis of Lattice Thermal Conductivity. *Phys. Rev.* **132,** 2461–2471 (1963).

36. Joshi, Y. P., Tiwari, M. D. & Verma, G. S. Role of four-phonon processes in the lattice thermal conductivity of silicon from 300 to 1300 K. *Phys. Rev. B* **1,** 642–646 (1970).

37. E., P., D., M., Q., W., K., G. & H, D. Thermal Conductance of an Individual Single-Wall Carbon Nanotube above Room Temperature. *Nano Lett.* **6,** 96 (2006).

38. Martin, P., Aksamija, Z., Pop, E. & Ravaioli, U. Impact of phonon-surface roughness scattering on thermal conductivity of thin Si nanowires. *Phys. Rev. Lett.* **102,** 1–4 (2009).

39. Sadhu, J. & Sinha, S. Room-temperature phonon boundary scattering below the Casimir limit. *Phys. Rev. B - Condens. Matter Mater. Phys.* **84,** 1–6 (2011).

40. Murphy, P. G. & Moore, J. E. Coherent phonon scattering effects on thermal transport in thin semiconductor nanowires. *Phys. Rev. B - Condens. Matter Mater. Phys.* **76,** 1–11 (2007).

41. Snyder, G. J. & Toberer, E. S. Complex thermoelectric materials. *Nat. Mater.* **7,** 105–114 (2008).

42. Hochbaum, a I., Fan, R., He, R. R. & Yang, P. D. Controlled growth of Si nanowire arrays for device integration. *Nano Lett.* **5,** 457–460 (2005).

43. Krylyuk, S., Davydov, A. V & Levin, I. Tapering control of Si nanowires grown from $SiCl_4$ at reduced pressure. *ACS Nano* **5,** 656–664 (2011).

44. Hippalgaonkar, K. *et al.* Fabrication of microdevices with integrated nanowires for investigating low-dimensional phonon transport. *Nano Lett.* **10,** 4341–4348 (2010).

45. Hochbaum, A. I., Gargas, D., Hwang, Y. J. & Yang, P. Single crystalline mesoporous silicon nanowires. *Nano Lett.* **9,** 3550–3554 (2009).

46. Peng, K.-Q., Yan, Y.-J., Gao, S.-P. & Zhu, J. Synthesis of Large-Area Silicon Nanowire Arrays. *Adv. Mater.* **14,** 1164–1167 (2002).

47. Dolling, G. Lattice vibration in crystals with diamond structures. *Symp. Inelast. Scatt. Neutrons Solids Liq.* **2,** 37–48 (1963).

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Author contributions

P.Yang conceived the ideas for the project. J.Lee, W.Lee, and J.Lim designed and performed the thermal transport experiments. J.Lee and W.Lee analyzed the data. J.Lee and W.Lee implemented theoretical models for phonon transport W.Lee performed finite-element thermal modelling. J.Lim carried out the rough nanowire synthesis and analyses. Y.Yu carried out the high-resolution TEM imaging and the elemental analysis. Q.Kong carried out the VLS nanowire synthesis. J.J. Urban and P.Yang guided the work. J.Lee, W.Lee, J.J.U, and P.Yang wrote the manuscript. All authors discussed the results and commented on the manuscript.

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Additional information

The authors declare no competing financial interests.

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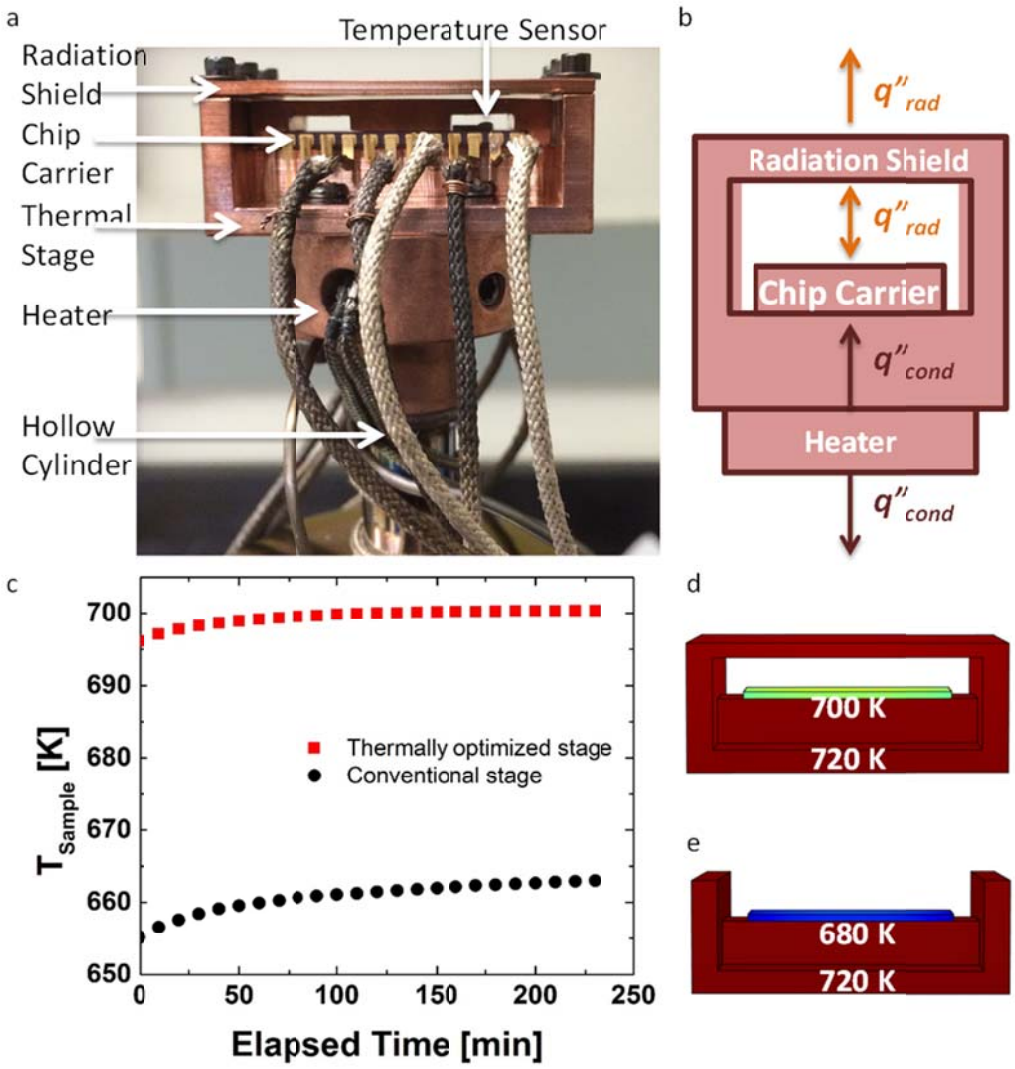

Figure 1. High-temperature experimental setup. **a,** Thermally optimized sample mount stage that enables thermal transport measurements up to 700 K. **b,** Schematic of important heat transfer paths through thermal conduction (q''_{cond}) and thermal radiation (q''_{rad}). **c,** Measured sample temperature for the thermally optimized stage compared to a conventional stage with no consideration to thermal contacts or radiation losses. The optimized stage demonstrates improved thermal coupling and a reduced time constant. **d,** FEM simulation result with a radiation shield **e,** FEM simulation result with no radiation shield. Given the same heater temperature (720 K), a higher sample temperature (700 K vs. 680 K) can be reached simply using a radiation shield, as verified by the experiment.

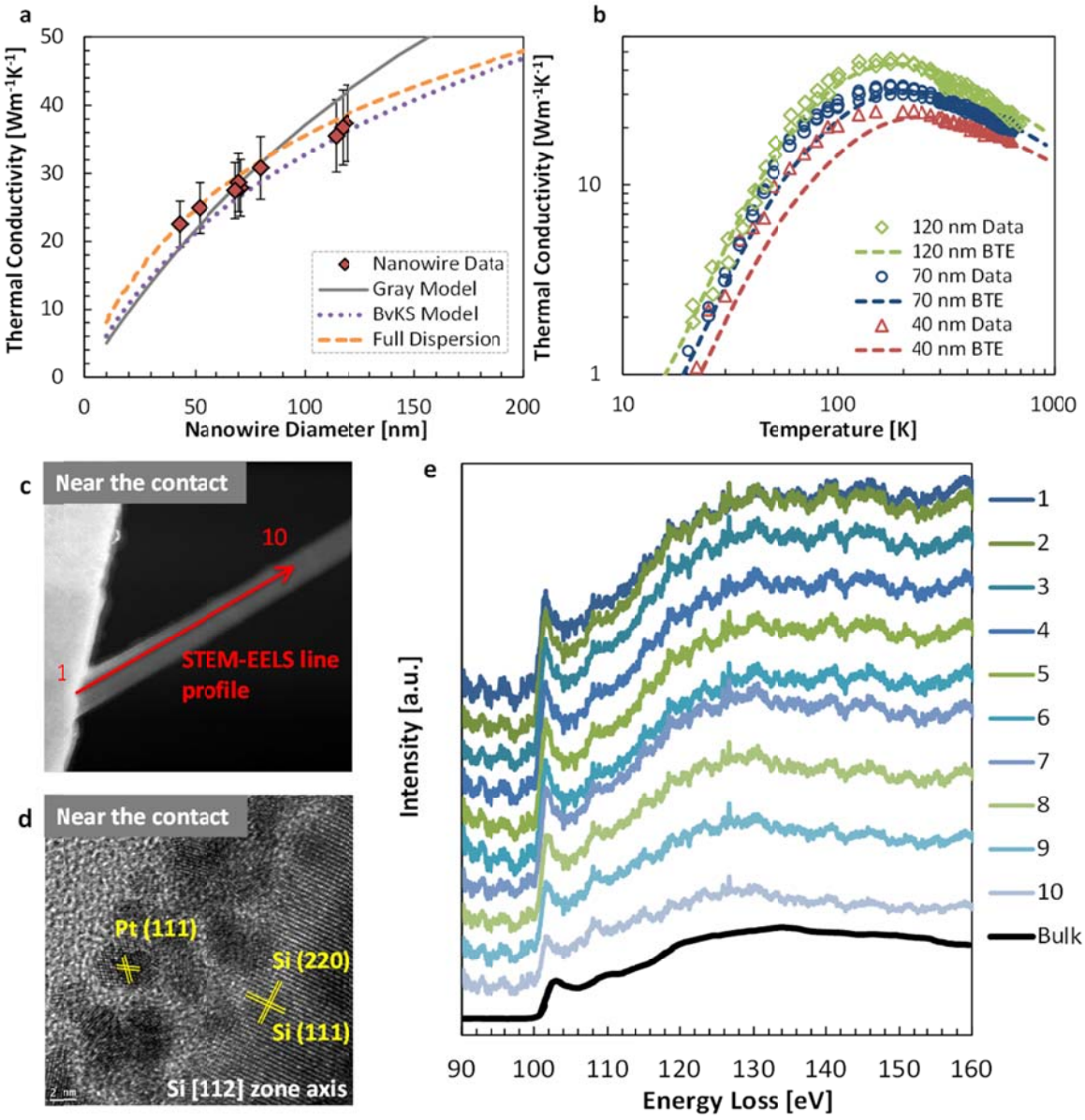

Figure 2. Thermal conductivity of VLS Si NWs and the material integrity. **a,** Diameter dependent thermal conductivity of VLS Si NWs from 40 nm to 120 nm at room temperature. Red filled diamond represents measured thermal conductivity. Gray solid line, purple dot line, and orange dash line represent theoretically estimated thermal conductivity with Gray model, BTE with BvKS, and BTE with full phonon dispersion relations, respectively. **b,** Temperature dependent thermal conductivity of VLS Si NWs from 20 K to 700 K. Dash lines show computed thermal conductivity using BTE model with full dispersion of acoustic and optical phonons and agree well with experimental data throughout the temperature range. **c,** STEM of VLS Si nanowire after multiple high-temperature excursions to 700 K. This particular nanowire was also exposed to more than four hours of the EBID while most other nanowires experienced about two hours of the EBID in average. The bright contrast implies a preferential deposition of heavy elements (i.e. Pt) near the contact area. The arrow indicates the EELS scanning location moving away from the contact as the number increases from 1 to 10. **d,** HRTEM image of near thermal contact shows strong presence of Pt at the nanowire surface. The Pt deposition is only appreciable near the contact and negligible near the center of nanowires. **e,** Electron energy-loss spectroscopy (EELS) results along the VLS Si NW near the contact area as indicated in Fig. 2c. The consistent spectra from the location 1 to 10 that match the bulk spectrum indicate the silicon nanowire is undamaged and there is no alloy formation even with the extensive exposures to EBID processes and high temperatures.

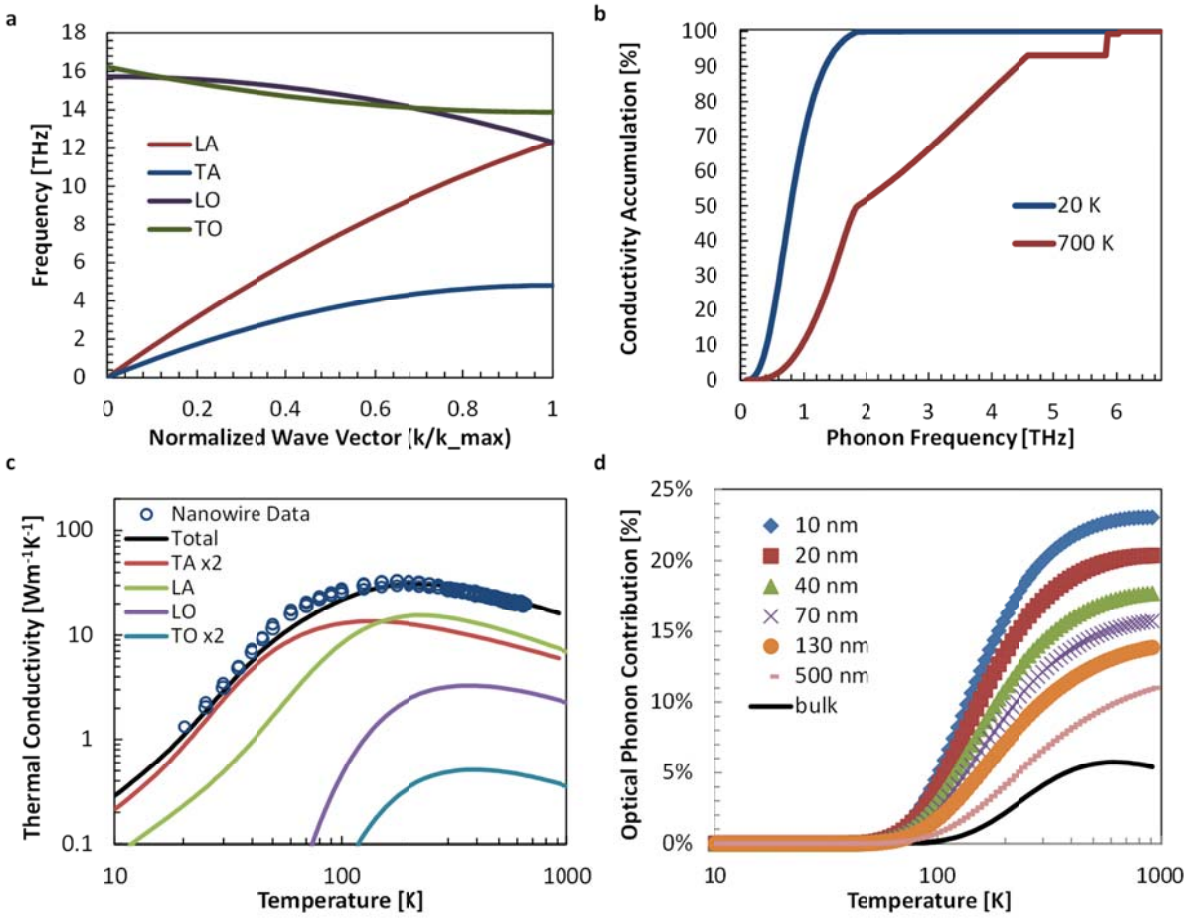

Figure 3. BTE modeling results based on full phonon dispersion relations. **a,** Phonon dispersions in silicon, which are modeled after the bulk silicon experiment[47]. While the transverse acoustic phonons (TA) and longitudinal acoustic phonons (LA) have large slopes, i.e. the group velocity, and low frequency modes, the transverse optical phonons (TO) and longitudinal optical phonons (LO) are only relevant at frequency greater than 12 THz. **b,** Frequency dependent phonon contributions to thermal conductivity in silicon. At 20 K, phonons with the frequency less than 1 THz carry 80 % of heat. At 700 K, phonons with the frequency less than 4 THz phonons carry 80 % of heat. **c,** Mode dependent thermal conductivity of 70 nm VLS Si NW and measured experimental data of 70 nm VLS Si NW . The acoustic phonons dominate thermal transport, but the optical phonons become important at high temperatures due to the relevance of high frequency modes. **d,** Temperature dependent optical phonon contribution to thermal conductivity in bulk silicon and nanowires of varying diameter. The optical phonons are not negligible to thermal transport, particularly in nanowires and at high temperatures.

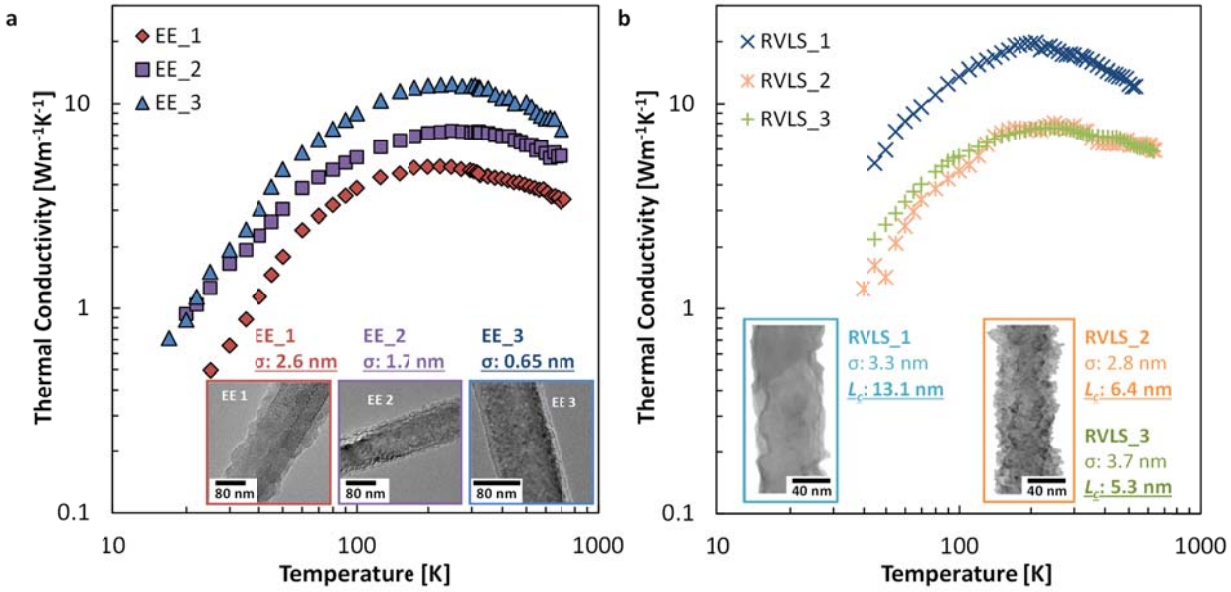

Figure 4. Experimental results of rough Si nanowires. **a,** Temperature dependent thermal conductivity data of electroless etched (EE) Si nanowires. The inset shows TEM images with corresponding roughness parameters including rms (σ) and correlation length (L_c) values. **b,** Temperature dependent thermal conductivity data of roughened VLS (RVLS) Si nanowires. The inset shows TEM images with corresponding rms (σ) and correlation length (L_c) values. While the EE nanowires show stronger dependence on the rms values, the RVLS nanowires show stronger dependence on the correlation length values. The high temperature data verify that the thermal conductivity reduction mechanisms are effective up to 700 K, which is a promising sign for thermoelectric applications. Due to strong effects of roughness, the diameter variations in these rough nanowires (120 nm for EE_1, 100 nm for EE_2, 103 nm for EE_3, 78 nm for RVLS_1, 70 nm for RVLS_2, and 62 nm for RVLS_3) are assumed less important for thermal transport, in accordance with our earlier studies[2,11].