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Abstract

With greater integration, the power dissipation in integrated circuits has begun to outpace the ability of today's heat sinks to limit the on-chip temperature. As a result, thermal issues have come to the forefront, and thermally aware design techniques are likely to play a major role in the future. While improved heat sink technologies are available, economic considerations restrict them from being widely deployed until and unless they become more cost-effective. Low power design is helpful in controlling on-chip temperatures, but is already widely utilized, and new thermal-specific approaches are necessary. In short, the onus on thermal management is beginning to move from the package designer toward the chip designer. This survey provides an overview of analysis and optimization techniques for thermally aware design. After beginning with a motivation for the problem and trends seen in the semiconductor industry, the survey presents a description

of techniques for on-chip thermal analysis. Next, the effects of elevated temperatures on on-chip performance metrics are analyzed. Finally, a set of thermal optimization techniques, for controlling on-chip temperatures and limiting the level to which they degrade circuit performance, are described.

Contents

1

Introduction

1.1 Overview

Thermal analysis is important in ensuring the accuracy of timing, noise, and reliability analyses during chip design. The thermal properties of integrated systems can be studied at a number of levels and length scales, as partly illustrated in Figure 1.1. For the problem of cooling racks of computing servers in a data center, the cooling structure must cover an area of the order of meter to tens of meters. At the next level, board-level cooling operates at length scales of the order of a tenth of a meter, while package level cooling corresponds to lengths of the order of centimeters. Within-chip solutions include microrefrigeration solutions, whose sizes range from the order of a millimeter to a centimeter [132] and can operate at the architectural level, to solutions that can scale down to several tens of microns [131] and operate at about the logic level.

In other words, the thermal problem is important at a wide range of length scales, and known cooling solutions exist at all of these levels. These solutions range in complexity and cost from the use of passive heat sinks, to active convective cooling using fans, to more exotic

Fig. 1.1 Manifestations of the thermal problem at a variety of length scales [72] ©Therminic reprinted with permission.

technologies based on microchannels and microrefrigeration. Some of these solutions are more traditional and have been available, in some form, for quite a few years, while others are relatively newer, and are actively being researched.

The genesis of thermal problems is in the fact that electronic circuitry dissipates power. This power dissipated on-chip is manifested in the form of heat, which, in a reasonably designed system, flows toward a heat sink. The power generated per unit area is often referred to as the heat flux. Temperature and power (or heat flux) are intimately related, but it is important to note that they are distinct from each other. For instance:

- For the same total power, it is possible to build systems with different peak temperature and heat flux distributions, simply by changing the spatial arrangement of the power sources. If all the high power sources are concentrated together in a region, that area will probably see a high peak temperature. Such a thermal bottleneck can often be relieved by moving the power sources apart.

- The relative location of the power sources to the heat sink also plays a part in determining the on-chip temperature, and by providing high-power elements with a conductive path to the heat sink, many thermal problems can be alleviated.

Most such optimizations can result in tradeoffs: for instance, thermal considerations imply that highly active units should be moved apart, but if these units communicate with each other, performance requirements may dictate that they be kept close to each other.

The focus of this survey is on presenting solutions for the within-chip thermal problem. However, an essential prerequisite to addressing thermal issues is the ability to model heat transfer paths of a chip with its surrounding environment, and to analyze the entire thermal system, including effects that are not entirely within the chip. Figure 1.1 shows a representative chip in a ceramic ball grid array (CBGA) packaging and its surrounding environment. This is modeled as a network of thermal resistors, using the thermal–electrical analogy to be described in Section 2.3.1, where power values map on to electrical currents, temperatures to voltages, and the ground node to the ambient.

In Figure 1.2, the chip is placed over a ceramic substrate, connected through flip-chip, or C4, connections all over its area. The substrate is connected to the printed circuit board through CBGA connections, and a small portion of the heat generated on-chip flows through this region to the ambient, which is denoted by the ground connection in the thermal circuit. At the other end, a heat sink with a large surface area is connected to the chip, with a thermal interface material lying between the chip and the heat sink. The role of the thermal interface material (TIM) is to act as a heat spreader. In the absence of this material, the surface roughness of the chip and the heat sink imply that the actual contact between the two surfaces could be as low as 1%–2% of the apparent surface area [111], and this is accentuated by warpage of the die under thermal stress; adding that the TIM improves the contact area, and consequently, the thermal resistance at this interface. The upper half of the thermal circuit shows how this region can be modeled.

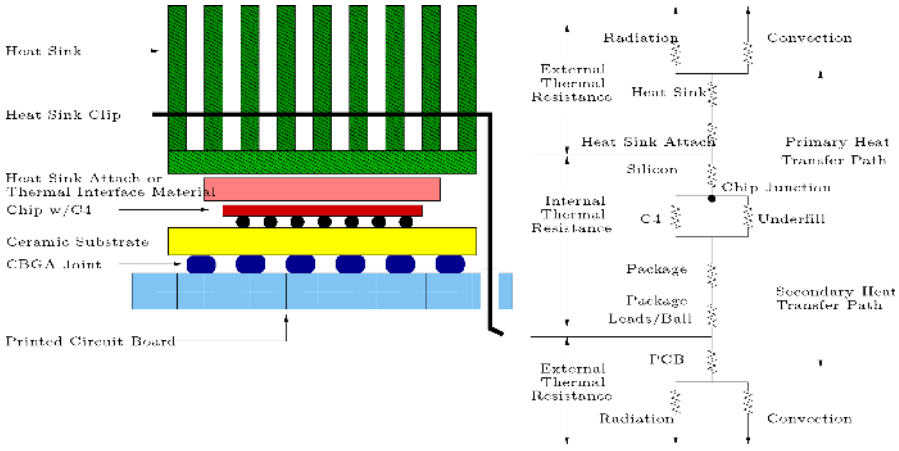

Fig. 1.2 Heat dissipation paths of a chip in a system [142] ©IEEE reprinted with permission.

Additional air-cooling schemes, such as fans that are connected to the heat sink, can be incorporated into this model.

A crucial step in design involves the choice of a heat sink: here, approximate techniques may be used to obtain a reasonable sinking solution [89], based on a gross characterization of the sink by its thermal resistance. At the package design level, a key item of interest is the thermal design power (TDP), which is the maximum sustained power dissipated by an integrated circuit. This is not necessarily the peak power: if the peak power is dissipated for a small period of time that is below the thermal time constant, it does not appreciably affect the choice of the heat sink. If the peak temperature is to be maintained at a temperature T_{peak} above the ambient temperature, then the maximum thermal resistance of the heat sink is given by a simple formula based on a lumped DC analysis:

$$R_{\text{sink}} = T_{\text{peak}}/\text{TDP}. \tag{1.1}$$

The choice of the heat sink can be made on the basis of this requirement. Note that this is a very coarse analysis that does not consider transient effects.

1.2 Thermal Trends

1.2.1 The Importance of Temperature as a Design Consideration

The problem of getting the heat out of a chip is not new: indeed, power issues have been at least partially if not wholly responsible for the demise of a variety of technologies before CMOS. For instance, as demonstrated in Figure 1.3, the rapidly increasing power dissipation trends in bipolar circuits played a large role in their displacement as the dominant technology of the day, being taken over first by NMOS and then by CMOS. Today, no clear successor to CMOS has emerged, but on-chip power dissipation has emerged as a major design bottleneck, and it is ever more important to build cooling solutions from the system level down to the subchip level. Historical trends, illustrated in Figure 1.3, show an ever-increasing profile for the volume of the external heat sink as on-chip power goes up, and this is unsustainable.

As illustrated in Figure 1.4, trends show that the cost of the cooling solution is a nonlinear function of the chip power dissipation: the initial rise is gentle, but beyond the point of convective cooling, the costs rise

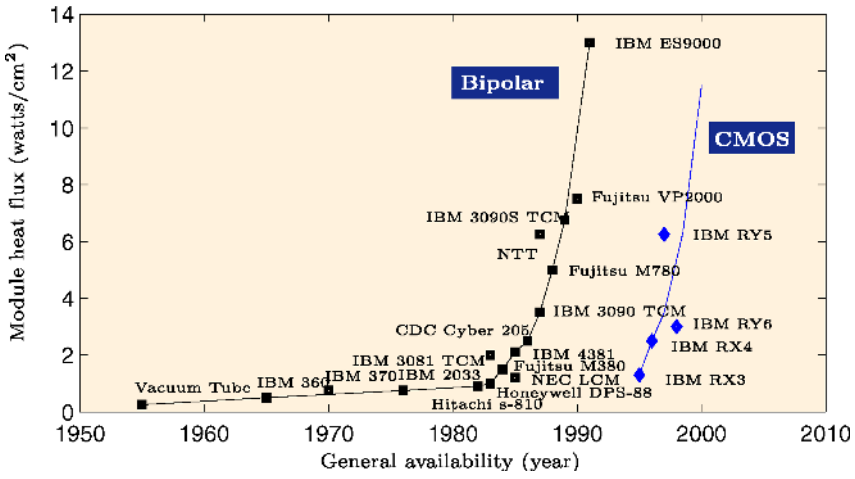

Fig. 1.3 Trends for the heat flux for state-of-the-art systems over the years [27] ©IEEE reprinted with permission.

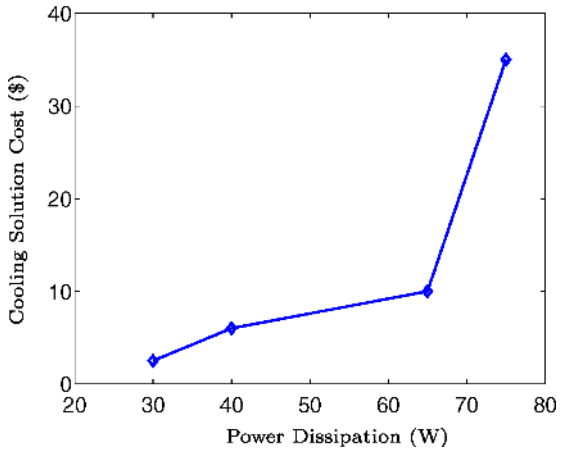

Fig. 1.4 Cooling costs as a function of the power dissipation [55] ©Intel Technology Journal reprinted with permission.

steeply. This knee point is a function of cooling system complexity and the volume of actively cooled packages/technologies, and may arguably permit slightly higher on-chip power dissipation in the future as newer technologies gain economies of scale, but the fundamental nature of the curve — of having a gentle ascent followed by a steep rise beyond a knee point — is unlikely to change. This has consequences on the size of the heat sink, and Figure 1.5 shows how the volume of the heat sink has increased with increased on-chip power.

To achieve the required heat sinking solution, it may be necessary to increase the heat sink size to unreasonable levels, or to move to new cooling technologies. For contemporary high-end, large-volume parts, anything that is more complex than air-cooling is probably too expensive. Although several of the bipolar chips in Figure 1.3, after 1980, used some form of water cooling [27], liquid cooling is not seen as a very viable solution today. There have been numerous improvements even in air-cooled technologies and improved thermal interface materials in the recent past, which have progressively shifted the knee of the cooling cost curve of Figure 1.4 progressively to the right, so that the heat fluxes that are currently obtained by air cooling could only be achieved by liquid cooling in the 1980s [122]. However, even these

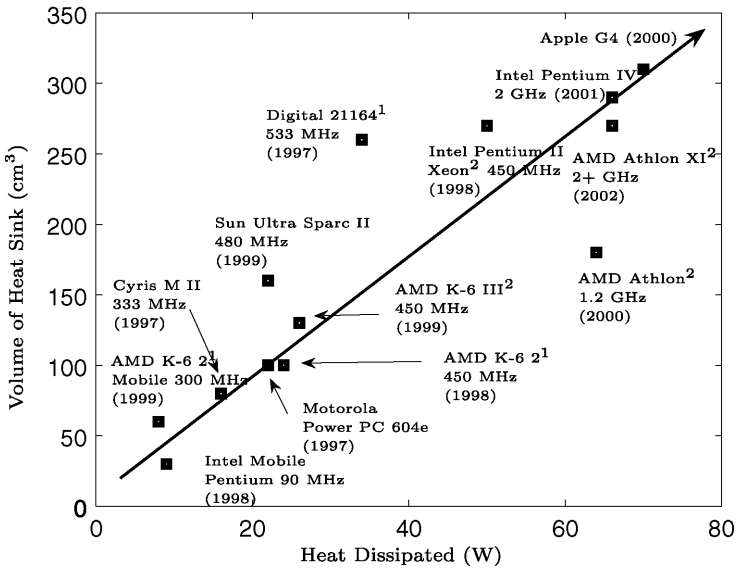

Fig. 1.5 Historical data showing the volume of the heat sink as a function of the total on-chip power [72].

improvements cannot keep up with the capability of Moore's law to integrate more functionality on a chip. Indeed, while it is possible to pack more transistors on a chip today, only a fraction of them can actually be used to full potential, because of power and thermal limitations. More advanced solutions using, for example microfluidic channels and microrefrigeration, have been proposed, these are not cost-effective enough for widespread use today.

1.2.2 Thermal Issues in 3D Integrated Circuits

The previous subsection explains why temperature must be an important consideration in the design of nanoscale integrated circuits. A further motivator for thermally conscious design has come about with the advent of three dimensional (3D) integration, which makes the on-chip problem particularly acute.

Unlike conventional 2D circuits, where all transistors are placed in a single plane, with several layers of interconnect above, 3D circuits stack tiers of such 2D structures, one above the other. 3D structures may be

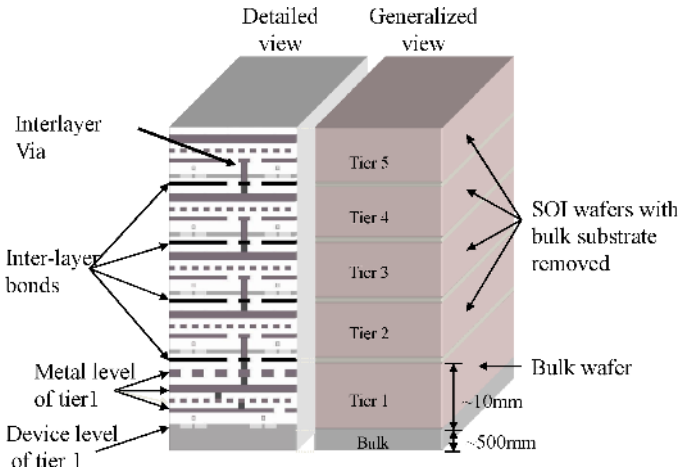

Fig. 1.6 A schematic of a 3D integrated circuit.

built by stacking tiers of dies above each other, where the separation between tiers equals the thickness of the bulk substrate, which is of the order of several hundreds of microns. Advances in industrial [54], government [18], and academic [119] research laboratories have demonstrated 3D designs with inter-tier separations of the order of a few microns, enabling short connections between tiers, accentuating the advantages of short vertical interconnections in these 3D structures. A schematic of a 3D chip is illustrated in Figure 1.6, showing five tiers stacked over each other. The lowest tier sits over a bulk substrate, while the other tiers are thinned to remove the substrate, and provide inter-tier distances of the order of ten microns.

With these technological advances, 3D technologies provide a roadmap for allowing increased levels of integration within the same footprint, in a direction that is orthogonal to Moore's law. Moreover, 3D technologies provide the ability to locate critical blocks close to each other, e.g., by placing memory units in close proximity to processors by placing them one above the other. These, and other, advantages make 3D a promising technology for the near future.

However, the increased packing density afforded by 3D integration has the drawback of exacerbating thermal issues. Based on a simple

back-of-the-envelope calculation, a k-tier 3D chip could use k times as much current as a single 2D chip of the same footprint; however, the packaging technology is not appreciably different. This implies that the corresponding heat generated must be sent out to the environment using a package with essentially similar heat sinking capabilities. As a result, the on-chip temperature on a 3D chip could be k times higher than the 2D chip. While this is a very coarse analysis with very coarse assumptions, the eventual conclusion — that thermal effects are a major concern in 3D circuits — is certainly a strong motivator for paying increased attention to thermal issues today.

1.3 Organization of the Survey

This survey begins its discussion of on-chip thermal effects by surveying techniques for evaluating the distribution of temperature on a chip. These analysis techniques essentially solve a partial differential equation (PDE) that relates the power dissipated on a chip to its temperature profile. While the solution of PDEs is a well-studied problem, it is possible to take advantage of some specific properties of the on-chip problem to obtain an efficient solution. Moreover, thermal analysis shows similarities to other well-studied problems in integrated circuit design, most notably, those of analyzing on-chip power grids [128], and of substrate analysis [46, 36], and techniques from these domains can be borrowed to enhance the quality of algorithms for thermal analysis.

Next, we study the manner in which on-chip temperatures affect the properties and performance of a circuit. In terms of delay, the performance of transistors and the resistance of interconnect wires can be affected; in terms of power dissipation, there is a strong relationship, with potential feedback, between temperature and leakage power; in terms of reliability, the lifetime of both devices and interconnects all depend critically on the operating temperature of the circuit. These are all critical factors in ensuring circuit performance, and the complexity of these problems makes it essential to build efficient and scalable CAD solutions for on-chip thermal analysis. Finally, we overview some representative techniques for thermally driven circuit optimization.

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