Thermally induced stresses resulting from coefficient of thermal expansion differentials between an LED sub-mount material and various mounting substrates

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ABSTRACT

A study has been conducted to determine the effects of mechanical stresses induced from the coefficient of thermal expansion (CTE) differential between a light emitting diode (LED) chip, and various substrate materials to which the LEDs were mounted. The LEDs were bonded to typical packaging materials including ceramics, copper and metal matrix composites. The objective of this investigation was to determine the viability of implementing alternate substrate materials for packaging of LED power chips. In particular, thermally induced stresses resulting from the CTE differentials between the alternate substrate materials and the LED sub-mount material were analyzed and compared against the stresses resulting from the nearly ideal CTE match that is realized with traditional ceramic substrates.

Keywords: light emitting diode, thermal management, coefficient of thermal expansion, thermal stresses, LED packaging, thermal conductivity.

1. INTRODUCTION

Thermal management is of critical importance when designing an LED based lighting system to ensure product reliability and longevity [1-3]. As the junction temperature of an LED rises past its ideal operating condition, the brightness and life of the chip tend to degrade.

LED chip performance, as defined by wall plug efficiency, optical power, brightness, reliability, and cost, continues to make significant strides as new opportunities for demanding lighting applications emerge. Many high brightness applications, such as projection display and endoscopy, in which system-level etendue must be conserved are particularly vulnerable to the effects of high thermal flux densities at the LED. In designing a thermal management solution for an LED package for high brightness applications, primary considerations include: maximizing thermal conductivity, minimizing the mismatch in the thermal coefficient of expansion, and minimizing cost. This investigation has a particular focus on examining the effects of stresses induced on the LED chip resulting from the mismatch in thermal coefficient of expansion between the LED chip and the substrate to which it is mounted, while balancing the CTE effects in light of optimizing the thermal conductivity of the package and overall package cost.

1.1 Failure mechanisms in LEDs

Several possible types of failure modes can occur in an LED package. Some failures are abrupt catastrophic material failures, while others cause gradual degradation of light output over many hours or years of operation. It has been shown previously that thermally induced stress can be the root cause for LED failures [1-4]. Sudden material failure at the chip attachment surface can result in portions of the LED being inadequately cooled, or completely detached. There are, however, other stress induced failures which are more subtle and require time to bring the failure to a noticeable point.

In a study of Gallium Arsenide based LEDs, Zaeschmar & Speer suggested that the failure mode at the LED may be caused by a stress induced increase in the number of lattice defects in the chip junction [4]. The thermal or otherwise induced stress at the LED junction is believed to produce non-radiative defects in the crystal lattice which allow additional current to flow through the junction without any additional light output. The authors derived an analytic formula which relates the rate of change in light output to temperature and stress, which agrees well with empirical data. An exponential relationship between stress and the rate of degradation in LED brightness was determined.

$$dB/dt \sim f(\sigma) = \sigma^n$$

where,

dB/dt = Rate of change in LED brightness
σ = Stress level

For the case of a Gallium Arsenide LED, it was shown that the rate of change in LED brightness is proportional to the third power of the stress (n=3).

Further, the relationship between the LED junction temperature and the rate of change in brightness was determined to be:

$$dB/dt \sim e^{(-c/T)}$$

where,

e = Natural logarithm
c = Constant related to the activation energy
T= Junction temperature

1.2 LED chip construction

Many of the highest performance LEDs on the market today are 1mm power chips from manufacturers including Cree Inc., OSRAM GmbH, Epistar Corporation, and others. Due to the relatively large size of the power chips, they are of greatest concern with respect to thermally induced stresses from CTE mismatches between the chip and its mounting substrate. A typical power chip construction is shown in Figure 1. From the figure, the expitaxial layer comprised of either InGaN or AlInGaP sits on top of a silicon sub-mount. Below the silicon sub-mount is a thin layer, on the order of 3 microns, of gold-tin (AuSn) eutectic for bonding the chip to a substrate for the purposes of thermal management and packaging. Typical thickness of the 1mm power chip is approximately 100-150 microns [5].

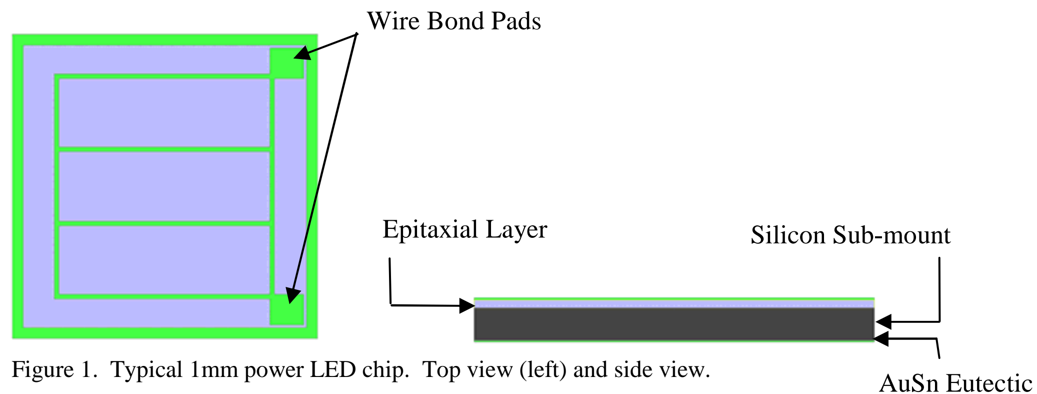

Figure 1. Typical 1mm power LED chip. Top view (left) and side view.

1.3 Typical LED Packages

The standard approach for designing a package for a power chip is shown in Figure 2. The LED is mounted to a ceramic substrate with a thin layer of solder. The ceramic substrate is then soldered to a metal heat sink. A well designed package for a power chip will have a thermal resistance on the order of 5-10 °C/W. The ceramic substrate serves several important functions in the package. First, the ceramic electrically isolates the LED from the metal heat sink material below it, thus preventing the heat sink from being electrical active. Second, ceramic PCB technology allows an array of LEDs to be packed at a high density and wired in series. High density packing of the LED chips enables the etendue of the system to be conserved, while wiring the LEDs in series enables the system to be run at a relatively low operating current. Third, the differential in coefficient of thermal expansion between the ceramic material and the LED sub-mount is minimal, thereby minimizing thermally induced stresses into the chip [6]. Finally, ceramics such as Beryllium Oxide (BeO) and Aluminum Nitride (AlN) have high thermal conductivities, which promote the spreading of heat from the LED, and the transfer of heat to the metal heat sink.

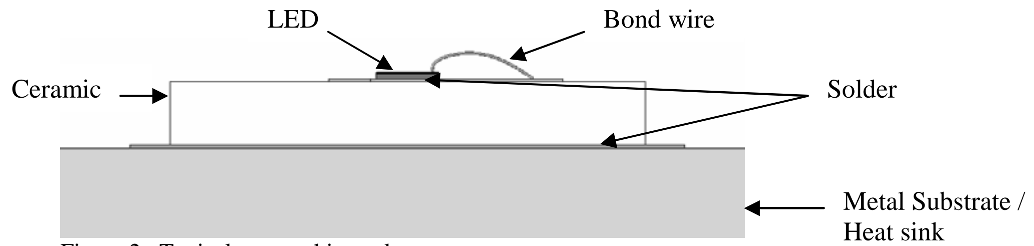

Figure 2. Typical power chip package.

As a cost savings, lower power LEDs often substitute a dielectric layer in place of the ceramic material to separate the electrical path from the underlying metal heat sink – see Figure 3. However, with a typical thermal conductivity ranging from 2-10 W/m-K, the dielectric layer tends to significantly add to the thermal resistance of the package. The thermal resistance of a dielectric based LED package is in the neighborhood of 50 °C/W, and consequently, dielectric layers within the LED package are not desired for high brightness packages using power chips.

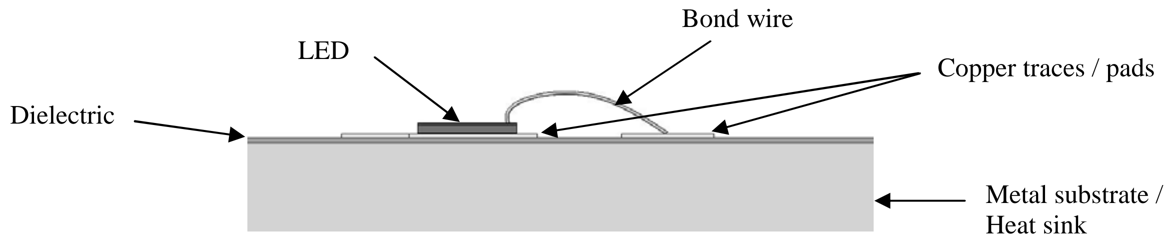

Figure 3. Dielectric based LED package.

As shown in Figure 4, an alternate high brightness power chip packaging approach is to solder the LED chip directly to a metal substrate, without having an additional ceramic or dielectric layer. The benefits of this approach include increased thermal conductivity through the package, and cost reduction. From an electrical design perspective, this approach results in an electrically active metal base, as well as higher current draws for a package that incorporates a multiplicity of LEDs wired in parallel. Beyond the electrical design considerations, the primary concerns in mounting LEDs directly to metal are product reliability and degraded life resulting from the CTE mismatch between the LED sub-mount and the metal substrate.

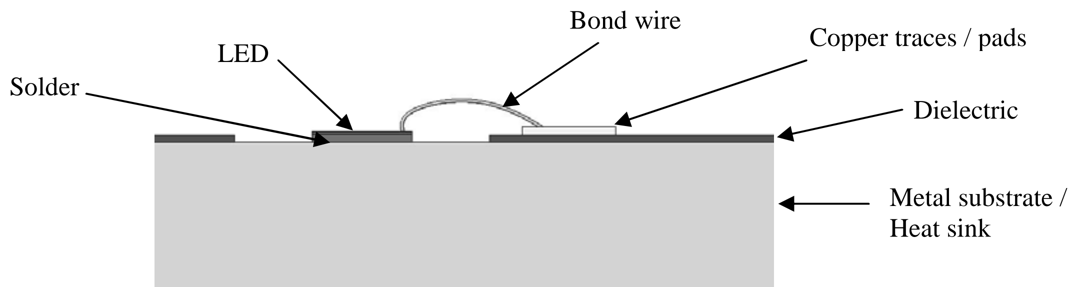

Figure 4. Direct to metal LED package.

1.4 Materials Properties

In this investigation, three distinct substrate materials were evaluated as shown in Table 1. Also shown in Table 1 are the thermal properties of silicon, which is the LED sub-mount material for this investigation [1]. Of particular note is the differential in the CTE between silicon and the substrate materials to which it is bonded. From the table, the CTE of the LED silicon sub-mount in nearly ideally matched to the CTE of the aluminum nitride ceramic material. The mismatch in CTE between silicon and copper is substantially greater than that of silicon and AlN [7].

Table 1 also lists the thermal properties of a metal matrix composite material: aluminum silicon carbide (AlSiC) [8]. AlSiC began gaining acceptance in the early 1990s as a packaging substrate material for the electronics industry, and in particular for applications such as microwave, microelectronics, and power electronic applications. Recently, AlSiC has been implemented as a packaging material within the optoelectronics industry. AlSiC is being evaluated as an alternative to the other substrate materials in this study as it has a close CTE match with silicon while providing high thermal conductivity.

Material	**Coefficient of thermal expansion (CTE) ($x10^{-6}/°C$)**	**CTE Differential with Silicon ($x10^{-6}/°C$)**	**Thermal conductivity (W/m-K)**
Copper	16.5	12.5	398
Aluminum Nitride	4.5	0.5	175
Aluminum Silicon Carbide	9.0	5.0	180
Silicon (LED sub-mount)	4.0	n/a	148

Table 1. Thermal properties of LED sub-mount and substrate materials.

2. METHODOLOGY

The objective of this investigation was to collect performance data for three distinct LED package configurations prior to and after stressing the packages via thermal cycling. The three LED packaging configurations are shown in Figures 5-7. The LED chip used for the experiment was the 1mm Cree Inc., 450nm EZ Bright power chip, part number C450EZ1000. All LED chips were bonded to their respective substrate materials via a eutectic attachment process by re-flowing the AuSn solder on the bottom of the silicon sub-mount at a temperature of approximately 280°C. Alternate attachment methods have been investigated [9, 10], however, the eutectic process is considered an effective and reliable process for attaching a power chip to an underlying substrate. All performance testing was conducted at ambient room temperature, and at rated electrical input of 1W per package.

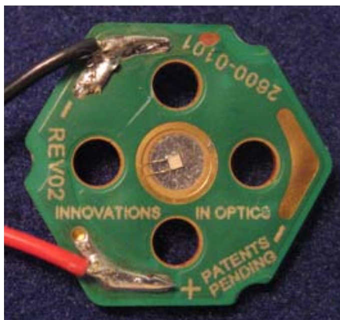

Figure 5. Power chip mounted to copper substrate.

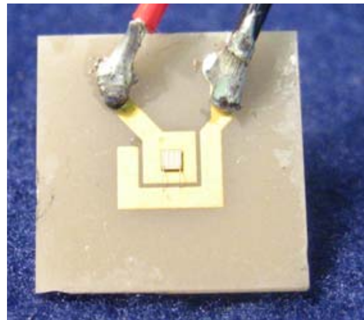
Figure 6. Power chip mounted to Aluminum Nitride ceramic substrate.

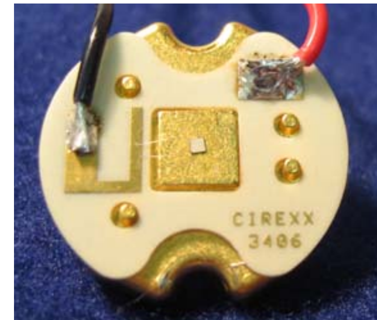

Figure 7. Power chip mounted to Aluminum Silicon Carbide substrate.

As shown in Figure 8, each thermal cycle consisted of a dwell time of 10 minutes at -40°C and 100°C with a temperature gradient of 14°C/minute between each dwell period. The units were removed from the oven after completing 1,000 full cycles.

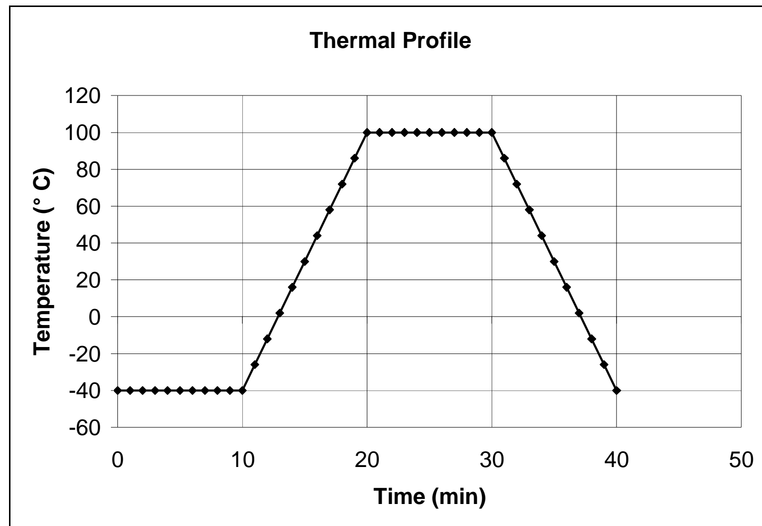

Figure 8. Thermal cycle profile.

All of the units under test were mounted in a high temperature plastic fixture. The units attached to the fixture via their electrical lead wires, thereby removing any thermal conduits to the substrate from the fixture or the oven. The LED packages were not powered during the test since the goal of the test was to examine the effects of stressing the bond between the LED and its sub-mount from +100C to -40C. If the units had been powered, the LEDs would have contributed additional heat and the temperature at the critical interface would not have been in accordance with the test objective.

2.1 Test plan

A sample size of 10 of each of the three configurations shown in Figures 5-7 were fabricated for the experiment. Prior to thermally cycling the 30 units, the devices were measured to set a baseline for luminance, spectral output, forward voltage, current, and infrared imaging analysis. The optical test set up for the measurement is shown in Figure 9. At the completion of the thermal cycling experiment, the 30 units were re-measured to investigate any evidence of a change in performance.

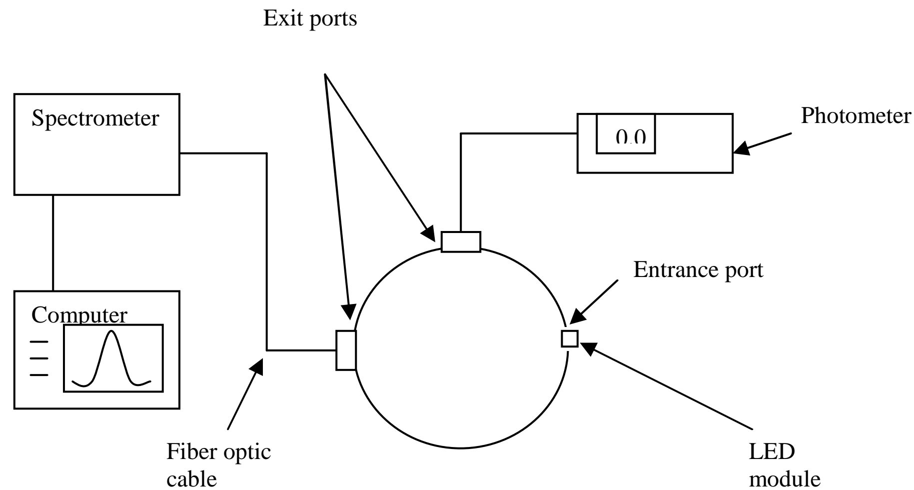

Figure 9. Test set up for optical measurements.

2.2 Infrared camera measurement

In addition to optical characterization of the unit under test, each device was measured using a thermal imaging camera. A 3-5 micron InSb thermal camera from Inframetrics, Inc. was implemented for the IR data. Thermal imaging of the LED provides qualitative insights into chip performance that may not be apparent when testing with visual inspection or luminance and spectral output. A chip that is free of defects will show a uniform temperature profile across the entire chip; however, a chip that is defective will tend to have localized "hot spots" as can be seen in figure 10. The inhomogeneous thermal areas are typically due to discontinuous regions of forward voltage resulting from the root cause of the defect, and are often related to thermal damage of the LED junction.

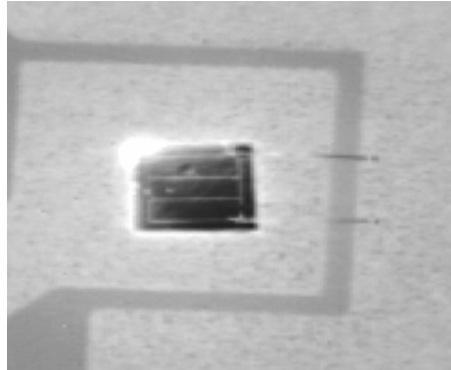

Figure 10. IR Image of a defective LED assembly.

3. DATA AND RESULTS

3.1 Theoretical Analyses

Finite element analysis was conducted to theoretically predict the thermally induced stresses in the LED substrate material that could be expected during the experiment. The purpose of the models was to provide insight into the probability of catastrophic mechanical failure for each of the three packaging configurations under consideration.

Table 2 summarizes results from the calculations of the Von Mises stress on the LED at the temperature extremes for the experiment. Von Mises stress was used as the criterion to predict LED failure since it provides measure of the onset of yield in ductile materials. The data have been normalized to an operating condition of +100C for the case of the LED mounted to a copper substrate. From the data, the Von Mises stress for the copper substrate is approximately 5X greater than that of the aluminum silicon carbide substrate, and about 10X greater than that of the aluminum nitride substrate. The reason the stresses are considerably higher at the low temperature extreme is because the LED chip is bonded to the LED at elevated temperature, which is typically about 280C for a eutectic attachment. As the temperature deviates from the temperature at which the chip was bonded to the substrate, the stresses increase.

Substrate Material	Relative Von Mises stress at +100C	Relative Von Mises stress at -40C
Copper	1.00	2.55
Aluminum Silicon Carbide	0.55	1.31
Aluminum Nitride	0.11	0.28

Table 2. Relative Von Mises stress at the experimental thermal extremes.

3.2 Test Data

Performance data was generated for each of the 30 units under test, both before and after thermal cycling. Measured data includes results from optical testing, electrical testing, and IR imaging tests.

3.2.1 Optical Test Data

Figures 11-13 show the optical power from each unit under test. As shown in Figure 14 and in Table 3, thermally cycling the test units resulted in little to no change in the optical power. No significant difference in optical power performance was noted for any of the three distinct packaging configurations, as any differences in optical power were within the margin of error for the measurement.

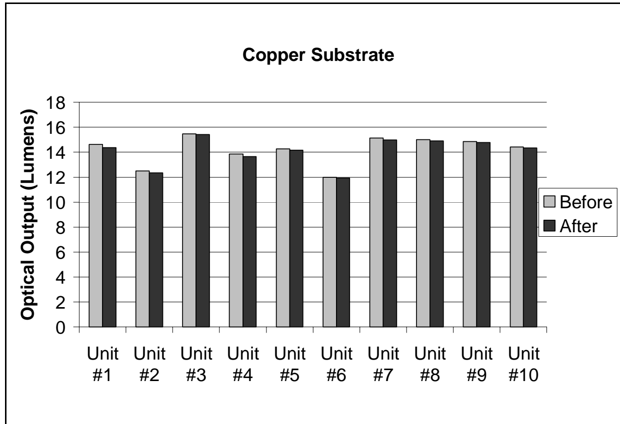

Figure 11. Optical power for LED mounted to copper.

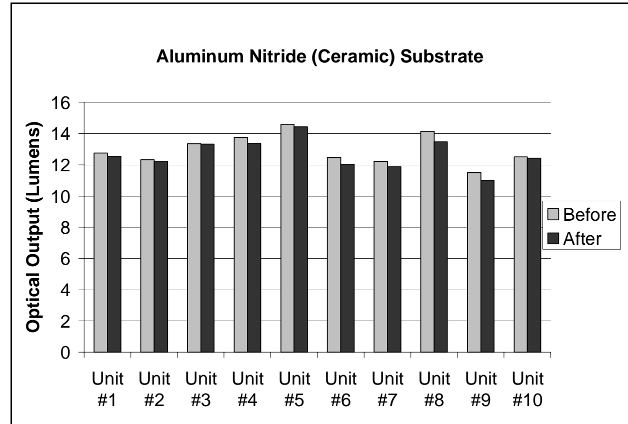

Figure 12. Optical power for LED mounted to ceramic.

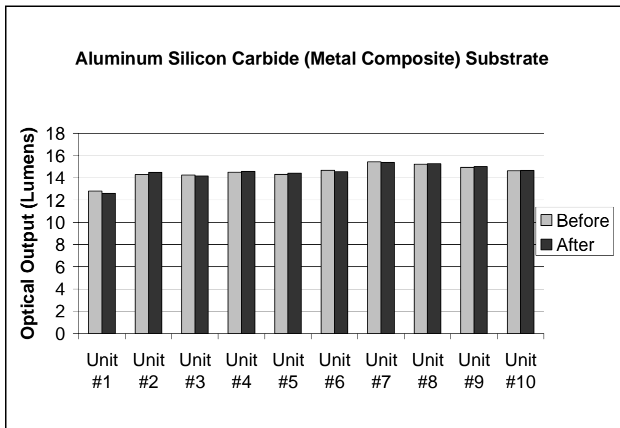

Figure 13. Optical power for LED mounted to AlSiC.

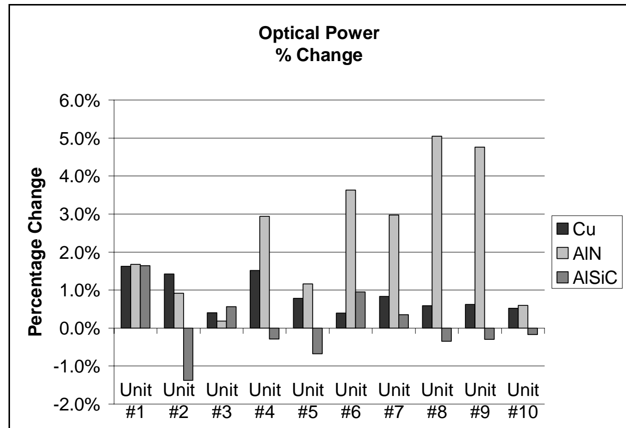

Figure 14. Percent change in optical power before and after thermal cycling test.

Substrate Material	Average change (%)	Standard Deviation of % change
Copper	0.87	0.47
Aluminum Silicon Carbide	0.03	0.86
Aluminum Nitride	2.39	1.70

Table 3. Summary of test data before and after thermal cycling.

The optical spectrum for each LED package type was measured before and after thermal cycling in an attempt to quantify the impact of thermally induced stress on spectral content. Figure 15 displays the spectrum for a representative sample of each package type. From the figure, the spectral output of the LEDs was not significantly affected by the thermal cycling test.

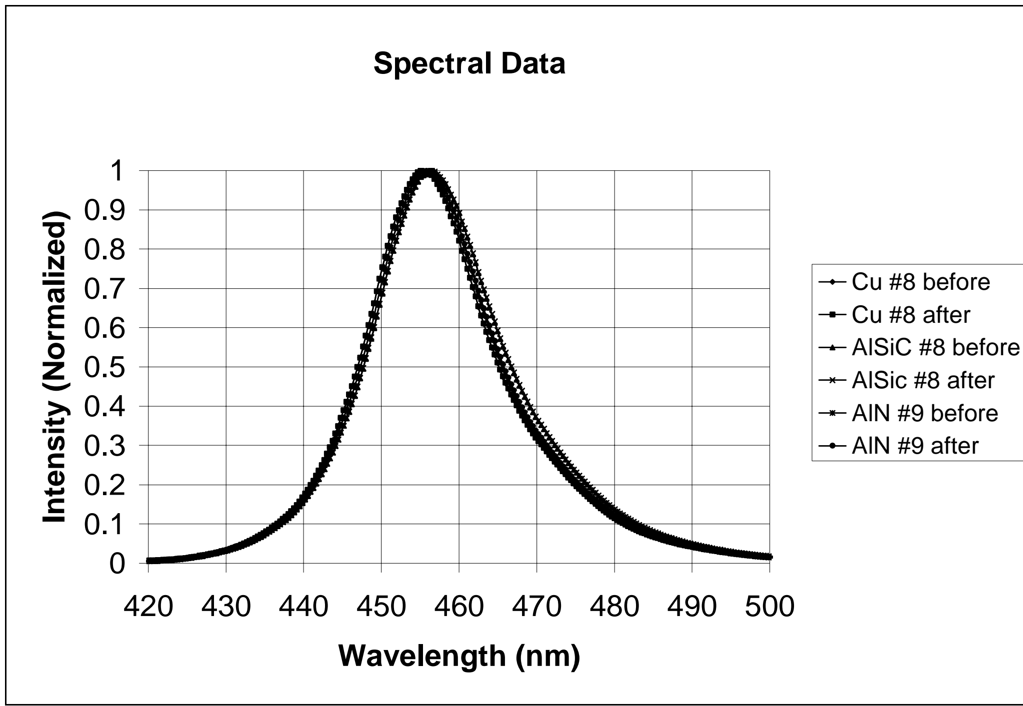

Figure 15. LED spectra before and after thermal cycling.

3.2.2 Electrical Test Data

It has been shown previously that the forward voltage of an LED increases as a function of stress applied to the LED material [11]. Figures 16-18 present the measured forward voltage data, and Figure 19 and Table 4 summarize the data. As with the prior data, there is no discernable impact on forward voltage with any of the configurations under test.

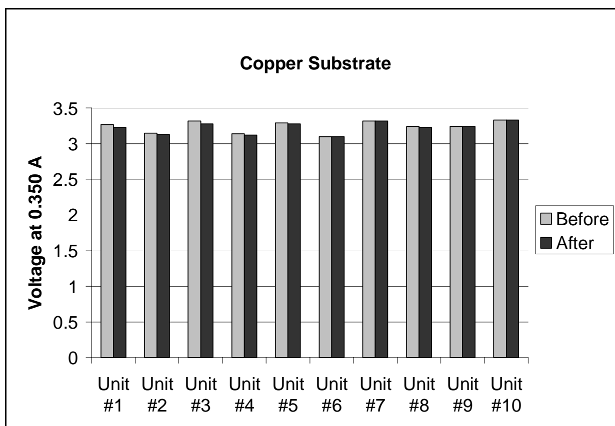

Figure 16. Forward voltage of LED on copper.

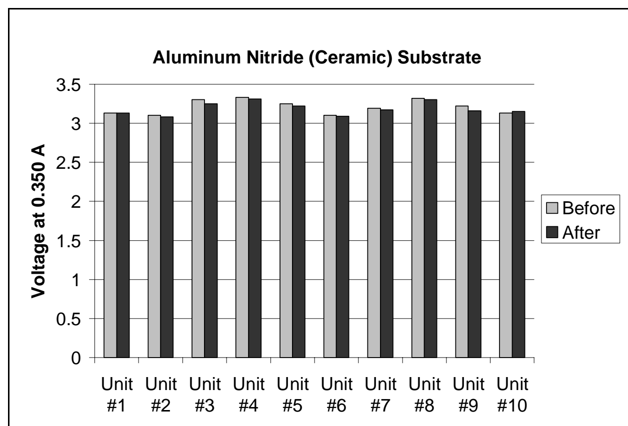

Figure 17. Forward voltage of LED on ceramic.

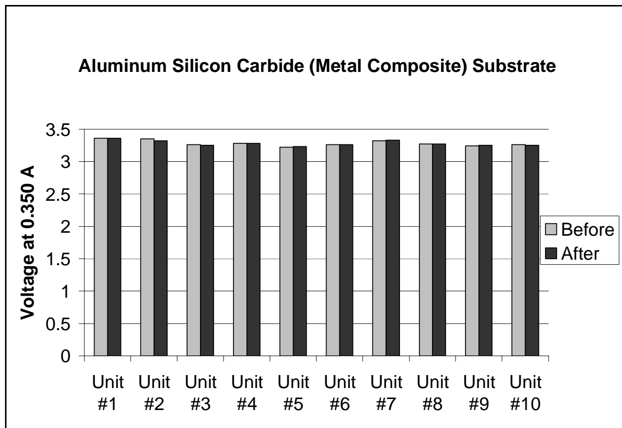

Figure 18. Forward voltage of LED on AlSiC.

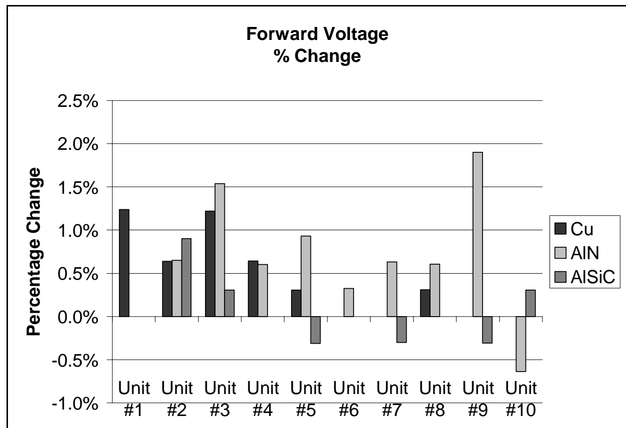

Figure 19. Percent change in forward voltage before and after thermal cycling test.

Substrate Material	Average change (%)	Standard Deviation of % change
Copper	0.44	0.49
Aluminum Silicon Carbide	0.06	0.37
Aluminum Nitride	0.65	0.72

Table 4. Summary of test data before and after thermal cycling.

3.2.3 Infrared Camera Images

Figures 20 and 21 show a representative sampling of infrared imaging of the LED chip. No significant qualitative change was detectable in any of the units under test via IR imaging analysis.

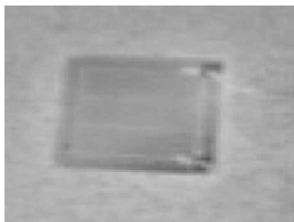

Figure 20. IR image of LED before thermal cycling.

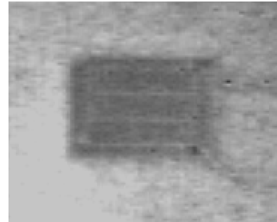

Figure 21. IR image of LED after thermal cycling.

4. CONCLUSIONS

FEA modeling and analyses suggest that the magnitude of thermally induced stress at the LED junction is strongly related to the CTE differential between an LED sub-mount and the substrate material to which it is bonded. Further, LED brightness and life are highly correlated to the stress at the LED junction. Results from thermally cycling LED packages consisting of CTE differentials ranging from 0.5-12.5 $x10^{-6}$/°C showed no significant difference in LED performance as measured optically, electrically, and with infrared imaging. From the data, it can be inferred that even under the worst case CTE differential, silicon onto copper, catastrophic mechanical failure did not occur, and that bonding an LED with a silicon sub-mount directly to copper may be a viable option for LED packaging engineers. In addition, since the CTE differential for aluminum silicon carbide is lower than that of copper, it is reasonable to suggest that AlSiC could be considered as a substrate packaging material for LED power chips.

Theoretical modeling indicates that the Von Mises stress level caused by the CTE mismatch between silicon and copper can be as much as 10X greater than that of standard ceramic substrates such as aluminum nitride. The mode of failure induced by propagation of defects in the crystal lattice may be occurring at the elevated stress levels associated with bonding an LED power chip to a copper substrate. Although the thermal cycling experimental results did not indicate any obvious performance degradation due to thermal stress or fatigue, the theoretical levels of stress are high enough to warrant additional investigation. Consequently, the authors recognize the importance of obtaining additional lifetime data prior to advocating the widespread use of non-traditional substrate materials for LED packaging.

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