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Thermomechanical Characterization and Modeling for TSV Structures

Tengfei Jiang^a, Suk-Kyu Ryu^b, Qiu Zhao^a, Jay Im^a, Paul S. Ho^a, and Rui Huang^b

^a*Microelectronics Research Center, University of Texas, Austin, TX 78712*

^b*Department of Aerospace Engineering and Engineering Mechanics, University of Texas, Austin, TX 78712*

Abstract. Continual scaling of devices and on-chip wiring has brought significant challenges for materials and processes beyond the 32-nm technology node in microelectronics. Recently, three-dimensional (3-D) integration with through-silicon vias (TSVs) has emerged as an effective solution to meet the future technology requirements. Among others, thermo-mechanical reliability is a key concern for the development of TSV structures used in die stacking as 3-D interconnects. This paper presents experimental measurements of the thermal stresses in TSV structures and analyses of interfacial reliability. The micro-Raman measurements were made to characterize the local distribution of the near-surface stresses in Si around TSVs. On the other hand, the precision wafer curvature technique was employed to measure the average stress and deformation in the TSV structures subject to thermal cycling. To understand the elastic and plastic behavior of TSVs, the microstructural evolution of the Cu vias was analyzed using focused ion beam (FIB) and electron backscattering diffraction (EBSD) techniques. Furthermore, the impact of thermal stresses on interfacial reliability of TSV structures was investigated by a shear-lag cohesive zone model that predicts the critical temperatures and critical via diameters.

Keywords: through-silicon via; thermal stress; via extrusion; interfacial reliability.

INTRODUCTION

Through-silicon-via (TSV) is a key element for 3-D integration in providing vertical interconnects for chip-stacking structures. Copper (Cu) is widely used as the via filling material because it is compatible with both the front-end of line (FEOL) and back-end of line (BEOL) processes. However, the mismatch in the coefficients of thermal expansion (CTEs) between Cu and Si is relatively large, which is responsible for the development of thermal stresses in the TSV structures. The thermal stresses can arise during fabrication, testing and service of the TSVs, leading to various reliability issues, such as crack growth, via extrusion, and degradation of device performance [1-4]. Therefore, it is important to experimentally characterize the thermal stresses and understand their impact on TSV reliability for development of 3-D interconnects.

This paper is organized in two parts. The first part presents the experimental methods for stress characterization. A precision wafer curvature technique has recently been applied to measure the thermal stresses of TSV structures during thermal cycling [5]. As a global measurement, the curvature change provides a measure of the average thermal stresses. The behavior can be correlated to the evolution of the Cu microstructure in the via when subjected to thermal processing, which was analyzed by focused ion beam (FIB) and electron backscatter diffraction (EBSD) techniques [6]. Based on the results from the microstructure analysis, the mechanisms underlying the linear and nonlinear temperature-curvature behavior of the TSV specimen are discussed. The local stress distribution near the Si surface around the Cu vias is important on device performance and interfacial reliability [7, 8]. This was measured by micro-Raman spectroscopy [9]. The stresses measured by Raman spectroscopy can in turn be correlated to that observed by the wafer curvature method through finite element analysis (FEA), taking into account the reference temperature, which was also based on the wafer curvature measurements. In the second part of this paper, the stress effects on interfacial reliability of TSV structures are discussed. It is found that plastic deformation is highly localized in the Cu vias but can be sufficient to cause via extrusion without interfacial delamination. Alternatively, via extrusion by interfacial delamination is simulated by a shear-lag cohesive zone model that predicts the critical temperatures and critical TSV dimensions.

PRECISION WAFER CURVATURE TECHNIQUE

The precision wafer curvature technique is an extension of the wafer curvature technique that has been used extensively for stress measurement in thin films and periodic line structures [10-12]. The measurement system is set up based on an optical lever with a capability to measure the curvature to a precision of $6.5 \times 10^{-5} \text{ m}^{-1}$. As shown schematically in Fig. 1a, the two incident laser beams are reflected by the specimen and the movement of the reflected laser spots is tracked by two position-sensitive photodetectors. The measurement system was designed with a heating stage inside a vacuum chamber. Therefore, the curvature change of the TSV specimen during thermal cycling can be measured *in situ* under a controlled atmosphere. More details of the system have been presented elsewhere [13].

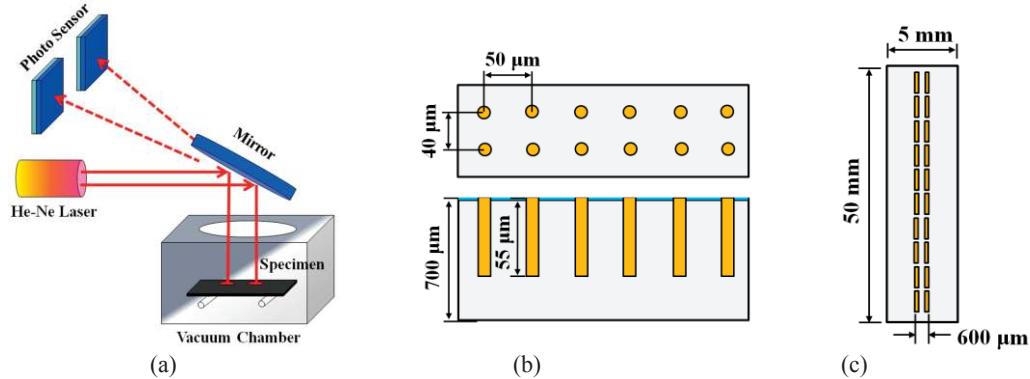


FIGURE 1. (a) Schematic of the precision wafer curvature measurement system. (b) Illustration of the TSV specimen, top and cross sectional views. (c) Top view of the TSV specimen for the curvature measurements, with TSV arrays in many blocks along the center line. Top view in (b) represents one block of arrays in (c).

The TSV structure used in the present study contains periodic arrays of blind Cu vias that are $10 \mu\text{m}$ in diameter with a nominal depth of $55 \mu\text{m}$. The silicon wafer is $700 \mu\text{m}$ thick and is of (001) type. The spacing between the TSVs is $40 \mu\text{m}$ along the $[110]$ direction and $50 \mu\text{m}$ along the $[1\bar{1}0]$ direction (Fig. 1b). For the curvature measurement, the wafer was cut into $5 \times 50 \text{ mm}$ beams where the TSVs were located along the centerline of the specimen (Fig. 1c). There was an oxide barrier layer of $0.4 \mu\text{m}$ thick at the via/Si interface and an oxide layer of $0.8 \mu\text{m}$ thick on the surface of the wafer. The surface oxide layer was mechanically removed for all measurements in this work.

The curvature measurements were conducted for several fully-filled TSV specimens subjected to different thermal cycling. To determine the residual stress in the Cu vias, a reference specimen was used by etching off the Cu vias. The curvature of the reference specimen was measured over the same thermal cycle as the specimen with fully filled Cu vias, and the curvature difference between the two specimens is attributed to the average thermal stress in the Cu vias. As shown in Fig. 2a, the curvature decreases nonlinearly with increasing temperature during the first cycle, suggesting an average compressive stress in the Cu vias and inelastic deformation. During cooling, however, the curvature changes linearly with the temperature, suggesting predominantly linear elastic deformation. In particular, the curvature difference between the two specimens becomes zero at around 100°C , suggesting a zero average stress in the Cu vias at this temperature. Below 100°C , the curvature becomes positive, and the average stress in the Cu vias becomes tensile. The temperature of zero curvature ($\sim 100^\circ\text{C}$) is taken as the reference temperature for subsequent thermal stress analysis.

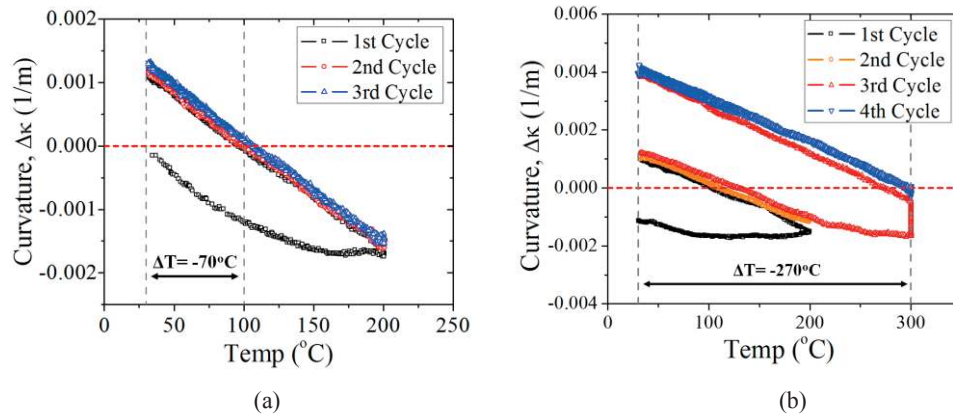


FIGURE 2. Curvature measurements for (a) a TSV specimen subjected to thermal cycling to 200°C; (b) a TSV specimen subjected to four thermal cycles with an annealing step at 300°C for 1 hour.

In the first measurement (Fig. 2a), the specimen went through three thermal cycles to 200°C at a heating rate of 2°C/min. After the first thermal cycle, the curvature-temperature relation became nearly linear and was reversible up to 200°C. The residual curvature at room temperature increased slightly after each cycle. In the second measurement (Fig. 2b), the specimen was heated to 200°C in the first two cycles, and then heated to 300°C during the third cycle and annealed for 1 hour prior to cooling, followed by an additional cycle to 300°C. For the first two cycles, the curvature behavior is similar to the first specimen. However, when the temperature was increased beyond 200°C during the third cycle, a nonlinear curvature-temperature behavior similar to the first cycle was observed from 200°C to 300°C. During annealing at 300°C, the curvature drops to almost zero. Evidently, the average stress in the Cu vias was relaxed considerably during annealing at 300°C. Subsequently, during cooling and the last thermal cycle, the curvature-temperature behavior again became nearly linear and reversible up to 300°C. Compared to Fig. 2a, the residual curvature in Fig. 2b is much larger after four thermal cycles, suggesting a higher tensile stress in the vias. This is attributed to the annealing process that reset the reference temperature to 300°C. Therefore, depending on the thermal history, different thermal load (ΔT) has to be used for the thermal stress analysis. In Fig. 2a, the reference temperature is 100°C, and the thermal load $\Delta T_A = -70^\circ\text{C}$ at the room temperature ($\sim 30^\circ\text{C}$). For Fig. 4b, the reference temperature becomes 300°C after the annealing step, and the thermal load $\Delta T_B = -270^\circ\text{C}$. The reference temperatures determined here were used in the finite element analyses to compare with micro-Raman measurements, as discussed in Section 4.

The measured curvature-temperature behavior can be related to the average thermal stresses and the deformation mechanisms of the TSV specimen. The negative curvature indicates an average compressive stress in the Cu vias, while the positive curvature implies tensile stress. The nonlinear curvature-temperature behavior observed during the heating process of the first cycle suggests inelastic deformation mechanisms, which was found to be related to the evolution of the Cu grain structures, as discussed in Section 3 along with microstructure analysis. On the other hand, the nearly linear curvature-temperature behavior in the subsequent thermal cycles indicates predominantly linear elastic behavior of the Cu vias, which is in sharp contrast with the thermomechanical behavior of Cu thin films [12].

MICROSTRUCTURE ANALYSIS

To further understand the deformation mechanisms underlying the measured curvature-temperature behavior of the TSV specimens, microstructure evolution of the Cu vias subjected to different thermal histories was studied [6]. A number of TSV specimens were each subjected to a single thermal cycle to different temperatures, and the measured curvatures are shown in Fig. 3. Despite the different cycling temperatures ranging from 100°C to 400°C, similar behavior was observed for all specimens: a nonlinear curvature-temperature relation during heating followed by a nearly linear relation during cooling.

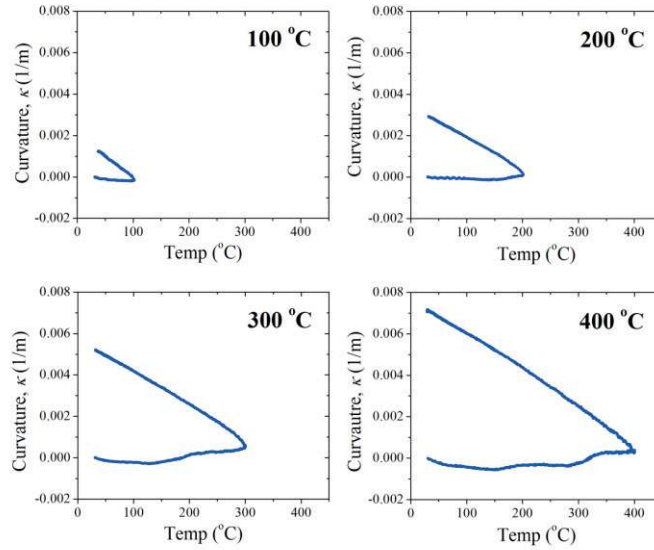


FIGURE 3. Curvature measurements for TSV specimens subject to thermal cycles with the highest temperature at 100°C, 200°C, 300°C, and 400°C.

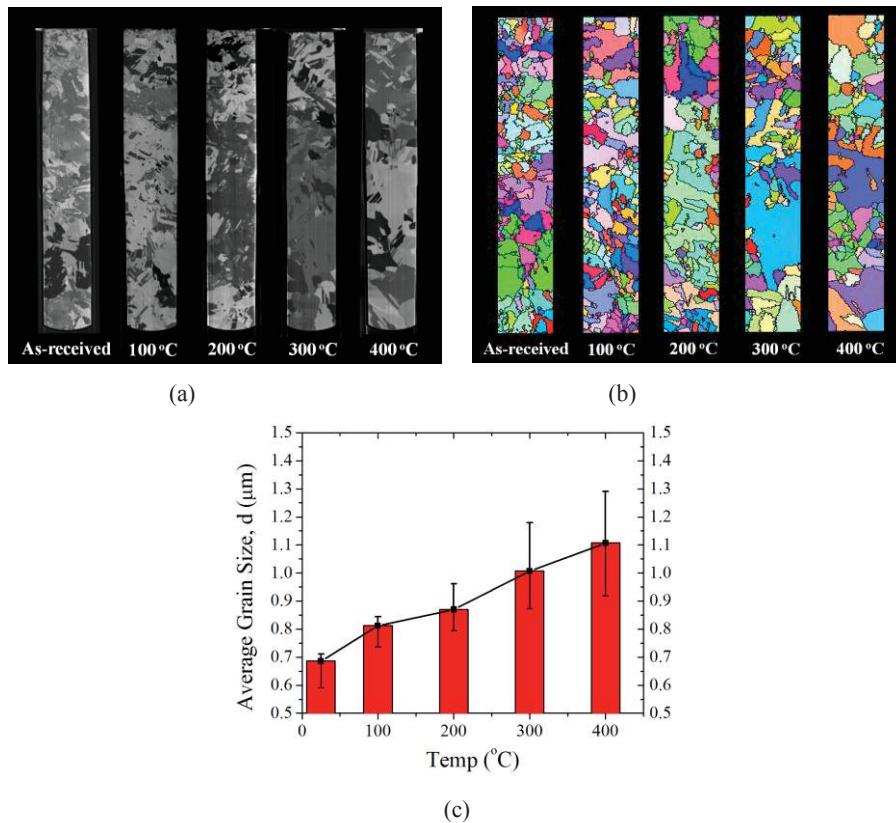


FIGURE 4. (a) Focused ion beam images of TSVs after different thermal loads. (b) Grain mapping by EBSD. (c) Average grain sizes.

Using focused ion beam (FIB), the cross-sections of the TSV specimens were examined after completing the thermal cycling measurements. The contrast of the ion channeling images of the Cu vias in Fig. 4a shows that the average Cu grain sizes are larger after thermal cycles and increase as the high end of the thermal cycling temperature increases, suggesting possible grain growth during the thermal cycles. This is confirmed by electron backscatter

diffraction (EBSD) analysis of the grain structures. The EBSD grain mappings for the Cu vias are shown in Fig. 4b together with the average grain sizes measured and compared in Fig. 4c. Evidently, systematic grain growth has occurred in the Cu vias after each thermal cycle. The average grain size for the via in the as-received TSV specimen is $0.69\ \mu\text{m}$. After thermal cycling to 100, 200, 300, and 400°C , the average grain sizes have grown by 18.4%, 26.8%, 46.8%, and 61.4%, to 0.81, 0.87, 1.00, and $1.11\ \mu\text{m}$, respectively.

With the EBSD technique, the grain orientation of the Cu vias was quantitatively measured. In Fig. 5, the inverse pole figures of the grain orientations are plotted for the TSVs along the directions normal to the TSV length (ND) and parallel to the TSV length (RD). Overall, there appears to be no preferred Cu grain orientation in all the specimens before and after thermal cycling. The lack of preferred grain orientation indicates a statistically isotropic grain structure in the Cu vias, and thus the thermomechanical properties of the Cu can be treated as isotropic in the thermal stress analysis. In addition, the misorientation across grain boundaries obtained from the EBSD measurements is plotted in Fig. 6. There exist a large number of twin boundaries with a characteristic misorientation angle of 60° across the grain boundaries for all the vias examined. The presence of twin boundaries may lead to relatively high yield strength of the Cu vias.

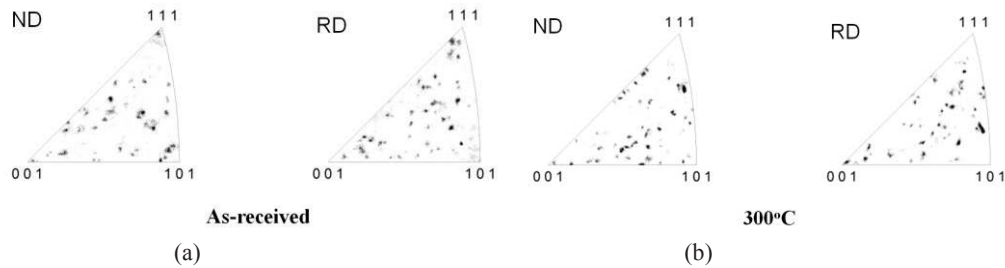


FIGURE 5. Inverse pole figures of (a) as-received TSV and (b) TSV after thermal cycling to 300°C . Two measurement directions were defined: ND (normal to the TSV axis) and RD (parallel to the TSV axis).

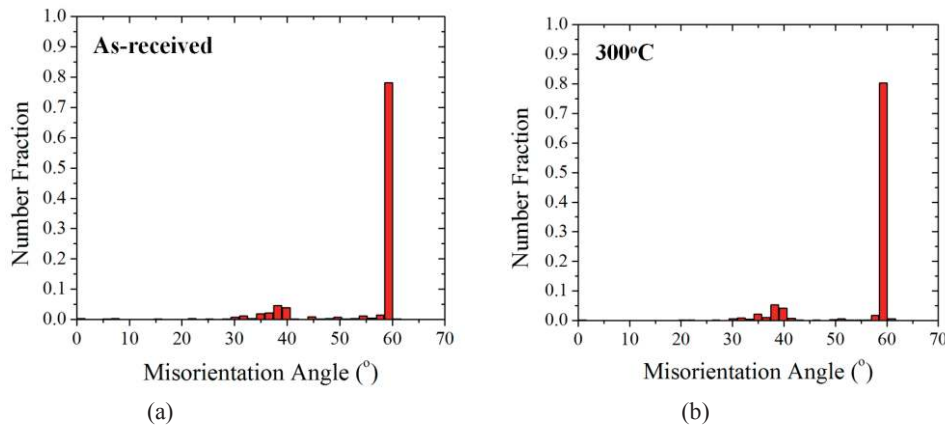


FIGURE 6. Grain misorientation angles obtained by EBSD for (a) as-received TSV and (b) TSV after thermal cycling to 300°C .

Based on the microstructure analysis, the curvature-temperature behavior of the fully-filled TSV specimen can be understood as the following. The nonlinear curvature-temperature relation during heating of the first cycle is mainly attributed to the nonlinear stress relaxation caused by grain growth. Similar curvature behavior due to grain growth has been observed for Cu thin films [14,15]. As grain growth proceeds to eliminate grain boundaries and reduce the excess volume, it is favored when the average stress in the Cu vias is compressive during heating [16]. The nearly linear curvature-temperature behavior during cooling and subsequent cycles suggests stabilized grain structures in the Cu vias. The grain structures would remain stabilized as long as the temperature does not exceed the highest temperature that the TSV specimen has experienced in any of the previous cycles. When the temperature increased beyond the highest temperature in the previous cycles, the grain structures would evolve further with additional grain growth and stress relaxation. Furthermore, the annealing process in Fig. 2b shows continual stress relaxation at the high temperature. In general, grain growth is a kinetic process that depends on both temperature and stress.

MICRO-RAMAN SPECTROSCOPY

For the TSV structure, the thermal stresses in Cu can in turn induce stresses in the Si matrix surrounding the TSVs where the stress distribution near the wafer surface is particularly important since most of the active devices are located near the surface. To measure the near surface stresses in Si, the micro-Raman spectroscopy technique was used [9]. Raman spectroscopy relies on the inelastic scattering (or Raman scattering) of Si, where the frequency shift of the Raman modes provides a measure of the stress in Si. The theory of Raman measurement and its application for TSV structures have been developed previously [17]. Under the [001] backscattering configuration, only the longitudinal Raman mode can be detected. Assuming a biaxial stress state near the wafer surface, the following relation can be deduced from the secular equation for (001) Si [18],

$$\sigma_r + \sigma_\theta \text{ (MPa)} = -470\Delta\omega_3 \text{ (cm}^{-1}\text{)}, \quad (1)$$

where $\sigma_r + \sigma_\theta$ is the sum of the in-plane normal stresses, and $\Delta\omega_3 = \omega_3 - \omega_0$ is the Raman frequency shift of the longitudinal Raman mode. With Eq. (1), the stress sum near the wafer surface can be determined from the measurement of $\Delta\omega_3$.

In this study, Raman measurements were carried out with a commercial micro-Raman Spectrometer equipped with a 442 nm Ar laser. Two TSV specimens were subjected to similar thermal treatment as those in the wafer curvature experiments (Fig. 2). Specimen A was heated to 200°C and then immediately cooled down to room temperature (RT), and specimen B was heated to 300°C and annealed for 1 hour prior to cooling down. For both specimens, the Raman measurements were conducted at RT by scanning across two neighboring vias along the [110] direction. To deduce the frequency shift $\Delta\omega_3$, a reference Raman frequency ω_0 is required, which was determined by extending the measurement to areas far away from the TSVs where the stress is assumed to be zero. With the calibrated reference frequency ω_0 , the sum of the two principal stresses in Si is deduced from the measured Raman frequency using Eq. (1).

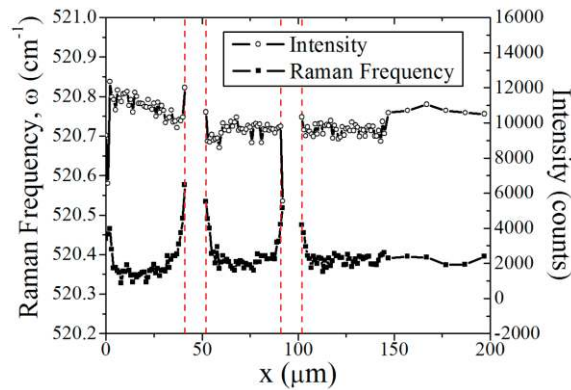


FIGURE 7. Raman intensity (open symbols) and frequency (filled symbols) of a TSV specimen. Dashed lines indicate the Cu/Si interfaces.

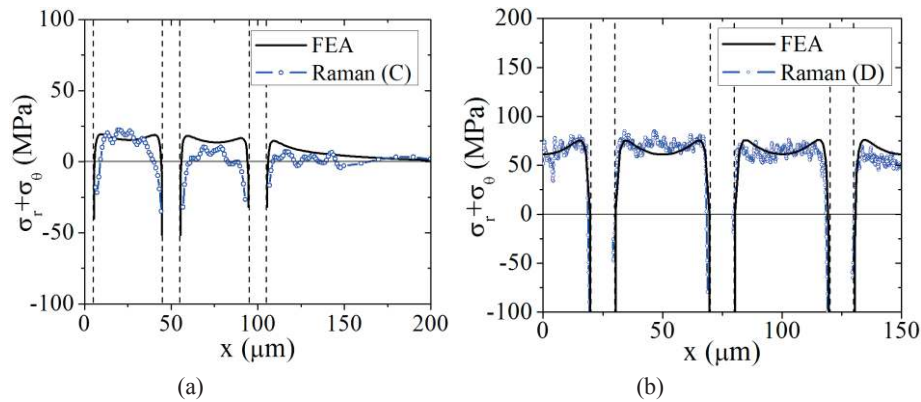


FIGURE 8. Comparison of the near-surface stress distribution between Raman measurements and FEA: (a) Specimen A; (b) Specimen B.

The measured Raman intensity and frequency shift obtained from specimen A are shown in Fig. 7, representing typical results obtained from Raman measurements. A sudden drop of the Raman intensity was observed near the Cu/Si interface. The distributions of the stress sums deduced from the Raman measurements are plotted in Fig. 8 for both specimens. Clearly, a sub-micron resolution was achieved in the measurement, but the results provided only the sum of the two individual stress components in Si. Further understanding of the stress characteristics in the TSV structure requires detailed stress analysis to delineate the stress components and correlate the micro-Raman measurements with the thermal cycling experiments [6, 9].

A three-dimensional finite element model was constructed using the commercial package, ABAQUS (v6.10). A quarter of the via with symmetric boundary conditions in the $[110]$ and $[\bar{1}\bar{1}0]$ directions was modeled to simulate the periodic TSV array used in the Raman measurement. The anisotropy of Si was taken into consideration by using the anisotropic elastic constants for Si, and Cu is treated as isotropic based on the microstructure analysis by EBSD. The following material properties were used for Cu and SiO₂: Young's modulus, $E_{\text{Cu}} = 110$ GPa and $E_{\text{oxide}} = 70$ GPa; Poisson's ratio, $\nu_{\text{Cu}} = 0.35$ and $\nu_{\text{oxide}} = 0.16$. The CTEs are $\alpha_{\text{Cu}} = 17$ ppm/°C, $\alpha_{\text{Si}} = 2.3$ ppm/°C and $\alpha_{\text{oxide}} = 0.55$ ppm/°C. Since the Raman signal penetrates up to 0.2 μm from the wafer surface, the stress components are extracted from 0.2 μm below the wafer surface. The sums of the in-plane stresses obtained by FEA for specimens A and B are calculated and compared with the Raman measurements. The thermal loads for the two specimens were chosen to be the same as those in the curvature measurements (Fig. 2) to facilitate the correlation of the results from the two techniques. Based on the curvature measurements, the reference temperature for specimen A is taken to be 100°C, and that for specimen B is 300°C, corresponding to thermal loads of $\Delta T_{\text{A}} = -70^\circ\text{C}$ and $\Delta T_{\text{B}} = -270^\circ\text{C}$, relative to the room temperature of 30°C. As shown in Fig. 8, the FEA results are in reasonable agreements with the Raman measurements. Moving away from the Cu/Si interface, the sum of the stresses first increases sharply, and then gradually decreases. Between the two adjacent vias, the stress depends on the pitch distance as a result of the stress interaction. The measurement for specimen B (Fig. 8b) shows a higher stress level in Si than for specimen A, as a result of the higher negative thermal load ($|\Delta T_{\text{B}}| > |\Delta T_{\text{A}}|$). Therefore, the stresses in Si around the TSVs depend on the thermal processes of the specimen.

INTERFACIAL RELIABILITY

Effect of Cu Plasticity on Via Extrusion

After thermal cycling, via extrusion was observed in the TSV specimen (Fig. 9a). A previous study has suggested that via extrusion could be caused by interfacial delamination [19]. However, in the present study, no evidence of interfacial delamination was observed. Instead, via extrusion appears to have occurred as a result of localized plastic deformation near the via/Si interface during thermal cycling. An elastic-plastic FEA model was constructed to investigate the effect of Cu plasticity on via extrusion. In general, the plastic deformation in the Cu TSVs depends on the thermal load and the yield strength of Cu. For the present study, the yield strength of Cu was assumed to be 300 MPa and a thermal load of $\Delta T = 270^\circ\text{C}$ was applied. In Fig. 9b, the deformed shape by the FEA model clearly showed extrusion of the via, similar to what was observed in our experiments. It is noted that plastic deformation in the Cu via is highly localized, as shown in Fig. 9c, where the equivalent plastic strain in Cu is non-zero only in a small region near the top of the via. The plastic yielding of Cu near the interface effectively relaxes the constraint of the surrounding materials and allows the via extrusion without interfacial delamination. Moreover, the local plasticity in Cu could also enhance the total fracture energy for interfacial delamination [20] and thus help prevent delamination.

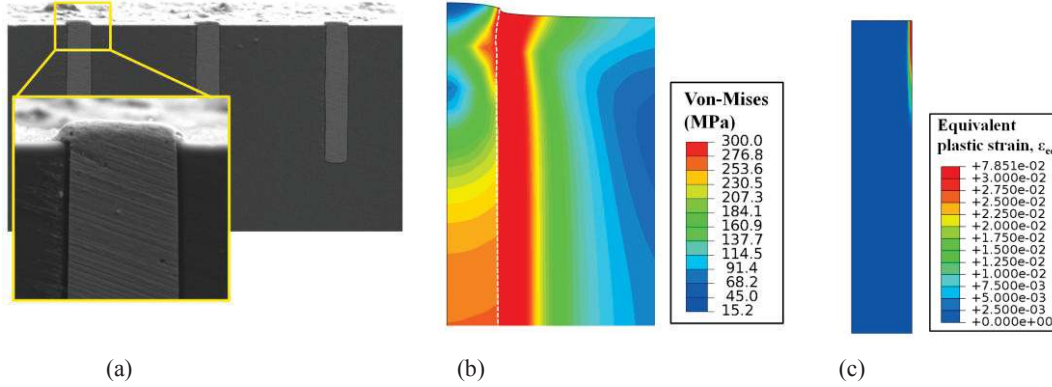


FIGURE 9. (a) SEM image of TSV extrusion observed after thermal cycling. (b) Stress distribution and deformation of TSV by an elastic-plastic FEA model. (c) Equivalent plastic strain in the TSV by FEA (yield strength = 300 MPa, $\Delta T = 270^\circ\text{C}$).

Via Extrusion by Interfacial Delamination

An alternative mechanism for via extrusion is due to interfacial delamination as observed in some studies [21]. To predict the critical condition for initiation of interfacial delamination, a cohesive zone model was adopted [22]. Using a bilinear traction-separation law for the interface, the interface first undergoes elastic deformation until the combination of the opening stress (mode I) and shear stress (mode II) reaches a critical level, which depends on the cohesive strength of the interface. Subsequently, the interface is partly damaged and weakened upon further loading. A delamination crack is nucleated when a critical separation (both opening and shearing) is reached, which depends on the fracture toughness of the interface. Therefore, two critical conditions can be determined, one for damage initiation and the other for crack nucleation. For the TSV structure subject to a positive thermal load ($\Delta T > 0$), the interfacial delamination is predominantly mode II (shearing), which can be analyzed by a shear-lag model [22]. For given material properties and via dimensions, two critical temperatures are predicted. For damage initiation, the critical temperature is

$$\Delta T_{c1} = \frac{2}{(\alpha_{TSV} - \alpha_{Si})} \sqrt{\frac{\tau_i \delta_i}{E_{TSV} D}} \coth\left(\frac{H}{\lambda}\right) \quad (2)$$

where $\lambda = \sqrt{\frac{E_{TSV} D \delta_i}{\tau_i}}$ is a characteristic length scale, τ_i is the shear strength of the interface, δ_i is the critical

separation, E_{TSV} is Young's modulus of the via material, D is via diameter, H is via height, α_{TSV} and α_{Si} are the coefficients of thermal expansion. For crack nucleation, the critical temperature is

$$\Delta T_{c2} = \frac{2}{(\alpha_{TSV} - \alpha_{Si})} \sqrt{\frac{2\Gamma_i}{E_{TSV} D}} \quad (3)$$

where Γ_i is the fracture toughness of the interface.

As an example, we plot in Fig. 10 the two critical temperatures versus the via diameter, taking the following material properties: $E_{TSV} = 110$ GPa, $\alpha_{TSV} - \alpha_{Si} = 14.7$ ppm/ $^\circ\text{C}$, $\Gamma_i = 10.0$ J/m², $\tau_i = 300$ MPa, and $\delta_i = 20$ nm. When the thermal load (ΔT) is specified for TSV processes, the critical via diameters can be determined. In general, vias with larger diameters are more prone to interfacial delamination and hence via extrusion. The model prediction agrees qualitatively with the experiments where via extrusion was observed for via diameters greater than a critical value [21], while the dependence on the via height is much weaker.

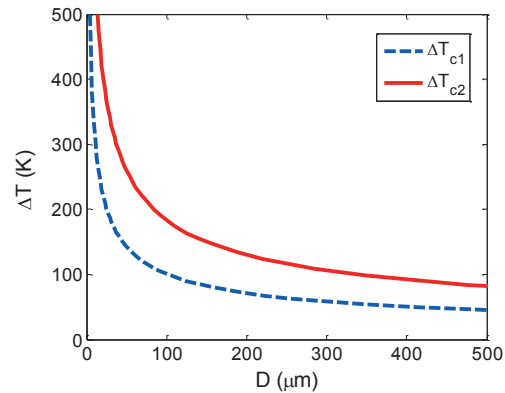


FIGURE 10. Critical temperatures predicted by the shear-lag cohesive zone model.

SUMMARY

This paper presents thermomechanical characterization of TSV structures by combining the precision wafer curvature technique in thermal cycling experiments with micro-Raman spectroscopy. The evolution of the Cu microstructure in the vias was analyzed by focused ion beam (FIB) and electron backscatter diffraction (EBSD) techniques, which provided insights into the underlying mechanisms for elastic and inelastic deformation in the TSV structures. Via extrusion was observed after thermal cycles, which may be due to local plastic deformation or interfacial delamination. Finite element analysis showed that plastic deformation is highly localized near the via/Si interface, which could be sufficient to cause via extrusion without interfacial delamination. Alternatively, a shear-lag cohesive zone model was developed to predict the critical temperatures for interfacial damage initiation and crack nucleation towards delamination.

ACKNOWLEDGMENTS

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REFERENCES

1. N. Ranganathan, K. Prasad, N. Balasubramanian, and K. L. Pey, *J. Micromech. Microeng.* 18, 075018 (2008).
2. C.S. Selvanayagam, J.H. Lau, X.Zhang, S. Seah, K. Vaidyanathan, and T.C. Chai, *IEEE Trans. Advanced Packaging* 32, 720-728 (2009).
3. A. P. Karmarker, X. Xu, and V. Moroz, *Proc. IEEE 47th Int. Reliab. Phys. Symp.* (Montreal, Canada), pp. 682–687 (2009).
4. K.H. Lu, X.F. Zhang, S.K. Ryu, J. Im, R. Huang, and P.S. Ho, *Proc. IEEE 59th ECTC* (San Diego, CA), pp. 630–634 (2009).
5. S.K. Ryu, T. Jiang, K.H. Lu, J. Im, H.-Y. Son, K.-Y. Byun, R. Huang, and P.S. Ho, *Appl. Phys. Lett.* 100, 041901 (2012).
6. T. Jiang, S.K. Ryu, Q. Zhao, J. Im, R. Huang and P.S. Ho, *Microelectronics Reliability*, 53, pp. 53-62 (2013).
7. S.K. Ryu, K.H. Lu, X. Zhang, J.H. Im, P.S. Ho and R. Huang, *IEEE Trans. Device and Materials Reliability* 11, 35-43 (2011).
8. S.K. Ryu, K.H. Lu, T. Jiang, J. Im, R. Huang, and P.S. Ho, *IEEE Trans. Device and Materials Reliability* 12, 255-262 (2012).
9. S.K. Ryu, Q. Zhao, M. Hecker, H.-Y. Son, K.-Y. Byun, J. Im, P.S. Ho, and R. Huang, *J. Appl. Phys.* 111, 063513 (2012).
10. R.P. Vinci, E.M. Zielinski and J.C. Bravman, *Thin Solid Films* 262, 142-153 (1995).
11. I.-S. Yeo, P.S. Ho, and S.G.H. Anderson, *J. Appl. Phys.* 78, 945 (1995).
12. D. Gan, P.S. Ho, R. Huang, J. Leu, J. Maiz and T. Scherban, *J. Appl. Phys.* 97, 103531 (2005).
13. I.-S. Yeo, *Thermal stresses and stress relaxation in Al-based metallization for ULSI interconnects*, Ph.D. thesis, University of Texas at Austin, 1996.
14. D. C. Miller, C. F. Herrmann, H. J. Maier, S. M. George, C. R. Stoldt and K. Gall, *Thin Solid Films* 515, 3208-3223 (2007).
15. J.M.E. Harper, C. Cabral, P.C. Andricacos, L. Gignac, I.C. Noyan, K.P. Rodbell, and C.K. Hu, *J. Appl. Phys.* 86, 2516-2525 (1999).

16. P. Chaudhari, *J. Vac. Sci. Tech.*, 9, 520-522 (1972).
17. I. De Wolf, H. E. Maes, and S. K. Jones, *J. Appl. Phys.* 79, 7148-7156 (1996).
18. M. Hecker, L. Zhu, C. Georgi, I. Zienert, J. Rinderknecht, H. Geisler, and E. Zschech, *AIP Conf. Proc.* 931, pp. 435-444 (2007).
19. S.K. Ryu, K. Lu, J. Im, R. Huang and P.S. Ho, *AIP Conf. Proc.* 1378, pp. 153-167 (2011).
20. M. Lane, R.H. Dauskardt, A. Vainchtein, and H.J. Gao, *J. Mater. Res.* 15, 2758-2769 (2000).
21. S. Cho, RTI 3D Workshop (Burlingame, CA), December 2010.
22. S.K. Ryu, *Thermomechanical Stress Analysis and Interfacial Reliability for Through-Silicon Vias in Three-Dimensional Interconnect Structures*. PhD dissertation, University of Texas at Austin, 2011.