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DOI: 10.1038/s41467-018-03436-0

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# Thickness-modulated metal-to-semiconductor transformation in a transition metal dichalcogenide

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The possibility of tailoring physical properties by changing the number of layers in van der Waals crystals is one of the driving forces behind the emergence of two-dimensional materials. One example is bulk MoS<sub>2</sub>, which changes from an indirect gap semiconductor to a direct bandgap semiconductor in the monolayer form. Here, we show a much bigger tuning range with a complete switching from a metal to a semiconductor in atomically thin PtSe<sub>2</sub> as its thickness is reduced. Crystals with a thickness of ~13 nm show metallic behavior with a contact resistance as low as 70 Ω·μm. As they are thinned down to 2.5 nm and below, we observe semiconducting behavior. In such thin crystals, we demonstrate ambipolar transport with a bandgap smaller than 2.2 eV and an on/off ratio of ~10<sup>5</sup>. Our results demonstrate that PtSe<sub>2</sub> possesses an unusual behavior among 2D materials, enabling novel applications in nano and optoelectronics.

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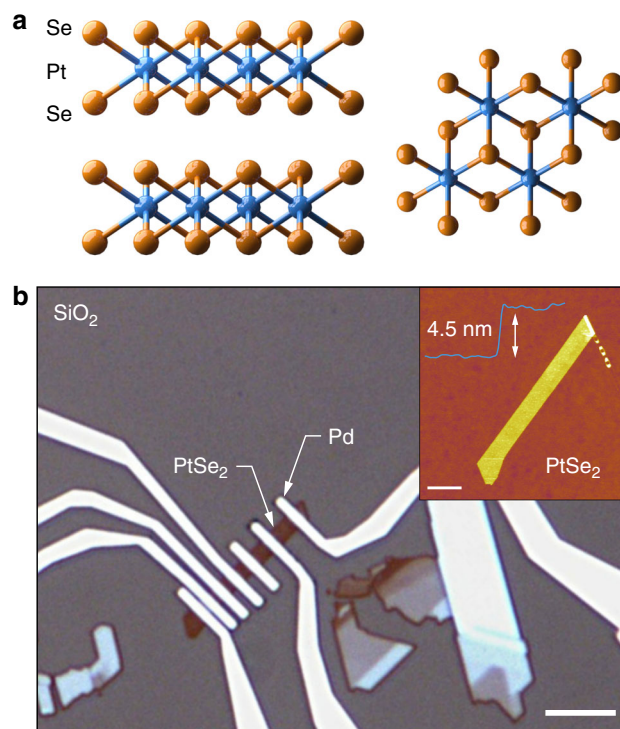
Two-dimensional crystalline materials such as graphene, transition metal dichalcogenides (TMDCs), and black phosphorus (BP) have attracted considerable attention in recent years, due to a set of properties that make them relevant for both fundamental science and technological applications<sup>1–3</sup>. Due to the interaction between atomic layers, these materials exhibit dramatically different properties compared to their bulk forms<sup>4–9</sup>. While the field was opened with the discovery of graphene<sup>10</sup>, the presence of a bandgap in TMDCs has made this class of materials appealing for applications in electronics<sup>11</sup>. A key enabler in the development of two-dimensional electronics is the ability to control the properties of the constituent materials, in order to modulate or complement their natural characteristics. Among these, the bandgap is a crucial one, governing both optical and transport properties. For example, a configurable bandgap can be used to tune the adsorption spectrum to specific wavelengths<sup>12</sup>, while the bandgap is also an important factor determining the on-state current and on/off ratio in field-effect devices. Due to their atomic scale thickness, van der Waals materials are susceptible to several methods of bandgap modulation, involving strain, pressure, chemical or substitutional doping, and application of electrical fields<sup>13–22</sup>. However, it is difficult to implement most of these methods in devices without increasing their complexity. A stable and simple approach to bandgap engineering of van der Waals materials involves merely changing the number of layers in the crystal. Apart from exfoliation, this method could be exploited on a large scale by engineering the growth process or by selectively thinning the material after deposition. For example, in the case of MoS<sub>2</sub> the 1.29 eV indirect bandgap in bulk form becomes a direct bandgap with a 1.8 eV optical resonance in monolayers<sup>4–7</sup>. Even more striking is the case of BP, where the bandgap modulation ranges from 0.35 eV in bulk to 1.73 eV in a monolayer<sup>23–25</sup>. However, in these systems we do not see a fundamental change of their semiconducting nature; we only see a change in the magnitude and type (direct vs. indirect) of the bandgap.

A much wider, qualitative change in the nature of electrical conductivity would extend the reach of two-dimensional materials further. It would, for example, allow the same material to be used both as an interconnect and as the semiconducting channel, greatly simplifying the realization of electronic circuits based on two-dimensional materials, as already proposed for PdS<sub>2</sub> and hydrogenated graphene<sup>26,27</sup>. One material that could offer this is PtSe<sub>2</sub>, a group VIIIc transition metal dichalcogenide. It shares the same layered structure with other MX<sub>2</sub> compounds, with each layer of the crystal made of a two-dimensional close-packed array of Pt atoms sandwiched between Se atoms in a 1T structure<sup>28</sup>. The electronic properties of bulk PtSe<sub>2</sub> have been controversial, with experiments suggesting both a semiconductor<sup>29</sup> and a semimetal<sup>30,31</sup>. More recently, it has been shown that in its bulk form PtSe<sub>2</sub> is expected to be a semimetal<sup>28,32</sup>, with the opening of a bandgap in monolayers<sup>33–35</sup>. Recent studies have also shown that this material can be grown, and that it exhibits appreciable transport properties and interesting spin physics, motivating further studies of its transport properties<sup>34,36,37</sup>.

Here, we fabricate electronic devices based on PtSe<sub>2</sub> and study electrical transport properties of crystals ranging in thickness from 14 to 2 nm. They show a transition from a metal to a semiconductor for thicknesses lower than 2.5 nm. Metallic samples show low contact resistance, while in semiconducting samples we observe ambipolar transport and estimate the size of the bandgap by employing electric-double-layer transistors (EDLTs).

## Results

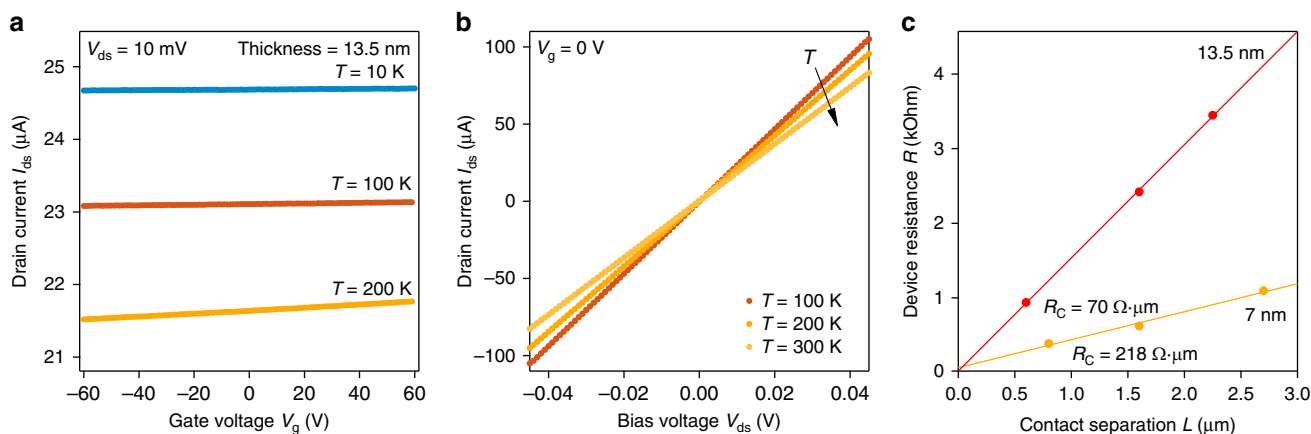
**Device characterization.** Ultrathin PtSe<sub>2</sub> crystals with 1T-phase (Fig. 1a) were obtained by mechanical exfoliation on doped Si



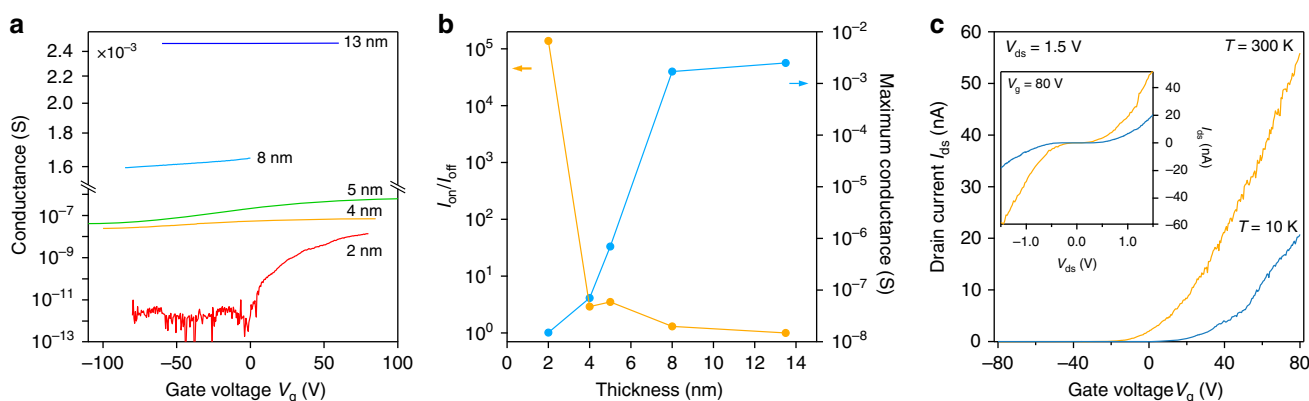
**Fig. 1** PtSe<sub>2</sub> structure and devices. **a** PtSe<sub>2</sub> layered crystal structure showing two layers from side and top view. **b** Example of PtSe<sub>2</sub> crystal before (inset, AFM image, scale bar is 2 μm) and after evaporation of Pd contacts (optical image). Scale bar is 5 μm

wafers covered with 270 nm of SiO<sub>2</sub>. AFM imaging was used to precisely measure the thickness of the resulting crystals, followed by evaporation of Pd contacts to obtain back-gated devices such as the one shown in Fig. 1b. Depending on the crystal size and geometry, simple two-terminal devices, as well as devices with variable electrode spacing needed for contact resistance determination using the transfer length method were prepared. Transfer characteristics of the devices were measured in vacuum at different temperatures between 300 and 10 K (see methods). We first discuss the case of the thickest sample (13.5 nm) we characterized, which is representative of our observations for samples thicker than 7 nm. As expected from theoretical predictions of bulk PtSe<sub>2</sub> being a semimetal, the device shows a metallic behavior with almost negligible n-type current modulation by the back gate ( $dI_{ds}/dV_g \sim 10^{-10}$  S) and a perfectly linear bias ( $I_{ds} - V_{ds}$ ) dependence, as shown in Fig. 2a, b. We calculate a sheet resistance of 400 Ω/sq at 10 K, which increases with temperature. Using the transfer length method, we extract a contact resistance as low as 70 Ω·μm at 10 K (Fig. 2c), significantly lower than the lowest reported numbers for semiconducting TMDCs with phase-engineered<sup>38</sup> or degenerately doped<sup>39</sup> contacts, indicating that the metallic PtSe<sub>2</sub> could be an interesting material for realizing contacts to two-dimensional semiconductors<sup>40</sup>.

We now turn our attention to crystals thinner than 7 nm, measuring the conductance as a function of the back-gate voltage. In Fig. 3a, we present a summary of the conductance dependence on the back-gate voltage  $V_g$  measured at 10 K for devices with different thicknesses of PtSe<sub>2</sub>. Starting with an almost gate-independent conductance in bulk samples, indicating efficient screening of the gate voltage by the high density of charge carriers in the metallic sample, in samples with a thickness of 5 nm we clearly start to observe a significant non-linear modulation with the presence of a well-developed off-state and n-type conduction in the thinnest sample we measured (2 nm). This change in



**Fig. 2** Electrical transport characterization of 13.5 nm thick PtSe<sub>2</sub>. **a** Gating characteristics showing weak current modulation at different temperatures. **b**  $I_{ds} - V_{ds}$  curves acquired at different temperatures. **c** Contact resistance extraction using the transfer length method for the 13.5 and 7 nm thick devices



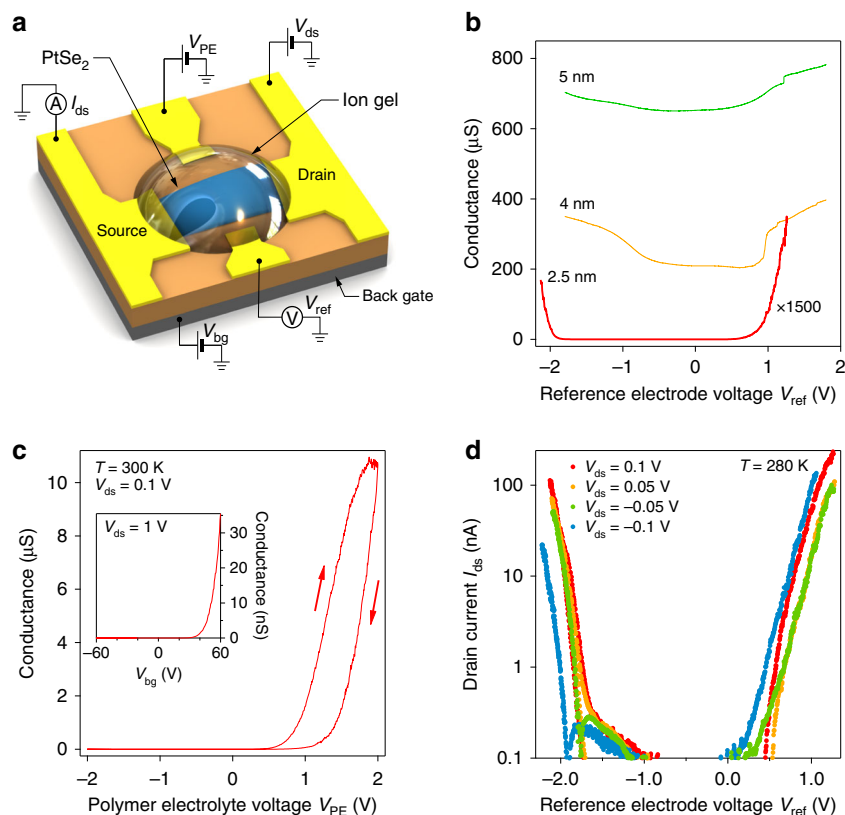
**Fig. 3** Thickness modulation of transport in PtSe<sub>2</sub>. **a** Conductance modulation as a function of gate voltage for different sample thicknesses. **b** Maximum conductance and on/off ratio as a function of sample thickness at 10 K. **c**  $I_{ds} - V_g$  curves recorded for the 2 nm thick device, showing n-type semiconducting behavior. Inset:  $I_{ds} - V_{ds}$  curves recorded for the same device

electrical transport properties is consistent with the presence of a finite number of states around the Fermi level in bulk PtSe<sub>2</sub>, which has been predicted by calculations<sup>28,34,35</sup>. The shrinking density of states with decreasing thickness results in a greater tunability of the conductance with the gate, up to the point where an appreciable bandgap is opened. This transition is summarized in Fig. 3b, where we observe a progressive decrease of the maximal conductance by more than five orders of magnitude compared to our thickest sample, from 2.5 to 15 nS in 2-nm-thick samples. This is accompanied by an increase in the relative current modulation that can be obtained, from  $\approx 1$  for the 13.5 nm thick sample to  $\approx 10^5$  (2 nm). The semiconducting behavior in the 2-nm-thick sample can be more clearly seen in Fig. 3c. We measure the modulation of the drain current  $I_{ds}$  as a function of back-gate voltage  $V_g$ . The device turns off even at room temperature, while the conductivity increases with the temperature (Fig. 3c, inset), as expected from a semiconductor. We have also made devices based on monolayer PtSe<sub>2</sub> (see Supplementary Fig. 1), for which no conduction could be detected. This follows the observed trend of the reduction of conductivity with reduced thickness, making few layers the optimal thickness range for transistor-based applications, where a compromise between the high on-state current and on/off ratio are required.

**PtSe<sub>2</sub> EDLT characterization and bandgap measurement.** To gain further insight into the behavior of PtSe<sub>2</sub>, we fabricate EDLTs

based on the ([EMIM]-[TFSI]) ion gel<sup>41,42</sup> and PtSe<sub>2</sub> crystals of different thicknesses, with the device schematic shown in Fig. 4a. Because of the higher gate capacitance<sup>41</sup>, this approach allows us to explore electrical transport in a wider range of electrostatically induced doping, while in the same time we also benefit from a reduced barrier for charge injection at the contacts<sup>12</sup>. Figure 4b shows the conductance as a function of polymer electrolyte gate voltage for PtSe<sub>2</sub> crystals in the 2.5–5 nm thickness range. In agreement with our observations on back-gated devices, the 4 and 5 nm thick samples show three orders of magnitude higher conductivity compared to the thinnest one, but a relative modulation of less than 50%. Together with the absence of an off-state in thicker crystals (also see Supplementary Fig. 2), we now observe that the modulation is indeed ambipolar. The presence of both electron and hole conduction branches allows us to rule out that the high conductivity we observe in thick PtSe<sub>2</sub> is due to intrinsic doping.

We move to the characterization of the 2.5-nm-thick PtSe<sub>2</sub> crystal, which was used to realize a two-terminal device. The inset of Fig. 4c shows the room-temperature conductance as a function of back-gate voltage before coating the device with the ion gel. Applying a drain-source bias of 0.1 V, we observe a threshold voltage of 1.5 V on the n-side for the PE gate, and can reach on-state conductance exceeding 10  $\mu$ S. The on/off ratio is higher than  $10^5$ , and we estimate FE mobility around  $3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ . For comparison (Fig. 4c, inset), the back-gated operation resulted in an on-state conductance of 36 nS, threshold voltage of 48 V, and a maximum relative modulation around  $10^4$ .



**Fig. 4** Devices with ion-gel dielectrics. **a** Device schematic. **b** Conductance as a function of electrostatically induced doping. **c** Device conductance for the device with 2.5 nm thick PtSe<sub>2</sub> as a function of polyelectrolyte gate voltage  $V_{PE}$  at 300 K. **d**  $I_{ds} - V_{ref}$  dependence for the device with 2.5 nm thick PtSe<sub>2</sub>

Since we already observe the presence of a bandgap in the sample, we subsequently cool it down to 280 K to be able to apply a higher gate voltage, thanks to the wider electrochemical window of the polymer electrolyte<sup>12</sup>. We assume the electrolyte capacitance at this temperature to be  $\sim 4 \mu\text{F}/\text{cm}^2$ , from previous reports<sup>41</sup>. As can be seen from Fig. 4d, the device shows clear ambipolar behavior, with an on/off ratio around  $10^5$  and subthreshold swings (SS) of 83 and 106 mV/dec for holes and electrons, respectively.

The large electrostatic capacitance in ionic and polymer electrolyte-gated FETs allows us to determine the bandgap<sup>43–48</sup> of PtSe<sub>2</sub> in the semiconducting thickness range. The prerequisite for this is ambipolar operation. The value of the bandgap can then be extracted from the difference between the threshold voltages for electron and hole branches  $\Delta V_{th} = |V_{th}^e - V_{th}^h|$ . Using a reference electrode to provide an accurate reading of the voltage drop across the gel  $V_{ref}$  (see methods), the energy  $e\Delta V_{th}$  is in an ideal case, equal to the energy needed to add an electron to the bottom of the conduction band and to create a hole at the top of the valence band. To apply this technique, we sweep the gate voltage at different source-drain bias levels and extrapolate from a linear fit the two threshold voltages at zero bias for better precision (see Supplementary Fig. 3). We obtain  $V_{th}^e = 0.4 \text{ V}$ ,  $V_{th}^h = -1.8 \text{ V}$ , which gives a bandgap value of  $E_G = 2.2 \pm 0.1 \text{ eV}$  (where the error is estimated from the fit at different  $V_{ds}$ ).

Theoretical calculations of the PtSe<sub>2</sub> band structure predict the bandgap of monolayers to be between 1.2 and 2.1 eV<sup>34,35</sup> with a significant reduction in bilayers. No calculations for larger thicknesses are available at this time. Interestingly, even if our sample is definitely thicker than a bilayer, it still shows a sizeable bandgap allowing efficient current modulation at room temperature. This difference between the theoretical calculations and our results for the 2.5-nm-thick PtSe<sub>2</sub> could be explained by a possible

underestimation of the bandgap in DFT calculations. Our samples could also be covered by a disordered “dead layer”, implying that the actual thickness of the active channel is lower than the one inferred by AFM measurements. These points require further future investigation. We would finally like to note that our measured value represents the upper limit for the actual bandgap, since it has been shown that all non-idealities in the EDLT operation such as trap states (see Supplementary Fig. 4) or contact resistance<sup>46</sup> can lead to an overestimated bandgap. However, our measurements show that a significant bandgap is already present in few-layer PtSe<sub>2</sub>.

## Discussion

Our results on PtSe<sub>2</sub> highlight a new type of behavior in an atomic scale TMDC material, with room temperature electrical transport characteristics which can be tuned from metallic to semiconducting, allowing both high electrical conductivity and efficient transistor operation to be realized in the same material. By implementing ohmic contacts and boron nitride encapsulation, it would be further possible to access the pristine properties of this material<sup>49</sup>, where theory predicts mobility of up to  $\sim 1890 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$  at room temperature<sup>50</sup>. Considering the air-stable nature of PtSe<sub>2</sub> even in the monolayer limit (see Supplementary Fig. 1), these observations open new possibilities for the facile realization of atomic scale circuitry based on thickness-modulated TMDCs.

## Methods

**Device fabrication.** PtSe<sub>2</sub> crystals were obtained by mechanical exfoliation from bulk crystals (HQ Graphene) onto a doped Si substrate with 270 nm of SiO<sub>2</sub>. The substrate was imaged using an optical microscope (Olympus BX51M) equipped with a color camera. The thickness of selected crystals was confirmed using AFM topography imaging (Asylum Research Cypher). Metallic contacts were prepared

using e-beam lithography and e-beam evaporation of Pd (60 nm). For PE gating, special gate electrodes were designed with a surface area much larger than that of the PtSe<sub>2</sub> channel, in order to maximize the gate efficiency.

**Measurements.** Devices were characterized at different temperatures inside a Janis cryostat under high vacuum (10<sup>-6</sup> mbar). Drain currents were measured using a Keithley Sourcemeter 2450, while a Keithley Sourcemeter 2400 was used for the solid and PE gates. The drain voltage was kept at 100 mV for most measurements, while the source was grounded. Voltage drop across the polymer electrolyte was measured using a Keithley Electrometer 6415.

**EDLT operation.** For PE gating, we used an ion gel made from an ethyl acetate solution of the triblock copolymer PS-PMMA-PS and the ionic liquid 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide ([EMIM][TFSI]). The devices were spin coated with the gel (6000 rpm, 1 min) in Ar atmosphere. The voltage drop across the polyelectrolyte was measured by using Pd reference electrodes close to the device, in order to be able to refer the measurements to the voltage effectively acting on the channel, as shown in previous works<sup>43,47</sup>. As can be seen from the  $V_{\text{ref}} - V_{\text{PE}}$  plot (Supplementary Fig. 5), the gate efficiency is around 60%. A small hysteresis can be observed in the dependence of  $V_{\text{ref}}$  on  $V_{\text{PE}}$ , as well as from the  $I_{\text{ds}} - V_{\text{PE}}$  dependence. However, the  $I_{\text{ds}}$  versus  $V_{\text{ref}}$  curves are almost free of hysteresis. This confirms that the hysteretic behavior is due to the gate-PE interface, and not due to the device itself<sup>46</sup>. The measurements were repeated with two different reference electrodes for increased reliability, yielding almost indistinguishable results.

**Data availability.** The data that support the findings of this study are available from the corresponding author on reasonable request.

Received: 10 January 2018 Accepted: 13 February 2018

Published online: 02 March 2018

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## Acknowledgements

We thank Adrien Allain and Kolyo Marinov for fruitful discussions and help. Devices were fabricated at the EPFL Center for Micro/Nanotechnology (CMi). We acknowledge the help of Zdenek Benes (CMi) with e-beam lithography. We would like to acknowledge support by the European Research Council (ERC, Grant 682332) and Swiss National Science Foundation (Grant 157739). A.K. acknowledges funding from the European Union's Horizon 2020 research and innovation program under grant agreement no. 696656 (Graphene Flagship).

### Author contributions

A.C., A.A. and D.O. fabricated the samples and performed the measurements. A.K. supervised the experiments. A.C. and A.K. worked on the manuscript preparation with input from all authors.

### Additional information

**Supplementary Information** accompanies this paper at <https://doi.org/10.1038/s41467-018-03436-0>.

**Competing interests:** The authors declare no competing interests.

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