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Thin 3D Multiplication Regions in Plasmonically Enhanced Nanopillar Avalanche Detectors

Pradeep Senanayake,*[,†] Chung-Hong Hung,[†] Alan Farrell,[†] David A. Ramirez,[§] Joshua Shapiro,[†] Chi-Kang Li,[∥] Yuh-Renn Wu,[∥] Majeed M. Hayat,[§] and Diana L. Huffaker[†,‡]

[†]Department of Electrical Engineering, University of California, Los Angeles, California 90095, United States

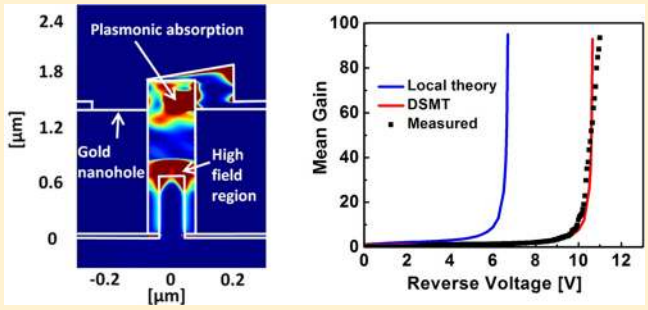
[‡]California Nano-Systems Institute, University of California, Los Angeles, California 90095, United States

[§]Center for High Technology Materials and Electrical and Computer Engineering Department, University of New Mexico, Albuquerque, New Mexico 87106, United States

[∥]Graduate Institute of Photonics and Optoelectronics and Department of Electrical Engineering, National Taiwan University, Taipei 10617, Taiwan

Supporting Information

ABSTRACT: We demonstrate a nanopillar (NP) device structure for implementing plasmonically enhanced avalanche photodetector arrays with thin avalanche volumes (~ 310 nm × 150 nm × 150 nm). A localized 3D electric field due to a core−shell PN junction in a NP acts as a multiplication region, while efficient light absorption takes place via surface plasmon polariton Bloch wave (SPP-BW) modes due to a self-aligned metal nanohole lattice. Avalanche gains of ~216 at 730 nm at −12 V are obtained. We show through capacitance−voltage characterization, temperature-dependent breakdown measurements, and detailed device modeling that the avalanche region is on the order of the ionization path length, such that dead-space effects become significant. This work presents a clear path toward engineering dead space effects in thin 3D-confined multiplication regions for high performance avalanche detectors for applications in telecommunications, sensing and single photon detection.



KEYWORDS: *Nanopillar, impact ionization, core−shell, avalanche gain, dead space, surface plasmons*

Semiconductor nanowires are attractive building blocks for nanoscale photodetectors as their small volume can ideally lower the capacitance and dark current compared to planar photodetectors.[1,2] However, typical demonstrations[3−5] involve the random growth of nanowires and subsequent transfer of a single nanowire from the growth substrate to a prepatterned substrate for electrical contact. This approach limits utility since nanowires can neither be controllably assembled into pixels for focal plane array applications nor integrated as low capacitance detectors for optical interconnect applications. In addition, the external quantum efficiency of single nanowire photodetectors is limited by the nanowire geometry with much less than 1% of the light being absorbed.[4,6] To overcome this inherent geometric limitation, antenna structures are necessary to collect light from a larger area and focus it within the nanowire. It has been recently shown that plasmonically enhanced absorption can be engineered by the geometry of the 3D antennae to excite either localized surface plasmon resonances (LSPRs) or surface plasmon polariton Bloch waves (SPP-BWs).[7,8]

Once light is absorbed in the nanowire resulting in photogenerated carriers, incorporating either avalanche or photoconductive gain can increase sensitivity.[6,9] Photoconductive gain has been generally attributed to trapping and detrapping of carriers leading to multiple carrier paths through the device.[10] Unfortunately, photoconductive gain is a slow process limiting response times to the millisecond or microsecond range. Avalanche multiplication, in contrast, is a stochastic process, which results from high energy carriers creating secondary carriers or impact ionizing by exchanging energy with the lattice. Avalanche gain typically has fast response times on the order of a picoseconds due to photogenerated carriers drifting at the saturation velocity in response to high electric field.[11] Avalanche gain requires a high electric field region so that carriers can gain sufficient energy to impact ionize. The minimum distance that carriers must travel to acquire sufficient energy to impact ionize is known as the dead space. It was predicted in planar avalanche photodetectors (APDs) that shrinking the size of the high field region to within the dead space thickness brought about improvement in both multiplication noise and gain-bandwidth product.[12] Indeed,

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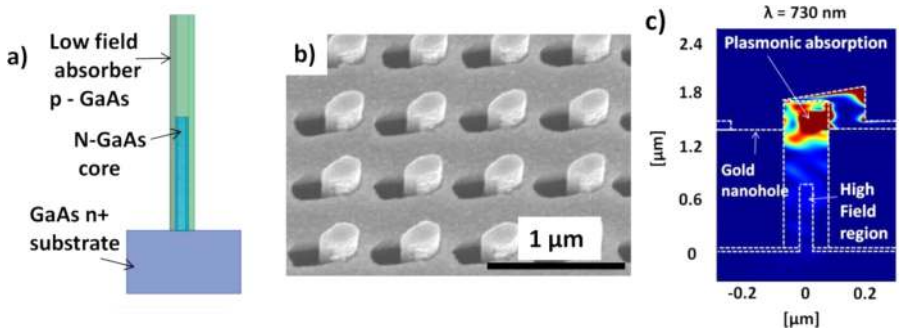

Figure 1. (a) Schematic of the separate absorption multiplication avalanche diode. (b) Self-aligned metal nanohole lattice for plasmonically enhanced absorption. (c) Plasmonically enhanced photogeneration within the nanopillar.

thin avalanche regions, comparable to the ionization path length of carriers, produce a more deterministic avalanche process, thus reducing uncertainty in the avalanche multiplication process.[12−15] Nanowires due to their flexibility in forming either axial or radial junctions offer unique opportunities in engineering a 3D electric field confined within a small volume. To date, APDs have been reported in silicon nanowires,[6,16] GaAs nanoneedles,[17] silicon−cadmium sulfide crossed nanowires,[5] and InP nanowires.[4,5] These demonstrations have shown extremely high gain values at bias voltages significantly below breakdown. While this phenomenon is attributed to avalanche gain in respective reports, the multiplication has not been supported with detailed modeling of the avalanche volume within the nanowire; thus further work is necessary to correlate the electric field within the nanowire with measurements of gain.

In this work, we report on plasmonically enhanced GaAs nanopillar (NP) APD arrays where the gain characteristics are due to a localized 3D electric field of a core−shell PN junction. We realize several improvements over state-of-art nanowire APDs by (1) fabricating position controlled NP APDs, (2) enhancing the absorption due to 3D plasmonic antennae coupling SPP-BWs modes, (3) correlating the avalanche gain to a 3D electric field of a core−shell PN junction using capacitance−voltage measurements, and (4) shrinking the size of the avalanche volume such that dead-space effects can be observed.

Figure 1a illustrates the structure of the NP APD comprised of a p-GaAs absorber (150 nm in width and 900 nm in height) atop a core−shell GaAs PN junction. The n-GaAs core is 80 nm in width and 800 nm in height, while the p-GaAs shell is 35 nm thick surrounding the core. The intended n-core and p-shell doping levels are both ∼10^{18} cm^{-3}. The nanopillars are encapsulated with an $In_{0.5}Ga_{0.5}P$ high bandgap passivation layer (not shown) to mitigate the effect of surface states.[18] The patterned growth process and precursors are fully described elsewhere.[19] The nanopillars are then planarized with a BCB polymer layer, where the tips are exposed by etch-back. Gold contacts are evaporated at an angle, such that a gold nanohole lattice is self-aligned to the nanopillar array. The nanohole width and length are defined and therefore controlled by nanopillar width and deposition angle.[8] After fabrication, the devices are diced, mounted, and wire-bonded to chip carriers for electrical and optical characterization. The final fabricated nanopillar arrays have active area of 17410 μm^2, 27030 μm^2, 42830 μm^2, and 53700 μm^2 comprising 48360, 75080, 119000, and 149160 NPs, respectively.

Figure 1b shows a scanning electron micrograph (SEM) of the resulting metal nanohole lattice self-aligned to the patterned nanopillar array. The hole dimensions are 150 nm × 200 nm on a 600 nm pitch. A nanohole lattice pitch of 600 nm is chosen for peak absorption within the GaAs bandgap. Detailed optical simulations of the SPP-BW absorption due to metal nanohole lattice are shown in the Supporting Information. Efficiency plots indicating 42% efficiency at 730 nm are also shown in the Supporting Information. Figure 1c shows an optical-field intensity contour plot associated with the plasmonically enhanced absorption at 730 nm. Due to the unique 3D geometry of the NP antenna, the SPP-BW mode confines the absorption at the tip of the p-GaAs absorber and away from the contact metal.[8]

Figure 2a shows the typical light and dark current−voltage ($I-V$) characteristics of the nanopillar array contacting

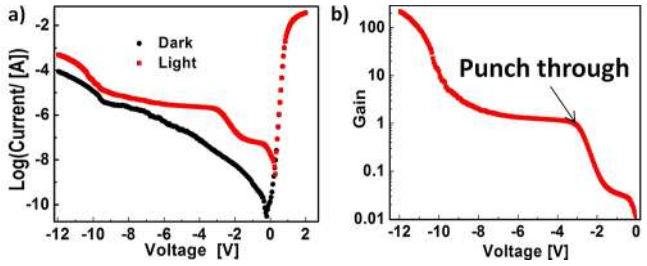

Figure 2. (a) Shows the light and dark $I-V$ characteristic and (b) the multiplication of the core−shell diode.

∼149160 NPs at 300 K. The dark $I-V$ characteristic in Figure 2a can be fit to the ideal diode equation where the current, I, is given by $I = I_o \exp(q(V - IR_s)/nkT)$, I_o is the saturation current, R_s is the series resistance, q is the elementary charge, T is the temperature, V is the bias voltage, and ideality factor n. The nanopillar array devices exhibit excellent diode characteristics with a low series resistance of ∼40 Ω, ideality factor of 1.6, and saturation current of 3×10^{-12} A. These diode characteristics suggest a high quality PN junction is formed within the nanopillar. At zero bias, under light conditions, an extremely low photocurrent of 20 nA is measured, indicating that a short diffusion length ($\ll 1$ μm) results in the photogenerated carriers not being extracted by the core−shell electric field. However, as the reverse bias is increased, the photocurrent increases corresponding to both (1) an increase in the field dependent diffusion length of photogenerated carriers[20] and (2) an extension of the depletion region into the low field absorber. At −3 V, all of the photogenerated carriers in the nanopillar are extracted, forming a plateau region in the

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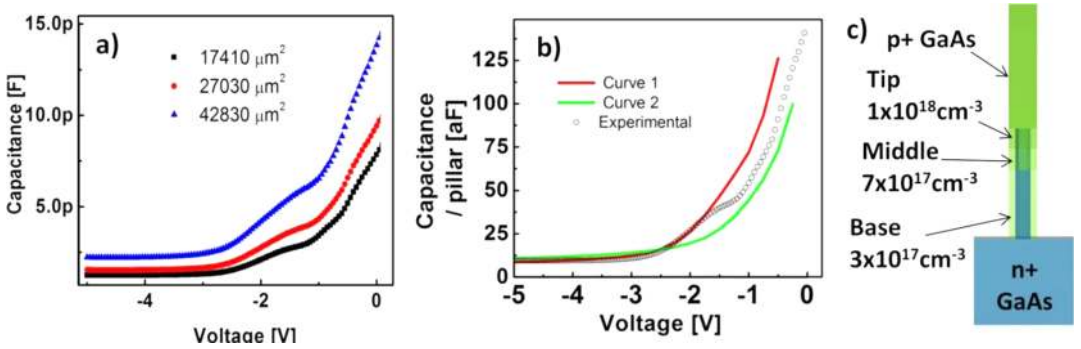

Figure 3. (a) Capacitance−voltage (C−V) characteristics of nanopillar arrays with different number of nanopillars. (b) Extracted average capacitance per nanopillar compared with a modeled capacitance. (c) Schematic of the structure used for 3D modeling of capacitance.

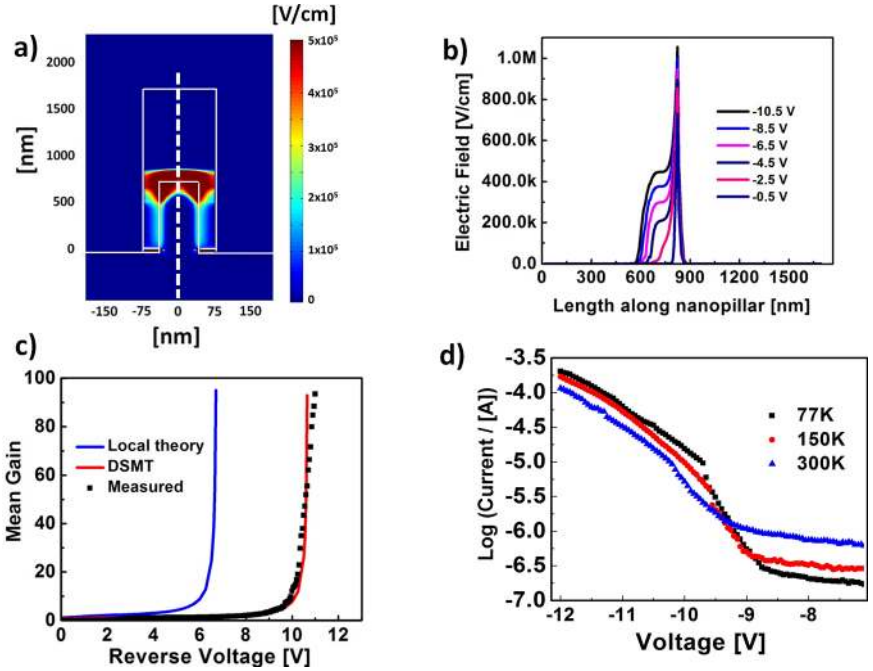

Figure 4. (a) Contour plot of the electric field in the nanopillar at −10 V. (b) Axial electric field profile along the pillar as a function of reverse bias. (c) Calculated gain using local and DSMT compared with experimental gain. (d) Characteristic temperature dependence of avalanche breakdown.

photocurrent resulting in a responsivity of 0.27 A/W at 730 nm. This bias voltage corresponds to the punch through voltage indicating the maximum expansion of the depletion region. Further biasing the device results in the photocurrent being multiplied beyond the primary photocurrent due to avalanche multiplication. Figure 2b shows the gain characteristic calculated by subtracting the dark current from the light current and normalizing with respect to the primary photocurrent at the onset of the plateau region. The unity gain primary photocurrent is measured at −3.2 V. Increased reverse bias results in a monotonic increase in avalanche gain until gains as high as ∼216 can be achieved at −12 V due to avalanche multiplication.

A deeper understanding of the measured gain characteristics and a correlation with the volume of the avalanche region can be obtained from modeling the capacitance−voltage (C−V) measurements using the doping and the geometry of the nanopillar. The best fit for the C−V characteristic can be used to estimate the high electric field volume responsible for the avalanche gain. Figure 3a shows capacitance (C−V) characteristics as a function of area at a high frequency of 1 MHz to sample purely the junction capacitance. The capacitance scales with area indicating that the junction capacitance of each nanopillar is acting in parallel and a very high uniformity in the formation of the core−shell PN junction in the nanopillar array. At zero bias the capacitance due to the core−shell junction is ∼0.347 fF/μm^2. A small reverse bias of −1 V results in a ∼50% drop in the capacitance, until higher reverse biases results in the saturation of the capacitance to ∼0.05 fF/μm^2. We roughly estimate that this ultrasmall saturation capacitance would allow nanopillar diode arrays, with as few as 3000 NPs to have a RC limited bandwidth exceeding 40 GHz.

Figure 3b shows the average capacitance per nanopillar overlaid with C−V modeling (Curves 1 and 2) of the NP core−shell junction. The average junction capacitance per nanopillar can be estimated by subtracting the contribution to the capacitance due to BCB and dividing by the number of NPs in the array. The modeled C−V curves are generated by solving the 3D Poisson equations[21] taking into account the core−shell geometry and doping of the hexagonal nanopillar. In both curves 1 and 2 the modeled core is 80 nm in diameter and 800 nm in height and uniformly doped n-type at a doping

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concentration of 3×10^{18} cm^{-3}. The doping of the p-type doped shell is coarsely graded, that is, divided into three sections including base, middle, and tip accounting for expected growth rate changes during nanopillar epitaxy.[19,22] The doping concentration within the base, middle, and tip sections are constant at 3×10^{17} cm^{-3}, 7×10^{17} cm^{-3}, and 1×10^{18} cm^{-3}, respectively. However, the $C-V$ characteristics are very sensitive to the thickness of the middle section surrounding the tip of the core. Thus, curve 1 (2) represents a base section spanning 500 nm (600 nm), the middle section of 150 nm (100 nm), and the tip at 150 nm (100 nm). A clear trend can be seen in that the peak capacitance at low bias voltages drops as the size of the high doped region encapsulating the tip of the core is reduced, while the saturation capacitance also increases. Curve 1 is chosen to most accurately represent the characteristics of the device in terms of predicting the punch through voltage, the shape of the CV characteristic, and the saturation capacitance $C_{sat} \sim 9$ aF. The $C-V$ characteristic of curve 1 can be understood as the radial expansion of the 3D depletion region by initially depleting the core−shell junction and then extending axially to the pillar edge. At the bias voltage of −5 V the depletion region has expanded axially resulting in the saturation of the capacitance at ∼9 aF for a single nanopillar.

Figure 4a shows a contour plot of the electric field through the center of the nanopillar (in the x-plane) at the breakdown voltage of −10 V. The graded doping of the p-shell results in the high field ($E > 5 \times 10^5$ V/cm) region being confined to within 310 nm of the tip of the core. Since very high electric fields are confined to within a very small region of the core−shell junction, the resulting impact ionization is also being confined to a very small volume. The thin avalanche volume results in the measured gain characteristics to be dominated by dead space effects.

Figure 4b shows the axial electric-field profiles as a function of reverse bias through the center of the nanopillar (at the location of the dotted white line in Figure 4a) for the structure described by Curve 1. The avalanche region at the breakdown voltage is confined to an axial region ∼310 nm in width with highly localized fields as high as 1 MV/cm at the tip of the nanopillar core. The bias dependent electric field profiles can be used to model the expected gain using both local theory for carrier multiplication[23] and dead space multiplication theory.[12] It is expected that modeling the gain in terms of dead space multiplication theory (DSMT) would lower the mean gain at a given bias and shift the breakdown voltage to higher biases. In both cases, it is assumed that a majority of carriers contributing to avalanche multiplication traverse a path through the center of the nanopillar as shown by the white dotted line in Figure 4a. In terms of the local theory the mean multiplication (M) is given using eq 1 below, where α is the electron ionization coefficient, β is the hole ionization coefficient, and is evaluated at $x_0 = W$ where W is the position of the depletion edge.

$$M(x_0) = \frac{\exp[-\int_0^{x_0}(\alpha(x) - \beta(x))\mathrm{d}x]}{1 - \int_0^W \alpha(x)\exp[-\int_0^x(\alpha(x') - \beta(x'))\mathrm{d}x']\mathrm{d}x} \quad (1)$$

For the case of DSMT the electric-field profiles in Figure 4b were also used to calculate the dead-space profiles across the nanopillar and the nonlocal ionization coefficients for electrons and holes in GaAs as described by Saleh et al.[14] With this information we calculate the probability density functions of the random distance of ionization for electrons and holes. A hard-threshold dead space is assumed, for which the ionization coefficient is zero for carriers that have traveled a distance shorter than the dead space and is a function of the electric field for carriers that have traveled a longer distance.

Figure 4c shows the calculated gain using local theory and DSMT using the electric fields of curve 1 overlaid with the experimental gain. Local theory is shown to produce an overestimation of the measured gain resulting in an under estimation of the breakdown voltage. However, the mean gain estimated by DSMT is able to predict the experimental gain and breakdown voltage more accurately than the local theory, since the effects of the dead space are significant.

Figure 4d shows the temperature-dependent $I-V$ characteristics of the core−shell NP diodes at high reverse biases from 77 to 300 K. All curves show similar behavior: a clear transition from a generation-recombination dominated current to an avalanche current close to the breakdown voltage at ∼9.5 V. The breakdown voltage is consistent with the predictions of the DSMT. This dramatic change in the $I-V$ characteristic suggests that dark carriers injected into the high-field core−shell region are multiplied. The breakdown voltage can be calculated by extracting the voltage at which multiplication (M) goes to infinity. The unmultiplied dark current is taken to be −7 V from which the multiplication factor M is calculated. The intersection of $1/M$ vs bias is used to estimate the breakdown voltage at each temperature (see Supporting Information). The breakdown voltage shifts to larger biases with increasing temperature with a shift of +3.3 mV/K, such a small shift in the breakdown voltage suggests that the avalanche gain is produced by a high field region on the order of the ionization path length of electrons as higher temperatures result in greater energy scattering of carriers. The clear shift in the breakdown voltage is in stark contrast to previous reports of GaAs nanowire APDs where a positive shift in the breakdown voltage is not clearly observed.[17]

The avalanche gain characteristic reported in this work is contrary to previous reports for NW APDs where very high gains are achieved at bias voltages significantly below breakdown.[4,5,17] High gain values below the breakdown voltage cannot be explained by either the local model for avalanche gain or dead space multiplication theory. Our results show that avalanche gain in nanopillar APDs can be explained by the avalanche multiplication of carriers within a volume ∼310 nm × 150 nm × 150 nm in size with the inclusion of the effect of dead space. Since this volume is within a few multiples of the ionization path length of carriers, local theory, which ignores the dead space, overestimates the mean gain produced by this NP-APD. The temperature-dependent characteristics support the conclusion of a small avalanche volume with a shift in the breakdown voltage of +3.3 mV/K, which has not been shown in previous demonstrations of GaAs nanowire APDs.[17] Detailed 3D modeling of the experimental capacitance−voltage is used to model the 3D electric field profile at breakdown, the size of the avalanche region, and fit the measured gain characteristics. Our results indicate that the gain characteristics of nanopillar APDs can be estimated by modeling the $C-V$ characteristics and 3D electric fields of the NP-APD.

In conclusion, we have realized position controlled plasmonically enhanced avalanche diodes with thin avalanche regions. Avalanche gains as high as 216 have been achieved due to the 3D electric field due to a core−shell junction. The core−shell PN diodes exhibit diode characteristics with ideality factors of 1.6, and a junction capacitance as low as 0.05 fF/μm^2.

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Temperature-dependent current−voltage measurements show a breakdown voltage shift of +3.3 mV/K confirming avalanche breakdown as the gain mechanism. The multiplication has been modeled using DSMT to show dead space effects are dominant in the avalanche characteristics of thin avalanche regions in NP-APDs. This demonstration shows that core−shell junctions can be engineered to produce high confined 3D electric fields within the avalanche path length of carriers and is a clear path toward utilizing dead space effects for high sensitivity and short transit time in nanopillar avalanche photodiodes. Future work will focus on extracting more accurate 3D doping profiles from atom probe tomography[24,25] for the design of 3D avalanche regions and the measurement of reduced excess noise characteristics due to dead space.

■ ASSOCIATED CONTENT

Ⓢ Supporting Information

Pitch dependent plasmonically enhanced absorption and experimental spectral response (Figure S1) and breakdown voltage extract as a function of temperature (Figure S2). This material is available free of charge via the Internet at http://pubs.acs.org.

■ AUTHOR INFORMATION

Corresponding Author

*E-mail: pradeeps@ee.ucla.edu.

Notes

The authors declare no competing financial interest.

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