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Thin electron beam defined hydrogen silsesquioxane spacers for vertical nanowire transistors

Running title: Thin EBL defined HSQ spacers

Running Authors: Memišević et al.

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A method to fabricate inorganic vertical spacer layers with well-controlled thickness down to 40 nm using electron beam exposure is demonstrated. These spacers are suitable in vertical nanowire transistor configuration. As spacer material, the authors use hydrogen silsesquioxane (HSQ), a material with low permittivity and high durability. They show that the resulting HSQ thickness can be controlled by electron dose used and it also depend on the initial thickness of the HSQ layer. To achieve good reproducibility, the authors found it necessary to fully submerge the nanowires beneath the HSQ layer initially and that the thickness of HSQ before exposure needs to be determined. Finally, they introduce these steps in an existing transistor process and demonstrate vertical nanowire transistors with high performance.

I. INTRODUCTION

Vertical nanowires may be used in a promising future transistor architecture, where the gate-all-around geometry provides good electrostatic control and the nanowire technology allows for growth of heterostructures with large lattice mismatch.[1] The vertical nanowire transistor architecture includes spacers that are required to separate the source-, channel-, and drain-regions of the transistor. The spacer material should have a low dielectric constant to reduce the parasitic gate capacitance; furthermore, the spacers need to be mechanically and thermally stable. To reduce the parasitic series resistance, the spacers' thickness must be below a few tens of nanometers.[2] Although individual transistors with excellent performance have been demonstrated using organic spacer layers,[3] this approach has difficulties in thickness scaling as well as thermal stability.

A good candidate for the spacer material is hydrogen silsesquioxane (HSQ), which is a flowable silicon oxide used for planarization as well as a negative resist for electron beam lithography.[4–6] HSQ has good gap-filling properties, it can withstand high temperatures, and it is durable and thereby can withstand further processing. It has previous been demonstrated that HSQ can be spin-coated on samples, and subsequently transformed to silicon dioxide through thermal heating. The final thickness of the spin-coated HSQ can be controlled with wet-etching in diluted HF.[7] The curing temperature however needs to be above 500 C, a high temperature that can damage the materials within the transistor architecture (e.g., III–V materials and high-k oxides). Another well-known approach is to transform the HSQ to silicon dioxide through electron beam

exposure (EBL), a method which does not require high temperatures. However, the use of HSQ technology in combination with vertical nanowires has not been explored for III–V materials. By introducing the HSQ in the fabrication process of InAs nanowire transistors, we can remove the reactive ion etching step used for thinning organic layers, a step which can be detrimental to the device performance. The inorganic spacer further allows for important postgate metal anneals at higher temperatures as compared to organic layers, which are limited to about 150 C anneals. Instead of EBL, extreme ultraviolet lithography can be utilized to reach large wafer scale processes. [8]

In this article, we study electron beam exposure of HSQ layers and demonstrate that the final thickness of the HSQ spacer can be set by the electron exposure dose in an electron beam lithography system, thus allowing for curing of the HSQ and accurate control of spacer layers. First, we investigate the thickness–dose relation for planar HSQ samples, followed by a study of how the exposure of the HSQ is affected by the presence of vertical nanowires. Finally, the process is used to fabricate vertical nanowire transistors with HSQ as the spacers. Measured transistor performance is comparable to devices with organic spacers.

II. EXPERIMENTAL

With the goal to realize a vertical nanowire transistor architecture, as illustrated in Fig. 1, we evaluated three types of samples. A general dose test pattern to develop a planar spacer layer, samples for studies of the effect of the nano- wires on the HSQ-exposure, and complete transistor samples. For each type, highly resistive 1 x 1 cm^2 Si-

wafers (111) with a 200-nm-thick InAs buffer layer was used. [9] Processing of the HSQ during prebaking, exposure, development, and curing was identical on all samples, and are referred to as standard steps as described in the following. After spin coating, the sample was baked for 2 min at 200 C to remove excessive solvent. The HSQ was subsequently exposed with an electron beam lithography (EBL) system, Raith 150 from Raith GmbH, with a beam voltage of 20kV. The exposed resist was developed in 25 wt. % tetramethylammonium hydroxide (TMAH) for 60 s and then rinsed in deionized water for 30 s. After development, the sample was cured for 60 min at 350 C in a mixed flow of 20% H_2 and 80% N_2 in a rapid thermal processing system.

A. Planar dose test samples

Dose test samples were used to study the effect of the electron exposure dose as well as different initial thicknesses of the HSQ on the final thickness of the HSQ. Four samples were spin coated with FOX 15 (HSQ) from Dow Corning, for final thicknesses of 550, 400, 200, and 130 nm. For the 550 nm sample, a spin speed of 1500 rpm was used. For the thinner films, a spin speed of 3000 rpm was utilized. To obtain the 200 and 130 nm films, the HSQ was diluted in 1:1 and 1:2 in methyl isobutyl ketone, respectively. The samples were prebaked, exposed, developed, and cured according to the standard steps. The exposed patterns for the dose test were rectangles with nominal sides of 4 x 20 um written in arrays with different doses, as shown in Fig. 2(a). No proximity correction was done due to the large spacing (20 um) between the exposed areas.

To determine the maximum HSQ thickness that can be achieved by exposure of these samples, large rectangles (20 x 40 um^2) were overexposed with a large electron dose of 800 uC/cm^2, which is three to four times higher than the dose needed to fully expose the HSQ. The height of the structures was determined by atomic force microscope (AFM) measurements, and the measured height from a representative sample can be seen in the Fig. 2(b).

B. Nanowire-HSQ samples

The next step after the dose test samples was to study the interaction of the HSQ spin-coating and EBL exposure with the nanowires. To define the position and diameter of the nanowires, a standard PMMA-based lift-off process was used to form 15-nm-thick thermally evaporated gold dots. The structures consist of 100 um-long lines with nanowires in zig–zag formation and with different pitch for the different lines.[10] The nanowires were then grown with metalorganic-vapor-phase-epitaxy at 420 C, [11] resulting in nanowires with diameters of 45, 47, and 50 nm with lengths between 200 and 1000 nm. For all three diameters there are structures with a nanowire pitch of 100, 200, 300, 500, and 1000 nm, as shown in Figs. 2(c) and 2(d). The distance between the rows in the structure is 2.5 um. The sample was then spin coated with HSQ using 1500 rpm for 60 s, resulting in a 550-nm-thick layer. After the coating, the standard steps were used for pre-baking, exposure, development, and curing. The HSQ was exposed around the nanowire arrays, as marked in Fig. 2(c). The exposure of the HSQ was performed with electron doses of 55, 60, and 65 uC/cm^2, which were chosen from the dose-test samples. The lowest dose is below the necessary dose to generate a continuous HSQ layer and the

other two doses are above, thus probing the minimum achievable HSQ thickness. The same type of reference structures was used as for the dose-test samples, to estimate the largest achievable thickness of the HSQ on a planar surface away from the nanowires. Finally, the sample was covered with 5 nm titanium after HSQ development to improve the contrast during the inspection with scanning electron microscope (SEM).

C. Device Fabrication

The final step was to use the HSQ as spacer in fabricating InAs nanowire transistors. The InAs nanowires were positioned and grown using the same method as for the cross section sample as described in Sec. II B. The devices consist of 60 nanowires with a diameter of 28 nm, a length of 500 nm, and a pitch of 200 nm. During growth, the top and the bottom parts of the wires were n-doped using tetraethyltin (TESn), corresponding to a doping concentration of around 10^{19} cm^{-3}. [12] The flow of TESn was turned off during the growth of the gated part, although memory effects probably introduced unintentional doping of about 10^{18} cm^{-3}. After the growth, a high-k oxide was deposited on the sample using atomic layer deposition. The high-k layer consists of ten cycles of Al_2O_3 deposited at 250 C and 50 cycles of HfO_2 deposited at 100 C, which corresponds to an equivalent oxide thickness of 1.4 nm. Subsequent fabrication steps described in the following text are visualized in the Figs. 3(a)–3(f). A bottom spacer was made by spin coating the sample with HSQ using 1500 rpm, followed by the standard steps described in the first paragraph in Sec. II, using an exposure dose of 65 uC/cm^2 to achieve a thickness of 90–100 nm Fig. 3(b). A layer of 60 nm tungsten gate was then sputtered on the sample and a gate-pad was defined using soft-UV lithography Fig. 3(c).

The gate-length of the devices was defined by reactive ion etching. After the gate-definition the high-k was removed from the top of the wires with buffered oxide etch using an organic resist. The top HSQ spacer is fabricated following the same fabrication steps as the bottom spacer. The difference is that the exposed area is smaller than the one used for the bottom-spacer and a higher exposure dose is used for the top-spacer to achieve a thicker spacer Fig. 3(d). Lift-off was then used to define the top-contact consisting of 30 nm evaporated nickel and 60 nm evaporated gold. A schematic illustration and a SEM image of the finished transistor can be viewed in Figs. 1(a) and 1(b).

III. RESULTS AND DISCUSSION

A. Results from the dose test samples

The results from the dose test exposures are shown in Fig. 4, showing the measured thickness of the HSQ layer as a function of the exposure dose and the pre development thickness. For the exposure doses above 180 uC/cm^2, the thickness saturates and becomes equal to the thickness for the reference structures. The smallest achievable thickness on a planar surface is found to be essentially independent on the initial thickness, with demonstrated films down to 25 nm.

To reduce the influences from local variations in the HSQ it would be beneficial to lower the slope of the curves, i.e., to decrease the contrast of the HSQ. The contrast of the HSQ depends on the ratio between the –Si–H–bonds and –Si–O–Si–bonds.[13] A

more strongly cross-linked HSQ contains more –Si–O–Si–bonds and a lower electron dose can be used to obtain a certain thickness. [13] Thermal heating and electron exposure contribute to cross-linkage of the HSQ, thereby the contrast can be decreased by a higher prebaking temperature. [14–16] After exposure, the slope can be decreased by lowering the concentration of TMAH or reducing the development time and thereby effectively reduce the amount of the dissolved HSQ. [13] Overall, the contrast of HSQ decreases with initial thickness due to a larger generation of the secondary electrons in the thicker resist. [16,17]

B. Results from nanowire cross-section samples

Figures 5(a)–5(c) shows structures where the same electron dose was used to expose HSQ around nanowires with varying pitch and length. The final thickness of the HSQ around the nanowires in Figs. 5(a) and 5(b) is about 60 nm, even if the nanowire length and spacing is varied. This corresponds well to the thickness obtained from planar samples for the given dose, 60 uC/cm^2. The final thickness of the HSQ in Fig. 5(c) is much thicker than what could be expected from the dose used; this result is discussed further in Fig. 6. In Figs. 5(d)–5(f), the pitch (200nm) and nanowire height (350–400 nm) is essentially constant, but the electron dose is varied between 55 and 65 uC/cm^2. Similarly to what was observed from the dose tests, the thickness of the remaining HSQ increases when the electron dose is increased. The lowest electron dose (55 uC/cm^2) used for the structure in Fig. 5(d) did not generate any continuous HSQ layer on the planar dose test samples and no continuous layer of HSQ around the nanowires are found around the wires, limiting the minimal achievable thickness.

The final thickness of the HSQ is plotted against the length of the wires in Fig. 6(a) to explain the result observed in Figs. 5(a)–5(c). The same electron dose (60 uC/cm^2) was used to expose the HSQ around the nanowires, although length and pitch were varied. The thickness is reproducible for nanowires with length below the pre-exposure thickness of the HSQ, 550 nm. The final thickness of the HSQ starts to increase when the length of the nanowires approaches the pre-exposure thickness of the HSQ. This can be explained with help of Fig. 6(b), which illustrates two possible cases when the sample with nanowires is coated with HSQ. Either the wires will be partially covered as in case A, or the nanowires are fully submerged under the planarized resist as in case B. For case A, the HSQ thickness close to the nanowires before exposure is observed to be larger as compared with the HSQ thickness far away from the arrays, due to the imperfect planarization. The final thickness of the HSQ in case A is larger due to higher amount of secondary electrons from the thicker HSQ around the wires. To obtain a good reproducibility with this method it is thus important that the spin-coating and prebaking generates the same pre-exposure thickness and that the nanowires are fully covered by HSQ. When these two requirements are fulfilled the final thickness of the HSQ will be well controlled by the electron dose used with a smallest thickness down to 41 nm can be achieved as shown in Fig. 6(c).

C. Devices

Results from DC-measurements from one device with a gate-length of 160 nm and 60 nanowires is shown in Fig. 7. The measured performance is comparable to devices using organic spacers or a mix of organic and nonorganic spacer, as expected. [3,10] The total circumference of the nanowires were used to normalize the data. The highest

transconductance, g_m, was 390 mS/mm with a threshold voltage of -0.02 V at V_{DS} of 0.5 V. The lowest value for the subthreshold swing was 243 mV/dec at a V_{DS} of 50 mV, and the lowest R_{ON} was 1.3 kΩ/um.

IV. SUMMARY AND CONCLUSIONS

We have developed a process to fabricate thin HSQ- spacers around vertical nanowires and show that the final thickness of the HSQ spacer can be controlled by electron beam exposure dose. To achieve a uniformly thick HSQ around the nanowires, it is important that the nanowires are fully covered by the HSQ, and it is necessary that the HSQ thickness before the exposure is known to select right elec- tron dose and accurately control the final thickness. Vertical transistor structures are implemented and the performance of the devices is comparable to earlier results.

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Figure Captions

Figure 1. (a) Schematic illustration of a vertical nanowire tran- sistor, where the spacers support the structure and separate the metal-layers. (b) SEM image of a finished device using the HSQ as spacer layers.

Figure. 2. (a) SEM image of a dose-test array. The exposure dose increases from left to right and from the top row toward the bottom row. In the two rows at the top, the used dose-steps are finer than the dose-step used in the bottom two rows. The size of the exposed rectangles differs with dose because the structures at top row are under-exposed and the structures at bottom row are over-exposed. (b) Measured height variation (AFM) for one pattern. The structure is wider than 4 lm due to the overexposure. (c) The rectangle in the figure marks the unit-cell of the structure which contains lines that have different pitch, i.e., 100, 200, 300, 500, and 1000 nm. The unit-cell was repeatedly written over the sample. During exposure, only the HSQ in the proximity of the unit- cell was exposed with one of the three doses, i.e., 55, 60, and 65 uC/cm^2. (d) SEM image of one of the nanowire arrays in zig–zag formation surrounded by HSQ. The pitch between these nanowires is 200 nm. (Sample is tilted 30° .) Inset shows Au-dots in zig–zag formation before the growth of the nanowires.

Figure 3. Main steps in the fabrication of the nanowire transis- tor. (a) The nanowires have been grown and the sample is covered with a high-k. (b) HSQ in an area larger than the gate-pad is exposed with EBL around the nanowire arrays to fabricate the bottom spacer. (c) Using sputtering, organic resist, UV-lithography, and reactive ion etching the gate-pad is fabricated and the gate-length is defined. (d) The top spacer is made by the same fabrication steps as the bottom spacer except for the difference that the exposed area is smaller and a higher exposure dose is used for the top- spacer. (e) The sample is

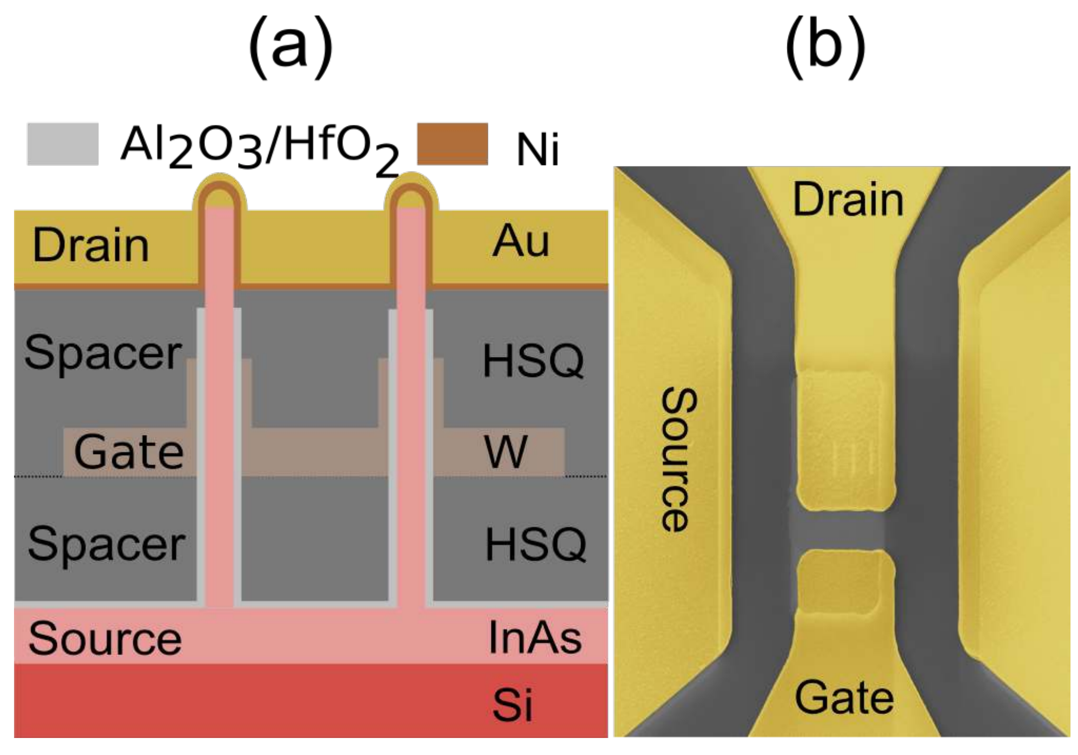
covered with resist to lift the contact-pads above the doped InAs-layer. (f) The contact-pads are defined using lift-off and evaporation.

Figure 4. Results from dose test samples. The thickness is increasing with the dose and the sensitivity is increasing with thicker resist due to larger amounts of secondary electrons.

Figure 5. Cross-sectional views of HSQ surrounding nanowires. (a)–(c) Images were the pitch between the nanowires is varied and the same electron dose of 60 uC/cm^2 was used to expose the HSQ. (d)–(f) The nanowires have same pitch (200 nm) and length. The electron dose was varied, using 55, 60, and 65 uC/cm^2.

Figure 6. (a) Final thickness of the HSQ is plotted as a function of the length of the nanowires. Same electron dose of 60 uC/cm^2 was used to expose the HSQ around the nanowires. (b) Schematic illustration of ideal and imperfect planarization around the nanowire. In the case A, the nanowires are partially covered with an upslope as the result or the nanowires are fully covered as in the case B. (c) Thinnest spacer that was achieved on these samples with a thickness of 41 nm.

Figure 7. (a) I_{DS} and g_m vs V_{GS}. This device consists of 60 nanowires with a diameter of 28 nm and the gate length is 160 nm. (b) I_{DS} vs V_{DS} from the same device as in (a).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(b)
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HSQ
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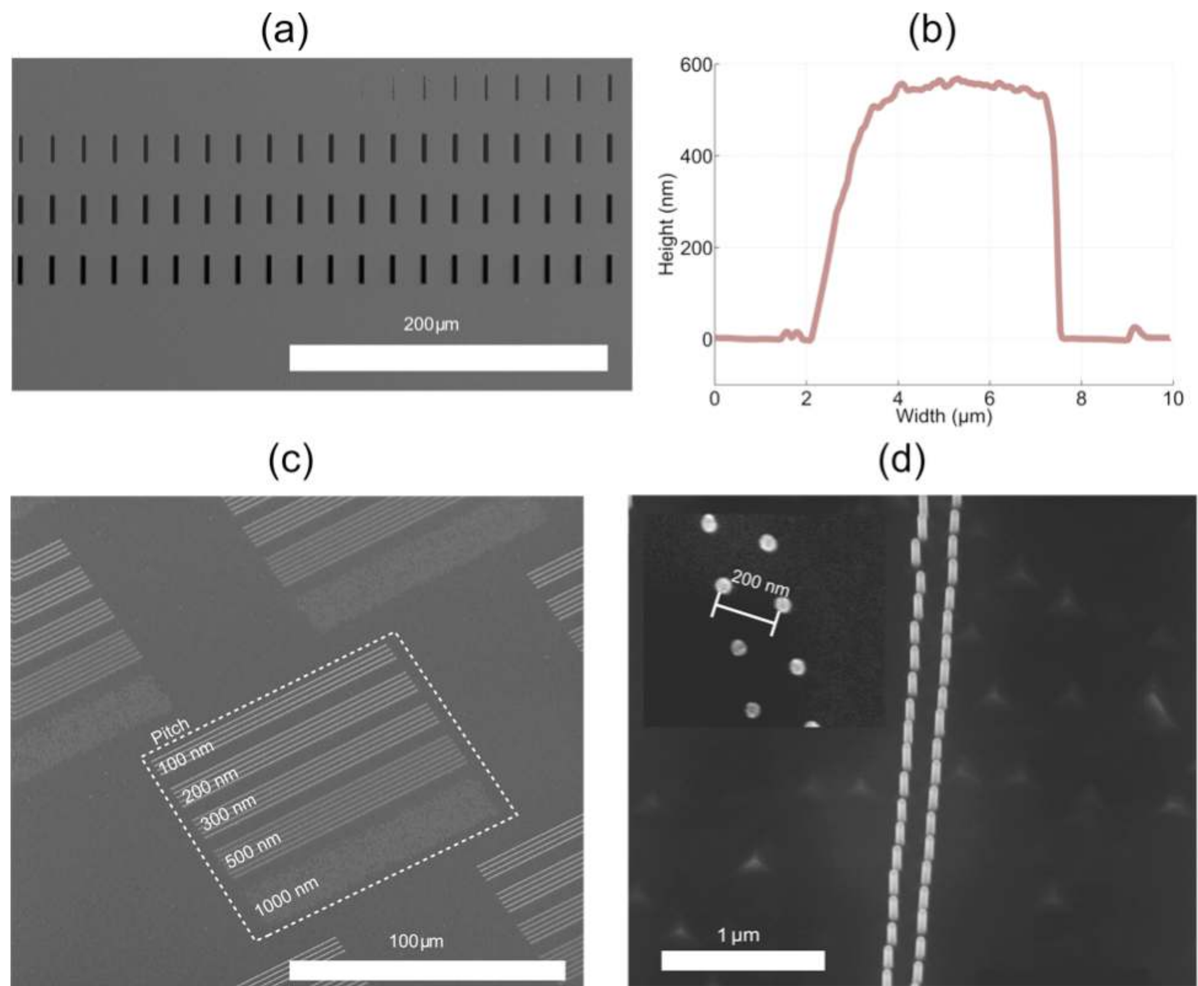
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(b)
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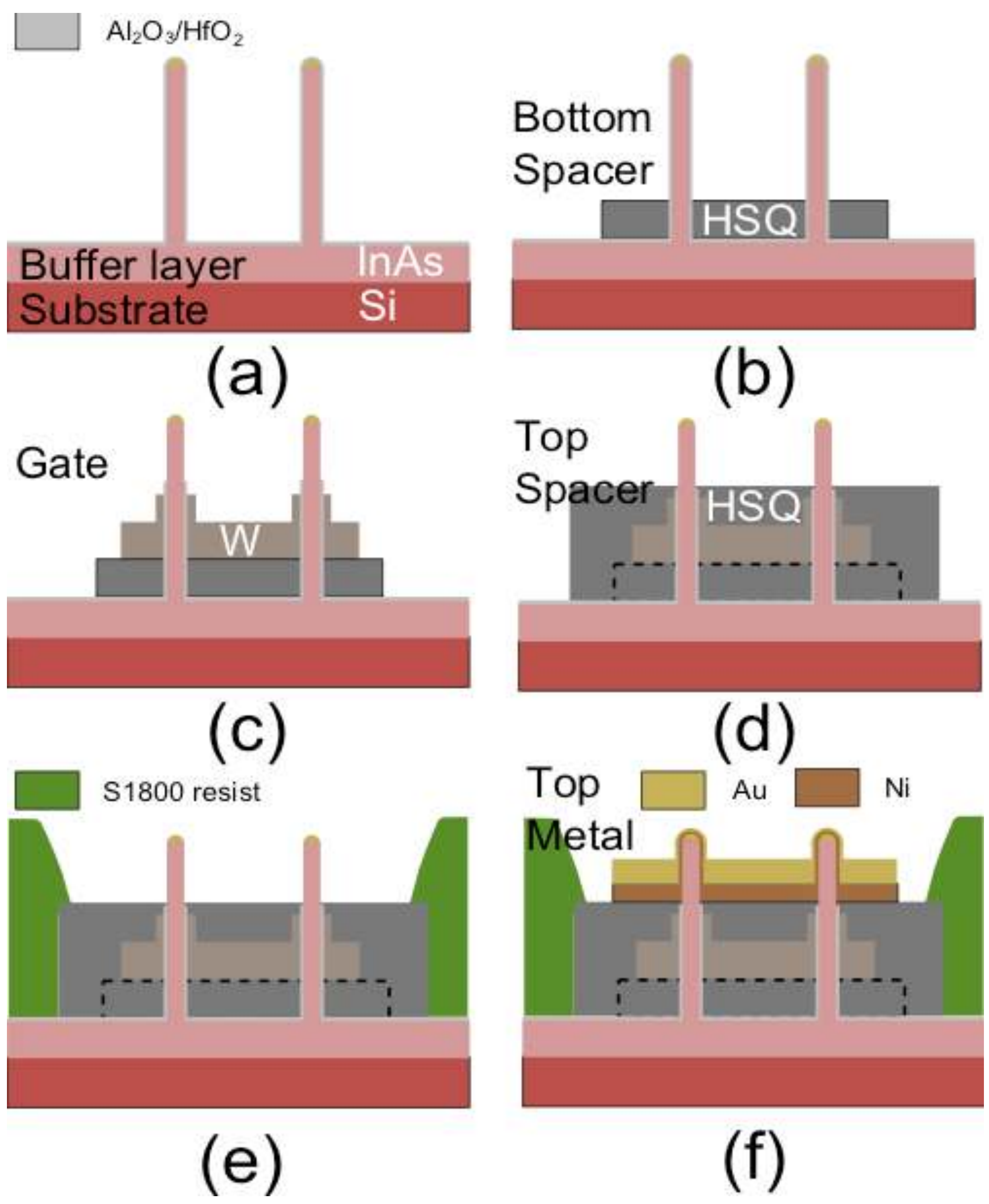
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Substrate
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Bottom
Spacer
HSQ
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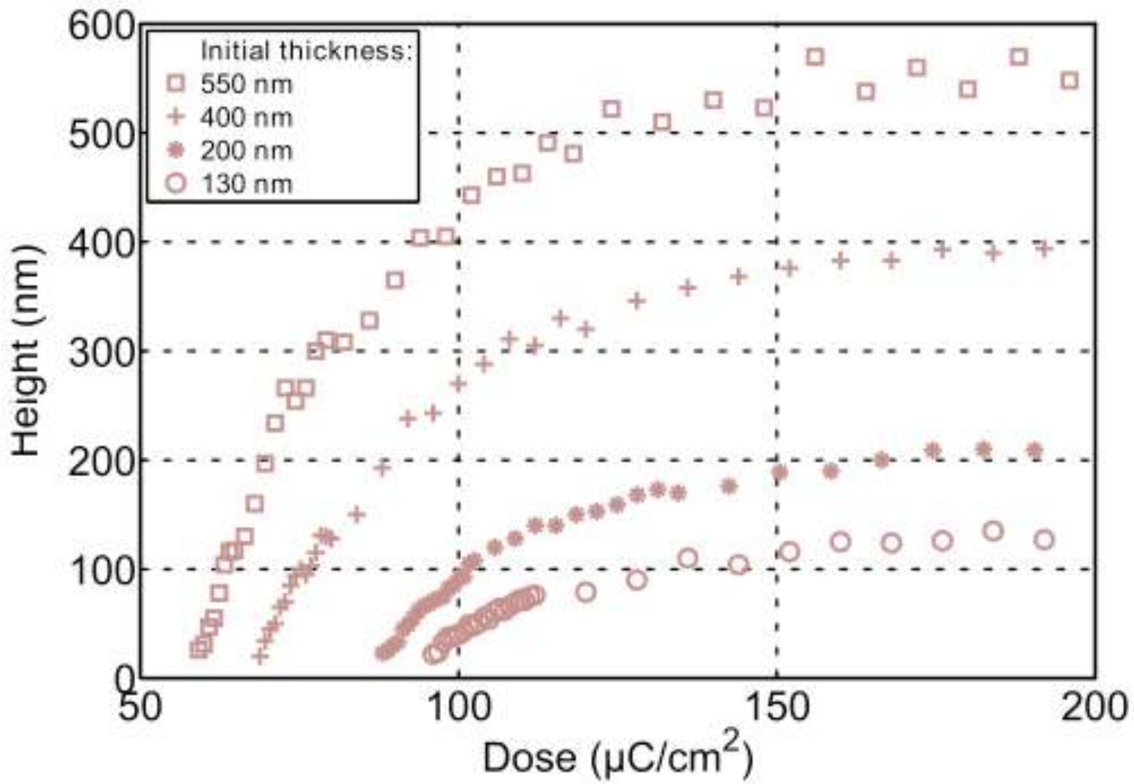
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200 nm
130 nm
Height (nm)
Dose (μC/cm2)
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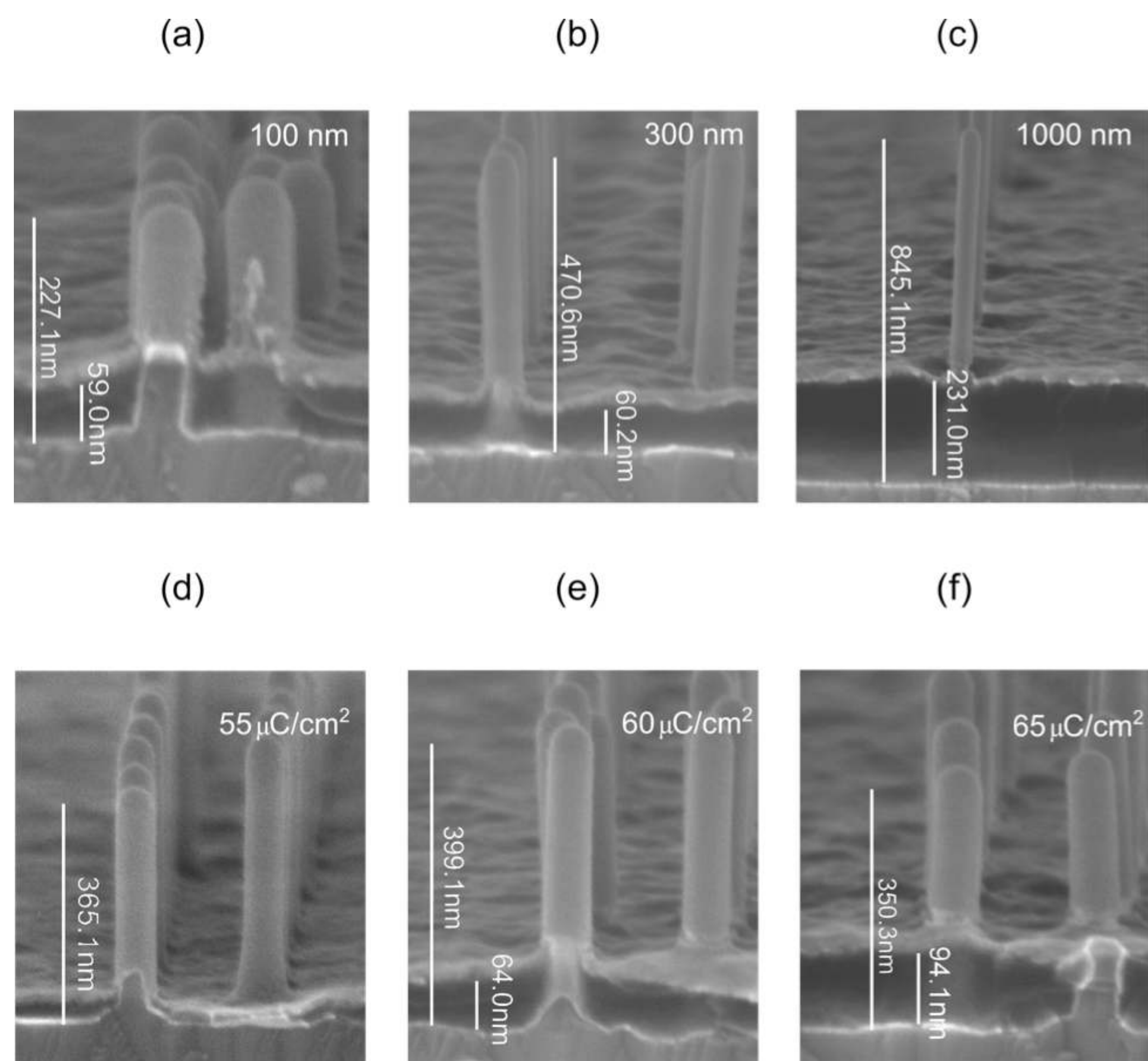
50
100
150
200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(b)
(c)
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300 nm
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(d)
(e)
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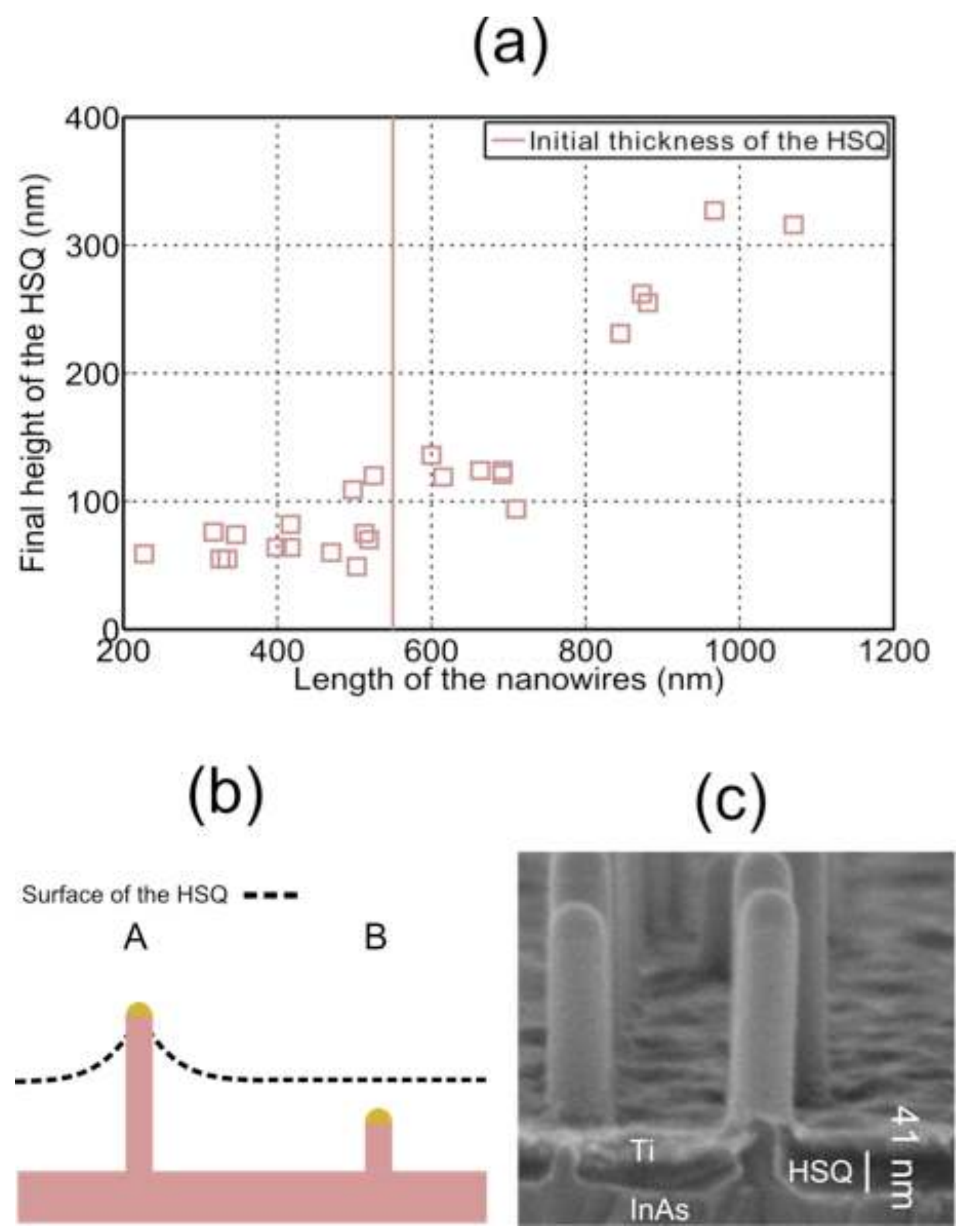
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Initial thickness of the HSQ
Final height of the HSQ (nm)
Length of the nanowires (nm)
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300
400
200
400
600
800
1000
1200
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Surface of the HSQ
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B
(c)
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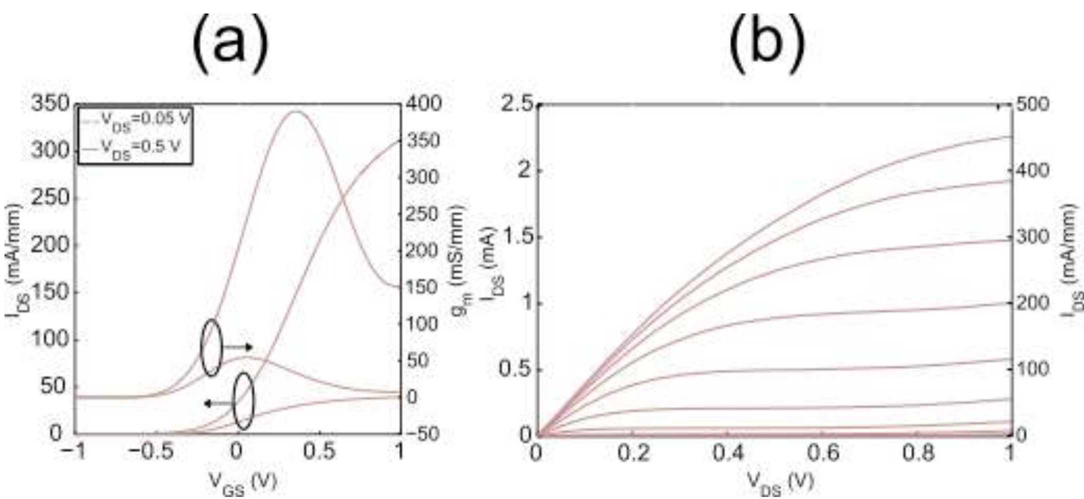
InAs
HSQ
41 nm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(b)
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g_m (mS/mm)
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I_{DS} (mA/mm)
V_{DS} (V)