Thin Film Deposition and Microelectronic and Optoelectronic Device Fabrication and Characterization in Monocrystalline Alpha and Beta Silicon Carbide

ROBERT F. DAVIS, GALINA KELNER, MICHAEL SHUR, FELLOW, IEEE, JOHN W. PALMOUR, AND JOHN A. EDMOND

Invited Paper

The unique thermal and electronic properties of silicon carbide provide multiplicative combinations of attributes which lead to one of the highest figures of merit for any semiconductor material for use in high-power, -speed, -temperature, -frequency and radiation hard applications. Structurally, silicon carbide exists in a host of polytypes, the origins of which are incompletely understood. The continual development of the deposition of silicon carbide thin films and the associated technologies of impurity incorporation, etching, surface chemistry, and electrical contacts have culminated in a host of solid-state devices including field effect transistors capable of operation to 925 K. The results of these several research programs in the United States, Japan and the Soviet Union, and the remaining challenges related to the development of silicon carbide vis a vis microelectronics are presented and discussed in this review.

I. Introduction

In certain close-packed structures such as SiC, there exists a special one-dimensional type polymorphism called polytypism. Polytypes are alike in the two dimensions of the close-packed planes but differ in the stacking sequence in the dimension perpendicular to these planes. In SiC, the stacking sequence of the close-packed planes of covalently bonded primary coordination tetrahedra (either SiC_4 or CSi_4) can be described by the ABC notation. If the pure ABC stacking is repetitive, one obtains the zincblende structure. This is the only cubic SiC polytype and is referred to as 3C or β-SiC, where the 3 refers to the number of planes in the periodic sequence. The hexagonal (ABAB) sequence is also found in SiC. Furthermore, both can also occur in more complex, intermixed forms yielding a wider range of ordered, larger period, stacked hexagonal, or rhombohedral structures of which 6H is the most common. All of these noncubic structures are known collectively as α-SiC.

The extremes in the thermal, mechanical, chemical, and electronic properties of all the common polytypes of SiC allow the types and the numbers of current and conceivable applications of this material to be substantial. From an electronics viewpoint, it possesses a range of wide band gaps [1] at 300 K, e.g., 2.2 eV (3C), 2.86 (6H) and 3.3 eV (2H); as well as high values of saturated electron drift velocity of 2×10^7cm/s (6H) [2] (a slightly higher value has been predicted [3] for 3C (beta) because of reduced phonon scattering); junction breakdown electric field (5×10^6V/cm [4] and thermal conductivity (3.5 W/cm°C at 300 K) [5]. As such, the primary driving forces for the current interest in SiC for electronic applications are its capabilities for high-power, -speed, temperature, and light-emitting devices resistant to radiation damage. Discrete devices having these properties have been achieved and characterized in the laboratory, as described below. Silicon carbide blue-LED's are now commercially available.

The high thermal conductivity of SiC also indicates the potential for high density integration of SiC devices. This idea has received considerable impetus with the recent development and scale-up of the seeded-sublimation growth technique for producing commercially viable single crystal

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R. F. Davis is with the Department of Materials Science and Engineering, North Carolina State University, Raleigh, NC 27695-7907.

G. Kelner is with the Naval Research Laboratory, Washington, DC 20375-5000.

M. Shur is with the Department of Electrical Engineering, University of Virginia, Charlottesville, VA 22903.

J. W. Palmour and J. A. Edmond are with the Cree Research, Inc., Durham, NC 27713.

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a (6H)-SiC boules from which highly thermally conducting wafers are attained. Significant advances have also been made in the growth of monocrystalline beta and alpha (6H) thin films via chemical vapor deposition (CVD) and the incorporation of n- and p-type dopants into these films during deposition or via ion implantation.

Silicon carbide was accidentally discovered by Berzelius [6] in his attempt to produce synthetic diamonds, an ironic twist of fate from the perspective of the current interest in the latter material as a competitor to SiC in the electronics arena (see companion papers on this subject in this issue). Round [7] observed electroluminesce in SiC as early as 1907. The announcement by Lely [8] in 1955 of an unseeded process for producing small single crystals of SiC catalyzed considerable research in the development of optoelectronic and some microelectronic devices in this material. This activity continued on an intermittent basis in the United States and Europe until 1973. The results of these studies may be found in the proceedings of these international conferences [9]–[11] and their bibliographies. By contrast, SiC electronics and crystal growth research continued on a steady and concentrated basis in the Soviet Union, but was often reported in journals not readily available in the West.

The present emphasis in SiC research and development has been driven by the need for operative devices under extreme conditions. Research activity and associated funding were forthcoming following the measurement of the saturated electron drift velocity in the 6H polytype by von Muench [2] and the development by Nishino *et al.* [12], [13] of a method of depositing crack-free, β-SiC films on Si (see the following). A substantial portion of this research through 1985 has been reviewed by Davis *et al.* [14]. The readers should also consult the Proceedings of recent conferences on SiC [15] and wide bandgap materials in general [16]–[18].

This paper reviews the recent advances in this field, especially in the areas of crystal growth, device fabrication and characterization. A special feature is the incorporation of results from the Soviet Union which have not been previously reviewed.

II. Bulk Crystal Growth

Prior to the mid 1950's, SiC was only available from the industrial Acheson process for making abrasive material. However, in 1955 Lely reported [8] the development of a sublimation process for growing higher purity α-SiC single crystals. Evolution of this technique over the next 15 years resulted in a configuration in which a hollow cavity was formed inside a charge of polycrystalline (solid or powder) SiC and lined with a porous graphite tube. The charge was heated by an outer graphite heating element to 2773 K to sublime the SiC which condensed on the slightly cooler parts of the inner graphite cavity as a result of radiation losses at the ends of the SiC. Nucleation was uncontrolled, and the resulting crystals were randomly-sized, hexagonally-shaped platelets. The platelets often exhibited a layered structure of various alpha polytypes with the stacking direction of the atomic planes of these polytypes being along the {0001} directions. Transition regions of random stacking (one-dimensional) disorder occurred between polytypes. Since the bandgaps differ in the polytypes, undesirable (or uncontrollable) heterojunctions were frequently produced within the crystals. Solution growth methods using molten Si or various transition metals were also explored in the mid 1960's [19]–[21]. The resulting crystals were very small, highly twinned beta needles. They exhibited good electrical properties but were unsuitable in size and quality for devices.

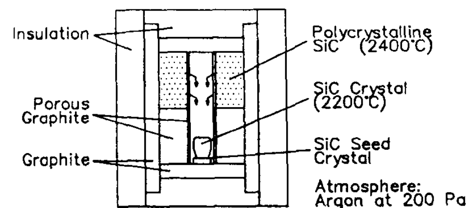


Fig. 1. Schematic of the cross-section of a typical container for the seeded sublimation growth of SiC single crystals [15].

Subsequent research by Tairov, Tsvetkov and coworkers [22]–[24], Ziegler *et al.* [25], and Carter *et al.* [26] have resulted in the implementation of a seeded-growth sublimation process wherein only one large crystal of a single polytype is grown. (In the Soviet literature this technique is often referred to as the LETI method.) The basic elements of this technique are shown in Fig. 1. In this process, nucleation occurs on a SiC seed crystal located at the top or bottom of a cylindrical growth cavity. As in the Lely process, SiC sublimes from a polycrystalline source to form Si, Si_2C and SiC_2 which diffuse through a porous graphite retainer and along carefully programmed thermal and pressure gradients. The primary gaseous species of Si reacts with the graphite walls of the growth cell to form additional Si_2C and SiC_2. Hence, the Si acts as a C transporting agent and plays an active role in the formation of the species impinging on the growing crystal. A complete analysis and discussion of this technique and the associated sublimation phenomena are presented in [22]–[25]. Boules of the pure 6H polytype having diameters $\geq$30 mm and lengths $\geq$40 mm have now been grown by Ziegler *et al.* [25], Carter [27], and Koga *et al.* [28]. Tairov and Tsvetkov [24], Koga *et al.* [29], and Woo and Matsunami [30] have also used this technique to grow complete boules of other alpha polytypes [24] or to deposit 4H on 6H [29], or 6H on 3C [30]. The size of the crystals is limited not by the technique, but by the ability to cut large diameters of this very hard material. The positive results of this research have added impetus to the development of SiC devices and to the research associated with this development, as described below.

III. Thin Film Growth And Characterization

Monocrystalline silicon has been almost universally

adopted as the substrate of choice for the growth of β-SiC thin films because of the availability of silicon in well-characterized and reproducible forms of controlled purity. The reduction of the mismatches in the coefficients of thermal expansion (about 8%) and the lattice parameters (about 20%), via the initial reaction of the Si(100) surface with a carbon-containing gas followed by the successful epitaxial deposition of relatively thick (up to 30 μm), crack-free β-SiC films on this converted layer using individual carbon- and silicon-containing gases has been initially reported by Nishino *et al.* [12], [13] and subsequently employed by numerous groups in the USA and especially Japan (see [15]–[18] for reviews and collected papers describing this research). The process routes and results of the NCSU research are, in general, similar to those of the other groups. As such, they will be described in more detail in the following paragraphs as a representative example of these studies. In all cases the references should be consulted for details regarding this and related research.

The chemical conversion process in our cold wall, vertical barrel reactor uses an optimum amount of C_2H_4 in flowing H_2 which is introduced into the chamber at room temperature (C_3H_8 in H_2 has also been used successfully in various process scenarios by most other groups (e.g., see [31]). The substrates (and the SiC-coated graphite susceptor on which they rest) are rapidly heated to 1600 K over a period of 150 s to produce a very thin, chemically converted layer of monocrystalline β-SiC, as shown by X-ray photoelectron spectroscopy [32]. Microstructural analysis via transmission electron microscopy (TEM) has revealed the layer to be microscopically rough, varying in thickness from 5 to 12 nm. It contains a high density of {111} microtwins and intrinsic stacking faults. In addition, localized regions of the converted layer exhibit disorder [33]. The subsequent CVD growth of β-SiC (100) films on this layer has been achieved at NCSU using SiH_4 and C_2H_4 carried in H_2, a substrate temperature of 1660 K and a total pressure of 1 atm. Growth rates are typically 2 μm/h. For a review of this process and for the results of the analyses of the converted layers and the SiC films, see [32]–[34].

Plan-view and cross-sectional studies of the β-SiC films reveal planar defects on {111} planes. As in the converted layer these defects were identified as microtwins and intrinsic stacking faults. The density of defects is higher at the interface; it decreases over a distance of 3–4 μm from the interface and becomes approximately equal to that at the surface, even for films 20-μm thick.

There are additional defects that appear as bands of mottled contrast that extend from the Si-SiC interface to the growth surface. These defects have been identified as inversion domain boundaries (IDB's (a.k.a. antiphase boundaries)) [35]–[37]. To eliminate these defects, silicon substrates were used with the <100> inclined 2°-4° toward <011> [35], [38], [39]. Films grown on off-axis orientations greater than 2° were similar and much smoother than the on-axis films. This has been verified by profilometry [39] and scanning tunneling microscopy [40]. Recently Shigeta *et al.* [41] and Fujii and coworkers [42] have examined the deposition on Si (111) and expanded the orientation concept to include Si (n11) where n = 3, 4, 5, and 6. Schottky diodes on Si (611), Si (411) and Si (111) were superior to those on Si (100); however devices on vicinal Si (100) were not compared.

Despite the high concentrations of these various defects, considerable work continues to be reported regarding CVD growth on Si. Recently, Shinohara *et al.* [43] reported the exceptional mobility values of 750 and 3000 $cm^2/V \cdot s$ for β-SiC on Si (100) at room temperature and 66 K, respectively. Their work indicated impurity introduction from the SiC-coated susceptor is a likely cause of lower mobilities reported by other workers. In the Soviet Union, Berezhinski *et al.* [44] have also obtained β-SiC on Si (100) having an electron Hall mobility as high as 700 cm^2/Vs and a carrier concentration of $(1–5) \times 10^{17} cm^{-3}$. Furumura *et al.* [45] have succeeded in growing single crystalline β-SiC films at 1273 K on vicinal Si (111) with <111> oriented 4° toward <$\bar{2}$11> using the gases of $SiHCl_3$, C_3H_8 and H_2 at 200 Pa *without* growing an initial buffer layer. A heterojunction diode was also fabricated using a P-doped SiC layer on a p-Si substrate. This diode showed an ideality factor of 1.05.

Spectroscopic and additional electrical (Hall) studies have been conducted on these new cubic (β)-SiC films in laboratories around the world. Choyke *et al.* have conducted low temperature photoluminescence (PL) [46] and Raman scattering [47] studies of the β-SiC films having a thickness range of 60 nm to 25 μm and grown on converted Si (100). In the former study, the "defect related" W band near 2.15eV and the G band near 1.90–1.92 eV dominated the spectra for very thin film samples and are believed to be related to dislocations and extended defects. With an increase in thickness of the β-SiC layers beyond 3 μm, nitrogen-bound exiton (N-BE) emission increased relative to the other bands.

The ratio of the intensities of the band and the N-BE line has been proposed [46] as a figure of merit for crystalline perfection in these types of films. Beyond a thickness of 16 μm, the spectra indicated that further improvement in film quality is dependent on the quality of the substrate and/or the initial nucleation conditions. It was also found that a 1–4 μm transition layer greatly reduced the interface misfit strain. For films thicker than 4 μm the film stress decreased only slightly within an increase of film thickness. This was supported by the Raman data which indicated an in-plane strain of 0.1–0.2% in the thicker films. The biaxial stress state resulted in a reduction of the intensity in the phonon and no-phonon transitions.

The Raman study [47] also showed that the Si 522 cm^{-1} phonon from a Si wafer is enhanced in intensity by a factor of 2–3 due to a CVD overlayer of cubic SiC. Furthermore, the 3C-SiC longitudinal optical phonon from the SiC/Si samples is enhanced by a factor of 2–3 following the removal of the Si substrate. The strict selection rules were no longer obeyed for this sample assembly.

Freitas *et al.* have reported [48] measurements of the temperature dependence of donor-acceptor pair PL spectra

in Al-doped cubic SiC films. By monitoring the thermal quenching of the close nitrogen-aluminum donor-acceptor-pair (DAP) band PL intensity they demonstrated that the thermal activation energy for the nitrogen donors was 54 meV. This value agrees with the results determined from the spectral energy of sharp-line close DAP spectra [49]. In this work they reported both new PL bands which appeared as low-energy shoulders in the zero phonon line (ZPL) and four phonon replicas of the sharp-line nitrogen bound exciton spectra. The intensity of these new lines increased with decreasing C/Si source gas ratio.

Bishop and Freitas [50] investigated the temperature, and the C/Si source gas ratio excitation intensity dependence of the PL spectra in several undoped and lightly Al-doped thin films of cubic SiC deposited on Si (100). The low power spectra in these samples exhibited a band at 1.91 eV, previously labeled as the G-band [46]. The behavior of this PL band with temperature and excitation intensity suggested that the recombination involves a shallow donor (at about 54 meV) and a previously undetected deep-acceptor with binding energy of approximately 470 meV. This interpretation is in agreement with time resolved PL studies carried out on the same samples, which show a range of decay times as expected in processes involving recombination between extended defects. The results from the three different C/Si ratios in the source gas showed an increase of the 470 meV PL band intensity with decreasing source gas ratio. Although this observation is consistent with native defects, it can be explained equally well in terms of a background acceptor impurity whose incorporation is influenced by film stoichiometry. (For a review of the considerable spectroscopic research conducted by Bishop and coworkers on thin films of β-SiC, see [51]).

The CVD β-SiC films grown on Si (100) and vicinal Si (100) have also been extensively characterized via Hall measurements. Segall *et al.* [52]–[53] determined the carrier concentration on unintentionally doped films as a function of temperature (4–300 K). Their detailed analysis revealed the films to be highly compensated ($N_A/N_D > 0.9$). Moreover the donor ionization energies were 13–17 meV, or less than one half the values conventionally reported (40–50 meV) from PL studies (see, e.g., [51] and associated bibliography) and from Hall measurements without the assumption of compensation [54]. Yamanaka *et al.* [55], Suzuki and coworkers [56], [57] and Tachibana *et al.* [58] have conducted similar measurements to 1000 K and also reported heavy compensation. The last authors also conducted the same investigations on vicinal β-SiC (100) deposited on Si (100) with the <100> inclined 3–4° toward <011>. However, similar characteristics were observed. It was concluded that the elimination of the IDB's by this growth technique (see foregoing discussion) did not reduce the level of compensation or change the donor ionization energies.

Segall *et al.* [52], [53] claimed the origin of the shallow donor in the β-SiC films was N; Yamanaka *et al.* [55] suggested that structural defects such as antisite atoms or vacancies behaved as shallow donors and Suzuki and coworkers [56]–[57] considered the origin *unknown.* A related theoretical study of the dominant point defects in β-SiC as a function of composition and the Fermi-level position has been conducted by Wang *et al.* [59]. In the case of n-type, Si-rich β-SiC (which is the usual type of undoped β-SiC) the Si antisite atoms are the dominant defects with the second most abundant defects being the C vacancies. This result supports the Si self-diffusion model involving Si antisite atoms and C vacancies proposed by Birnie [60]. However, the Si antisite atoms are electrically inactive and the C vacancies are double donors. This does not explain the high concentration of compensators in β-SiC films on Si (100) described above.

Additional research to explain the compensation phenomenon has been performed by Carlos *et al.* [61], Freitas *et al.* [48] and Tachibana and coworkers [58]. Carlos *et al.* [61] conducted electron spin resonance (ESR), PL, as well as Hall studies on these films. The ESR (25–200 K) and PL (1.5–120 K) measurements detected only the presence of N as a shallow donor with a binding energy of 53 meV. From their Hall data, they reached similar conclusions as the previous investigators. After examining the PL spectra at 1.5 K, Freitas *et al.* [48] subsequently noted that the donor ionization energy levels of 13–22 meV may come from N if it is spatially inhomogeneously distributed in the film. It should be noted that PL is not applicable for the determination of energy levels which do not undergo a photoemission process. Finally, Tachibana *et al.* [58] conducted Hall measurements to 1000 K on β- and α(6H)-SiC films grown on α(6H) substrates. By contrast, these films were not high compensated (N_A/N_D = 0.36 for β-SiC on α-SiC; = 0.02 for α-SiC on α-SiC, respectively). This research indicates that decreasing the defect density in the film leads to a decrease in the compensation ratio. The donor ionization energies in β- and α- film were 33 meV and 84 meV, respectively. However, these values are still smaller than those for N determined from PL studies (E_D = 54 meV [62], [63] for β- and 170 meV [64] for α-SiC, respectively). Finally, Molnar and Kelner [65] have reported differential Hall studies of epitaxial β-SiC layers grown on Si (100) substrates at four different laboratories. The results were similar for all the samples and demonstrated that the interfacial layer between the substrate and SiC is much more conductive than the bulk of the SiC film. This layer is related to the carbonization of the Si surface prior to the epitaxial growth. The width of the layer varies from 1 to 2 μm for different samples. The carrier concentration increase near the surface is correlated with the defect density determined by SIMS and ESR which revealed an increased nitrogen (donor) concentration in this interfacial region. A 470-meV acceptor was also present in all doped and undoped films. In summary, the evidence to date regarding the origins of the shallow donor and the compensation effect points to N and point defects [66] in the material, respectively. However, the exact nature of the latter is yet to be determined.

The research regarding the deposition of β-SiC on Si (100) has now sufficiently matured such that new deposition

technologies are now being investigated to determine if the film quality can be improved. Fuyuki *et al.* [67] have recently reported atomic layer-by-layer control using gas source molecular beam epitaxy of the deposition of β-SiC within the temperature range 1250–1320 K on β-SiC (100) substrates previously prepared on Si (100) by the two-step CVD process described above. The source gases of Si_2H_6 and C_2H_2 were alternately introduced into a chamber previously evacuated to 3×10^{-10} torr. The RHEED pattern of the surface structure changed from (1×1) to (3×2) when the Si_2H_6 was introduced. However, it returned to the (1x1) structure when the C_2H_6 was introduced. The primary results of this process were 1) the fabrication of single crystalline films having a smooth and mirror-like surface and 2) the determination that the number of Si atoms forming the surface superstructure controls the growth rate of each layer.

Gas-source MBE of β-SiC (111) on Si (111) oriented 4° toward <2$\bar{1}\bar{1}$> has also recently been reported by Sugii *et al.* [68]. In this case the Si surface was initially subjected to a beam of C_2H_2 at 1173 K for 600 s to effect the epitaxial growth of a 1–2 nm layer of SiC, as is the case in CVD. Monocrystalline SiC was subsequently deposited on this layer at 1173 K using beams of C_2H_2 and Si simultaneously. Cross-sectional TEM revealed the layers to be nearly as good as that produced via CVD at higher temperatures. Photostimulated epitaxial deposition of β-SiC on sapphire (α-Al_2O_3) (0001) has been achieved by Nakamatsu and coworkers [69], [70] using an ArF laser, C_2H_2 and Si_2H_6 in the temperature range of 1253–1425 K, and a pressure of 10^{-2}Pa. Wavelengths shorter than 310 nm were effective for epitaxial growth. Similar studies using an Ar laser and CH_3SiCl_3 and $(CH_3)_2SiCl_2$ carried in N_2 or CO_2 have been conducted by Salun *et al.* [71]. The 20–60-m diameter of the beam caused the growth of SiC rods at a rate of 1–70 μm/s depending on the starting compounds and the power density of the laser. Stoichiometric SiC was formed when $(CH_3)_2SiCl_2$ in N_2 was used, but only graphite occurred when CH_3SiCl_3 was used.

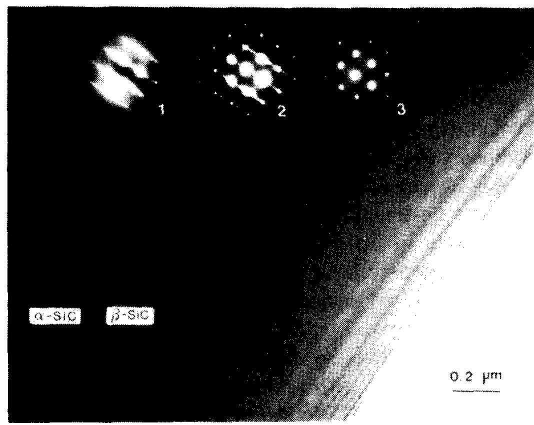
By far the lowest temperature (680–900 K) at which β-SiC has been deposited on Si has been achieved by Chayahara *et al.* [72] using an electron cyclotron resonance (ECR) plasma (ν = 2.45 GHz) discharge in a gas mixture of SiH_4, CH_4 and H_2. The deposited material was oriented polycrystalline with a maximum grain size of 80 nm; however, this or related techniques are being increasingly used to achieve deposition of semiconductors and insulators at low temperature. It is anticipated that it will see additional use for SiC.

The almost universal use of Si has allowed considerable progress in the understanding of thin film growth as well as the additional procedures necessary to produce devices (see the following). However, the mismatches in thermal expansion coefficient and lattice parameter cause considerable problems in device performance because of the extremely high concentrations of the various defects. In an attempt to substantially reduce the concentrations of all defects simultaneously, growth on the Si (0001) and C (000$\bar{1}$) faces of commercial (Acheson-derived) 6H-SiC single crystals substrates has been investigated at NCSU within the temperature range of 1683–1823 K at 1 atm total pressure [73]–[75]. The resulting films were β-SiC (111) at all temperatures studied. Similar research has been conducted by Powell *et al.* [76] using 6H-SiC crystals with the (0001) surface subjected to various polishing, oxidation, and etching treatments.

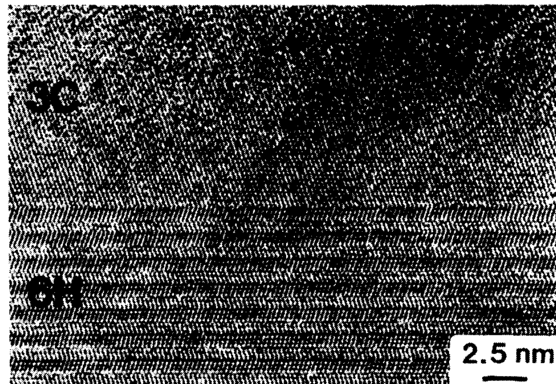
The surfaces of our films grown on (0001) were very smooth and reflective; whereas, those grown on were (000$\bar{1}$) relatively rough and unsuitable for device fabrication. In contrast to films grown on Si substrates, few defects were observed in these films when examined by cross sectional transmission electron microscopy (XTEM) (Fig. 2(a)). In fact, high resolution XTEM shows an abrupt and coherent β-SiC/α-SiC interface (Fig. 2(b)). A single atomic layer runs completely across the interface which indicates that the growth direction of the β-SiC films was exactly [$\bar{1}\bar{1}\bar{1}$] in this region (for the growth of β-SiC on the of the C face α-SiC). However, examination in plan view revealed the presence of double positioning boundaries, (DPB's) on both the Si and C faces, as shown in Fig. 2(c) [74], [75], [77]. In an FCC film, these defects, are caused by the existence of two equivalent sites (e.g., B and C on plane A in conventional crystal stacking notation in the [111] direction) on a (111) or (0001) surface. A nucleus forming from an assembly of atoms on the A sites will be rotated 60° relative to a nucleus growing on the B sites. To release the internal energy many stacking faults are generated from the DPB's, as shown in Fig. 2(c). They either intersect another fault or stop at the partial dislocation which bounds them. When these nuclei grow and meet each other, DPB's are formed between them.

The elimination of the DPB's was achieved by using vicinal α-SiC (0001) crystals lapped such that the [0001] was oriented 3° toward [11$\bar{2}$0] [78]. The prepared substrates were oxidized prior to deposition to eliminate subsurface damage caused by the lapping. Deposition was conducted at 1773 K at 1 atm total pressure. In contrast with the results noted above, all films produced in this manner were a pure 6H polytype, as shown by the identical diffraction patterns shown as insets in the TEM lattice fringe imaging micrograph in Fig. 3, taken from the substrate/film interface region. The horizontal fringes in Fig. 3 are the traces of (0001) planes which can be seen to cross from the substrate into the epilayer without distortion. No line or planar defects were present in the area of this micrograph; in fact, few were observed in the entire XTEM sample. This low defect density was verified by extensive plan-view TEM [78]. More recently, Matsunami and coworkers [79], [80] and Powell *et al.* [81] have reported similar off-axis growth and characterization studies, but without any associated microscopy.

A very different and innovative technique to achieve epitaxial growth of α-SiC films on alpha crystals has been employed for several years in the Soviet Union [82], [83]. Ten to fifty grams of n-type Si having a resistivity of 100–200 Ω·cm are thermally heated to ≈1275K in He such that a conductivity sufficient for levitation is achieved



(a)



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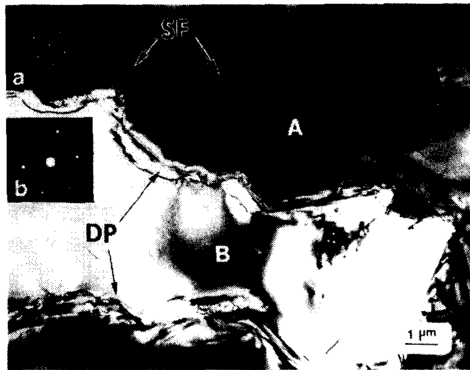


(c)

Fig. 2. XTEM micrographs of the β-SiC (100) - α(6H)-SiC (0001) interface taken at (a) moderate and (b) high resolution. The insets in (a) are selected area diffraction patterns of 1) α(6H)-SiC, 2) the interfacial region between them, and 3) β-SiC. (Micrograph (b) is courtesy of Steve Nutt Brown University, Providence, RI). (c) Plan view of the same film but showing the double positioning boundary and associated stacking faults.

in the electromagnetic field of an inductor with parallel opposite turns (see Fig. 4). The Si is subsequently melted and saturated with C. Aluminum is added if p-type films are desired. The absence of a container for the Si avoids

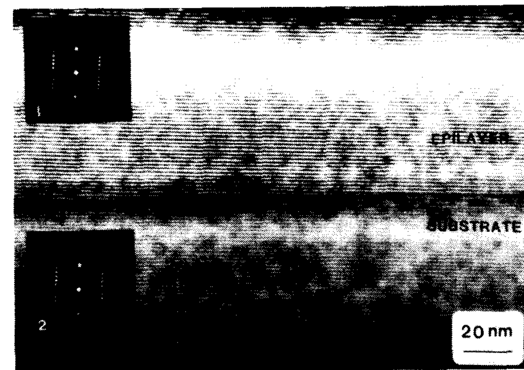


Fig. 3. XTEM micrographs of α(6H)-SiC film on vicinal α(6H) substrate having the [0001] oriented 3° towards [1120].

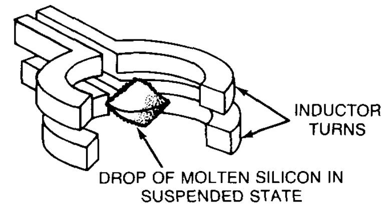


Fig. 4. A schematic of the method of RF heating of molten, C-containing Si in a containerless levitated state developed at the A. F. Ioffe Physicotechnical Institute in Leningrad for the purpose of growing epitaxial films of α-SiC.

such problems as auto-doping from a susceptor which can occur at the high temperatures commonly used for CVD of SiC films. In a typical procedure, α-SiC substrates with <0001> orientation are dipped into the molten solution at 1825–1975 K, the solution cooled at 1–10 K/min to cause supersaturation of C and the deposition of SiC onto the substrate and the film/substrate assembly withdrawn.

IV. Surface Chemistry

The accomplishment of monocrystalline thin films of any semiconductor material automatically sets in motion the research necessary to fabricate devices. As most devices are produced in the surface region of the films, it is important to understand the nature of the surface and the effect of temperature, cleaning procedures, and chemical reactions on the crystallographic structure.

The observations of the SiC surface on an atomic scale were initially reported by van Bommel *et al.* [84]. They described several low energy electron diffraction (LEED) patterns from the Si and C faces of the {0001} planes of the 6H poltype. More importantly they found that the formation of a graphite monolayer occurs on both faces as low as 1175 K under ultrahigh vacuum due to the evaporation of Si and the subsequent collapse of the C of three successive SiC layers. Muehlhoff and coworkers [85] subsequently conducted a more extensive study of the segregation phenomenon on the same surfaces. Between

900–1300 K, the SiC (000$\bar{1}$) surface became enriched in surface C; evidence of graphite formation was also indicated. Above 1300 K, graphite readily formed on both surfaces, but the C-terminated surface graphitized at a higher rate than the Si- terminated surface.

Kaplan has conducted an in-depth study of the composition and structure of the (0001) surface of α(6H)-SiC [86] and the (001) and (111) surfaces of β-SiC [86], [87]. Results for the (0001) and (111) surfaces were indistinguishable. Three distinct phases were observed for these orientations: 3×3, ($\sqrt{3} \times \sqrt{3}$) R30°, and 1×1. The 3×3 was identified with an adsorbed Si bilayer. Nakanishi *et al.* [88] found only the 3×3 and the ($\sqrt{3} \times \sqrt{3}$) R30° on the carbon (000$\bar{1}$) face; off-axis (5°) material showed only the 1×1 structure. Kaplan found the (001) orientation of the β-SiC exhibited five distinct phases: 3×2, c(4×2), 2×1, c(2×2) and 1×1. It was postulated that the c(4×2) and 3×2 structures were caused by ordering of asymmetric dimers. The c(2×2) was produced by altered bonding at the surface and implied that the common dimerization was absent. The (3×2), c(2×2) and (2×1) structures have also been discerned by Dayan [89].

V. Device-Related Studies

A. Metal Surface Reactions and the Development of Contacts

For a semiconductor material to ultimately become the host for electronic devices, numerous related technologies must also develop. For example, one must also achieve good ohmic and Schottky contacts which now implies that a scientific approach be used to understand the chemistry and physics of the contact/semiconductor interface. To this end, several investigators have recently reported results of the reactions of various metals with α(6H)- and β-SiC surfaces. Most studies have employed a combination of Auger, EELS, and LEED to observe changes in the interface region upon the deposition of a given metal on a given surface plane. Bermudez [90] has deposited Pd on the (0001) and (000$\bar{1}$) faces of α(6H)-SiC single crystals previously disordered by Ar^+ ion bombardment during cleaning. He found the interface to be reactive at room temperature with intermixing producing a Pd silicide and dissolved C in the surface region. The Auger results suggested that the local environment of Si in the silicide was that of a mixture of Pd_3Si and Pd_4Si. Annealing to 1073 K caused the evolution from these silicides to Pd_3Si and the most stable phase of Pd_2Si. The unreacted free C accumulated at the interface. Additional research by this author [91] with Al on the same disordered surfaces showed that quasimetallic islands occurred randomly over the SiC surface. Annealing at moderate temperatures ($\leq$873 K) caused aggregation of Al at C-rich sites but with little interfacial reaction. At higher temperatures, Al reacted only with C to form Al_4C_3.

Similar investigations [92] by Bermudez have been conducted using Al and Pt and the ordered β-Si (001) face. In contrast to the deposition on the α-SiC (0001) noted above, Al formed two-dimensional layers in the first few monolayers with Al island formation at higher coverage. Moreover, Al-Si interaction was apparent, but no clear indication of Al carbide formation was found unless the sample was treated to produce a C-rich surface. This suggests that the Al_4C_3 formed on the disordered α-SiC surface occurred via the reaction of Al and C rather than Al and SiC. This is also consistent with the thermodynamic heats of formation of Al_4C_3 and SiC. During annealing of Al on β-SiC(001)–(2×1), LEED showed first (4×1) then c(8×2) structures as the coverage decreased. This can be understood in terms of bonding of Al between alternate (110) rows of Si on the SiC surface. A Schottky barrier height of 1.4 eV was determined. For the somewhat less reactive Pt/β-SiC (001) system, the interface structure appeared to be dominated by the surface diffusion of Pt. A thin Pt layer deposited near room temperature was initially uniform but became heterogeneous during low-temperature anneals as Pt agglomerated into islands. Near 1273 K a reaction occurred forming Pt silicide and releasing free C, as was evidenced by distinct changes both in LEED and in the Si and C Auger line shapes. The deposition of Pt on a SiC surface at 1273 K led to a more uniform layer, since reaction occurred immediately (i.e., before the onset of the diffusion). The silicide layer appeared to be extremely stable at temperatures as high as 1323 K with no interdiffusion of the remaining Pt. However, in the case of deposition on the Si-terminated α-SiC (0001) surface, Pt interdiffused rapidly leading to almost complete disappearance of the Auger signal from an initial Pt layer at T$\leq$1273 K. This demonstrates the difficulty in extrapolating metal/SiC results from one type of SiC lattice to another.

The metal/SiC interface studies have recently become more oriented to finding suitable ohmic and Schottky contacts. Zeller *et al.* [93], and Bellina and Zeller [94] have investigated the interface reactions of nichrome, Ni, Cr, Au/Ta, and Ti deposited onto β-SiC (001). For all metals except nickel, metal carbides were detected at the interfaces combined with the liberation of Si which diffused to the surface. In the case of Ti the amount of liberated Si depended on the relative amounts of both free surface carbon and deposited Ti. Initially these carbides tended to promote adhesion and limit the reaction with the substrate. Annealing at or above 723 K caused nickel to diffuse into the SiC and the Ta and Cr films to migrate through the capping material and away from the SiC. This caused delamination. Nickel adhered well to the β-SiC but at 723 K, it tended to decorate defects on the surface. The Cr and Ta did not diffuse into SiC upon annealing.

Ioannou *et al.* [95] have successfully fabricated Au/β-SiC Schottky barriers via electron beam evaporation. The forward current-voltage characteristics of the as-deposited contacts were exponential over at least six orders of magnitude, the ideality factor was in the range of 1.5±0.2 and the barrier height was approximately 1.2 eV. The forward turn-on voltage was 0.6–1.0 V, and in the reverse direction, soft breakdown occurred in the range 8–10 V. These contacts remained almost unaltered by a 1-h heat treatment at 300°C in argon, and were still rectifying after further

heat treatments at 773 K. However, at 973 K the contacts degraded and showed ohmic behavior. Auger studies of the interface of the as-grown and annealed material showed a gradual outdiffusion of Si which became more prominent at higher temperatures. However, the SiC interface was found to be an effective barrier to Au diffusion into the semiconductor.

Additional Auger studies of Schottky contacts, namely $PtSi_x$ on n-type β-SiC (001) by Papanicolaou *et al.* [96] have shown that short annealing cycles in the 623–1073 K range cause the formation of $PtSi_x$ and PtC at the interface, as shown by the migration of Pt into the SiC. The barrier height increased from 0.95 to 1.35 eV with increasing annealing temperature. The rectifying characteristics improved as a result of a low temperature anneal and remained stable to 1073 K. Waldrop and Grant [97] have used XPS and electrical property measurements to determine the chemistry and electrical properties of Schottky barrier metal (Pd, Au, Co, Ti, Ag, Tb, and Al)/β-SiC (001) interfaces wherein the SiC was terminated by approximately one monolayer of oxygen. They also found the interface to be chemically unreactive at room temperature. The metal contacts exhibited a wide range (0.95–0.16 eV) of barrier heights which depended strongly on the work function of the metal. (For device applications, high work function metals are appropriate for Schottky barrier contacts and low work function metals for ohmic contacts.) Additional efforts regarding Schottky diodes in which there was no associated interface chemistry research are described in Section VI.

B. Impurity Incorporation

In Situ Doping: A limited number of studies have been conducted to investigate the incorporation via CVD techniques of electronically active n-type (N and P) and p-type (B and Al) impurities in β-SiC during thin film growth. Bartlett and Muller [98], Long *et al.* [99] and Nishino *et al.* [13] produced p-type β-SiC by adding B_2H_6 or $AlCl_3$ to this normally n-type (unintentionally doped) material. In addition, von Muench and Pettenpaul [100] doped polycrystalline β-SiC p-type by flowing H_2 through trimethylaluminum (TMA) during crystal growth via the van Arkel process.

Figure 5 shows the results of the experimental SIMS measurements by Kim and Davis [101] of atomic dopant concentration as a function of the partial pressure of the dopant source gases for N, P, Al, and B. The linear character of both the curve for Al and the sections of the graphs for P, B, and N at lower pressures is predicted from considerations of Henry's law.

Solubility data from direct measurements such as diffusion or lattice parameter studies are not available in the literature for the various dopants for the temperature of 1633 K used for the CVD growth. However, the change in slope of the atomic concentration curves for P, B, and N, as well as the changes in the surface character and the X-ray Laue patterns of these heavily doped samples relative to the undoped (or lightly doped) materials indicate the onset of polycrystallinity. These changes are believed to be triggered by the introduction of the various dopants in excess of their solubility limits. Furthermore, the grain boundaries can act as sinks for excess dopant and thus allow continued incorporation of these species at levels significantly higher than allowed by the lattice. The maximum in the Al concentration could not be determined because of increased gas phase nucleation and the resultant occurrence of poor films at high TMA input.

The carrier concentrations of each dopant were also found to be a linear function of the partial pressure of the dopant source when plotted on a log-log scale, as shown in Fig. 5. Each figure also reveals a major difference between the atomic concentration and the carrier concentration for each dopant. The reasons for this include the measured deep energy levels for the p-type dopants of Al (0.24 eV) and B (0.735 eV) as well as the possibility of compensation from unintentionally introduced n-type dopants (e.g., N). Other possibilities include i) compensation from line or point defects and/or trapping of impurities at the dislocations and stacking faults in the material, ii) dopant-Si and/or dopant-C interaction, and iii) location in nonelectrically active interstitial sites (especially plausible for B). Thus a portion of each of the dopants is either ionized on nonelectrically active sites or complexes with Si or C. Combinations of these events are also probable.

Ion Implantation: As alternatives to *in situ* doping, diffusion and ion implantation provide means of controllably introducing impurities into semiconductor materials. In SiC, diffusion processes require both temperatures greater than 2273 K and relatively long times to accomplish the mass transport required for device fabrication. Under these conditions, masking oxide layers, essential for selective doping, vaporize and SiC decomposition occurs. Therefore, a more viable solution is ion implantation.

The Group IIIA elements of B, Al, Ga, In and Tl; the Group VA elements of N, P, Sb, and Bi, as well as Be, have also been implanted into 6H α-SiC single crystals in research directly related to microelectronics (Leith *et al.* [102], Dunlap and Marsh [103], Marsh and Dunlap [104], Addamiano *et al.* [105], Marsh [106], Burdel *et al.* [107], Vodakov *et al.* [108], Violin *et al.* [109] and Kalinina *et al.* [110]). Burdel *et al.* [111] have used an eximer laser to heat (SiC does not melt at 1 atm) the implanted amorphous SiC and to recrystallize this near-surface layer. Functional p-n junctions have been successfully produced by Leith *et al.* [102], Dunlap and Marsh [104], Marsh and Dunlap [105], Addamiano *et al.* [105] and Marsh [106] via implantation of Group VA elements into in situ doped p-type layers. By contrast, the implantation of the Group IIIA elements into n-type 6H-SiC has almost always resulted in high resistivity layers but not p-type conduction [106]; the two exceptions are the implantation of Al reported by Kalinina *et al.* [110] and Violin *et al.* [112]. Boron implantation [112] as well as that of Sc and Be [113] produced only partial compensation of the n-type conductivity. Implantation into β-SiC has been conducted, by investigators at North Carolina State University [114]–[117] and Case Western Reserve University [118], these studies are described as follows.

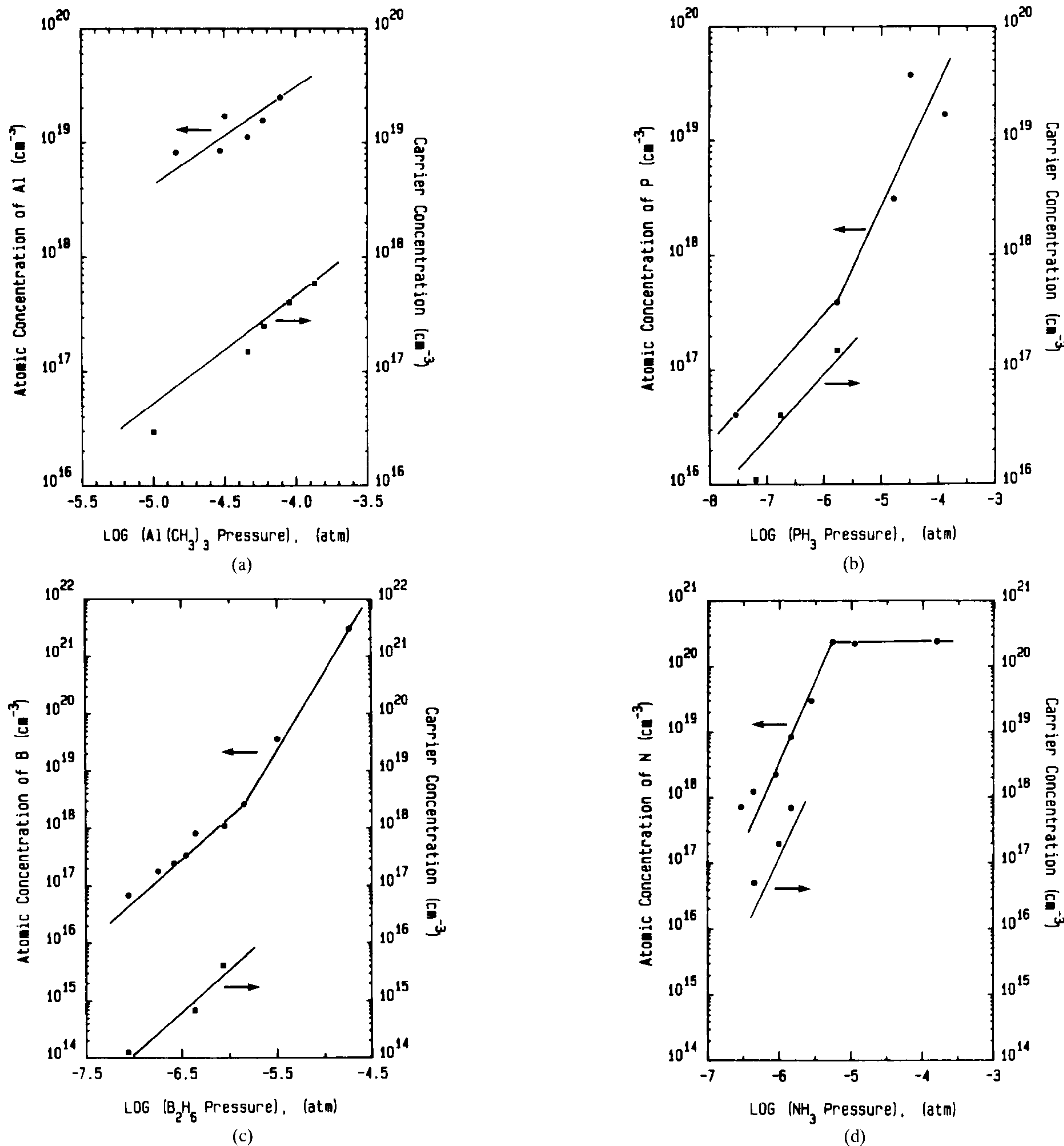


Fig. 5. Atomic and carrier concentrations of (a) aluminum, (b) phosphorus, (c) boron, and (d) nitrogen in β-SiC as a function of the partial pressure of reactant doping gas during CVD growth.

Ryu *et al.* [114] obtained a buried amorphous layer via dual B implant under liquid N_2 conditions using the doses and (energies) of 2×10^{15} cm^{-2} (200 keV) and 1.5×10^{15} cm^{-2} (100 keV) and an offset angle of 7° from the sample surface to ameliorate channeling. This layer extended from 0.1 to 0.44 μm into the film. Annealing at 1763 K for 300 s caused solid-phase epitaxial (SPE) regrowth of the layer from both crystalline/amorphous interfaces. Two distinct bands of B-containing precipitates, corresponding in position to the maxima in the two implant peaks also occurred. No out-diffusion of B was detected as a result of this heat treatment. Annealing at 1873 K (but not lower temperatures) caused the formation of defect clusters at about 0.06 μm from the amorphous/crystalline interfaces and near the center of the original amorphous layer. Profiling of the B concentration in the 1873 K annealed sample via secondary ion mass spectroscopy (SIMS) showed remnants of the implant peaks, although diffusion of the B from the original implanted peaks had obviously occurred. Virtually perfect SPE regrowth, without visible damage, occurred during annealing at 2073 K for 300 s. However, SIMS analysis revealed that essentially all the B had diffused away.

A dual implant of Al at 298 K by Edmond *et al.* [115], [116] using the doses and (energies) of 9×10^{14} cm^{-2} (190 keV) and 6×10^{14} cm^{-2} (110 keV) also produced a

buried amorphous layer with a 10 nm crystalline surface, an amorphous depth of 0.17 m and damage to 0.22 μm. Annealing at 1873 K for 300 s caused SPE regrowth, but the regrown layer contained many defect clusters. A dense band of clusters occurred at a depth from 0.04 to 0.11 μm. When annealed at 2073 K (instead of 1873 K) for 300 s, the number of defect clusters were reduced. In this case, SIMS showed a decrease in the concentration of Al by a factor of 2 to 4 throughout most of the profile depth; however, it was slightly increased at the sample surface.

The dual implantation of N by Ryu *et al.* [114] under liquid N_2 conditions using a range of doses ((0.9–1.5) $10^{14}cm^{-2}$) and energies (90–200 keV) produced a heavily damaged but crystalline layer. Annealing of the sample above 1573 K caused structural rearrangement. No visible damage was observed. Annealing at 1873 or 2073 K for 300 s caused considerable out-diffusion of N which resulted in a high concentration of this species in the near-surface region.

The effect of ion implantation at room temperature versus liquid N_2 conditions on the extent of amorphization in β-SiC may be seen by the efforts of Edmond *et al.* [115] with P using the same dose and energy of 1×10^{15} cm^{-2} and 110 keV, respectively. The 298 K sample had a 10 nm crystalline surface, an amorphous depth of 0.13 μm and visible damage to 0.23 μm. The LN implant created a thinner crystalline cap ($\sim$5 nm), an amorphous depth of 0.17 μm and visible damage to 0.35 μm. Annealing studies by Edmond *et al.* [116] at 1973 K for 300 s using samples containing a dual implant of P (220 keV, 1×10^{15} cm^{-2}, and 110 keV, 6×10^{14} cm^{-2}) revealed that the buried amorphous layer became saturated in P causing the layer to regrow in a polycrystalline microstructure after the first 100 nm. Even in this latter region, many small precipitates and loops were observed.

The implantation research of Avila *et al.* [118] had as its principal objective the fabrication of p-n junctions via the introduction of B or Al into the n-type ((1.8–3.8) $\times$ 10^{17} cm^{-3} β-SiC films. Triple implants of B (4, 6, and 10 $\times$ 10^{14} cm^{-2} at 30, 50, and 100 keV, respectively) and double implants of Al (7 and 10 $\times$ 10^{14} cm^{-2} at 100 and 200 keV, respectively) were produced at 923 K and the samples annealed at 1638 K for 1800 s in Ar. The implant profile was unaffected by the annealing. The current-voltage characteristics of the Al-implanted structures showed little rectification. The B-implanted diodes exhibited rectification with ideality factors of 2.2 and higher, breakdown voltages of 5–10 V and a series resistance of 20 KΩ.

As described above, little success has been achieved in affecting precipitate and/or damage-free SPE regrowth in β-SiC films previously amorphized by ion implantation. In addition, no pronounced changes in the electrical properties of any of these films occurred until anneal temperatures equal to or in excess of 1673 K were employed. As such, high-temperature implantation was studied (see Edmond, *et al.* [117]) to surmount some of these problems. For example, implantation of Al or N at 623, 823 and, especially, 1023 K using doses and energies similar to those used at room and liquid N_2 temperatures allowed sufficient *in situ* annealing during implantation to produce both essentially damage-free implant regions as well as virtually complete electrical activation of the implanted species. The backscattering spectra from the 1023 K implants nearly coincided with the aligned spectrum of the unimplanted material. In addition, cross-sectional TEM analysis revealed that implantation at the highest temperature resulted in neither visible lattice damage nor precipitates obtained from the anneals of the low temperature implants. Finally, it should be noted that a slight increase in the electrical activation of the high-temperature implants can be achieved if the samples are annealed at 1473 K for 1800 s; however, this is far below the temperatures needed for processing the samples implanted under 298 K or LN conditions.

C. Dry Etching

In order to characterize electrically the β-SiC films via p-n junction measurements, as well as fabricate certain devices, a method of selective, controllable etching is needed. However, SiC is an extremely inert material that can only be conveniently etched by molten salts or Cl_2 or H_2 gases at high temperatures (see Appendix A in [11]). Therefore, dry etching techniques using fluorinated gases have been investigated. Previous experiments of this type on β-SiC thin films have all used CF_4 and CF_4 + O_2 mixtures in a variety of modes, including reactive ion beam etching [119], plasma etching [120], and reactive ion etching (RIE) [121]. These techniques and the various parameters employed in their use did not result in etched surfaces sufficiently smooth for devices. A more recent effort by Palmour *et al.* [122] has shown that for reactive ion etching of β-SiC, the choice of cathode material plays a major role in the chemical and physical characteristics of the etched surface. Anodized Al cathodes were found to cause micromasking of the SiC during etching, as shown by the detection of this element on the etched surface and the presence of surface roughness. The degree of roughness also depended on the choice of fluorinated gas, with the faster etching NF_3 causing more roughness than CF_4 employed under the same conditions. The use of the Al cathode also caused accumulation of F in both gases used, allowing it to polymerize with the C on the SiC surface. The use of a C cathode coverplate ameliorated the micromasking problem, allowed anisotropic patterns to be produced and left a smooth and chemically clean surface, with little or no fluorocarbon polymerization. This decrease in roughness was especially true with the C cathode/NF_3 combination. Plasma etching in SF_6 caused crystallographically spiked formations but left a very clean surface that actually had less native oxide than unetched β-SiC.

More recently, Pan and Steckl [123] have conducted an in-depth study of the RIE of RF-sputtered SiC films on Si (100) substrates which were subsequently annealed at 1373 K in N_2 for 0.5 h. The resulting films were polycrystalline. The fluorinated gases of SF_6, $CBrF_3$ and CHF_3 mixed with O_2 and an Al mask were employed. The SiC etch rate was believed to be controlled by a combination of physical (dc bias) and chemical (fluorine and oxygen concentration)

mechanisms. A critical dc bias separated the two regimes. Good anisotropic profiles were obtained using CHF_3/90% O_2 and SF_6/35% O_2 plasmas. These conditions also allowed selective SiC to Si etching.

VI. Device Fabrication And Characterization

Operable SiC devices have been successfully fabricated in α-SiC in previous concentrated efforts to develop this material as a semiconductor (for an overview of this earlier work see [124]). However, the devices were produced in Lely crystals, the character of which was not reproducible from run-to-run, as described above. This coupled with a sharp downturn in funding delayed the evolution of devices in this material. A review of device research and characterization in β- and α-SiC materials conducted in the last five years is discussed in the following two subsections. Where possible, the reader should consult the indicated references for a more complete account of the research.

A. Beta-Silicon Carbide Devices

Yoshida *et al.* [125] have produced Schottky-barrier diodes on unintentionally doped films grown on Si (100) with nickel and gold as the ohmic and rectifying contacts, respectively. The barrier height, as determined by capacitance and photoresponse measurements, was 1.15±0.15 and 1.11±0.03 eV, respectively.

Beta-SiC films in the (111) orientation have also been used to fabricate Schottky diodes. The Au diodes fabricated by Furukawa *et al.* [126] showed excellent rectification with reverse leakage currents of $\approx 5\ \mu$A (1.1×10^{-3} A/cm^2) at -5 V and 250 μA (5.5×10^{-2} A/cm^2) at -10 V. The ideality factor was 1.4–1.6, and the Schottky barrier height was determined to be 0.9–1.1 eV. These investigators also examined the effects of different (n11) orientations of the β-SiC films (n=1, 3, 4, 5, and 6) and compared these results with Au and Pt diodes produced on Si (100) [42]. Additional aspects of this work are also referred to above and in [14] and [17]. The 0.75-nm diodes on Si (611), (411), and (111) showed excellent characteristics relative to those on (100); namely smaller reverse leakage currents, ideality factors near unity and larger barrier heights. Relatively poorer characteristics were found in devices on (311) and (511). As expected, the barrier height of the Pt diode was higher (1.69 eV) for this larger work function metal than for Au (e.g., 1.4 eV for the (611) oriented material).

Suzuki and coworkers [127], [128] have fabricated β-SiC (100) p-n junction diodes having a mesa structure and determined their electrical character to 773 K. No significant chemical degradation was observed at any temperature. At room temperature, the device had a forward turn-on voltage of about 1.2 V and a reverse leakage current of 5 μA at 5 V. However, both parameters seriously degraded with an increase in temperature. The curves of forward current density versus voltage contained three distinct regions at all temperatures which indicated the following: 1) excess currents at applied voltages lower than about 0.6 V; 2) exponentially increasing currents at 0.6–1.1 V; 3) gradually increasing currents at voltages greater than 1.1 V.

Yoshida *et al.* have also fabricated metal/semiconductor (Schottky-barrier) field-effect transistors (MESFET's) by the successive CVD of aluminum-doped (1×10^{17} cm^{-3}), p-type and undoped, n-type ((3–$7)\times10^{16}$ cm^{-3}) β-SiC layers on p-type silicon substrates [129]. Gold and aluminum electrodes were used for the Schottky-barrier gate and for the ohmic (source and drain) contacts, respectively, for the n-type SiC. Gate voltages (V_G) from 1.0 to 0.6 V were applied. A high channel resistance and a small drain current (I_D=10 μA) indicated that the leakage current (I_L) through both the SiC p-n junction (used for isolation of the device region from the silicon substrate) and through the isolation grooves, was significant compared with the current through the n channel. A transconductance at saturation of about 0.09 mS/mm^{-1} and a threshold voltage of about 1.4 V were reported. Daimon *et al.* [130] and Yoshida *et al.* [131] have also investigated the effect of heating to 573 K and 673 K [130] on the operation of a MESFET similar to that just described but one which had the aluminum layer replaced by a layer containing boron and a different configuration of electrodes. Gold and aluminum were again used for the contacts. The effective channel length and width in both cases were 20 and 500 μm, respectively. At 298 K the I_L was considerably reduced in this sample relative to that in the aluminum doped material. The gate voltages necessary to achieve nominal pinch-off of the devices ranged from -1.6 V to -4 V. Saturation was observed in both cases. In the devices taken to 473 K, a maximum transconductance of 0.5 mS/mm was reported at room temperature. In the improved devices taken to 573 K, the value was 1.1 mS/mm at the same temperature. In both cases, increasing the temperature resulted in a decrease in both soft-breakdown voltages and transconductances. A considerable increase in leakage current was also noted. The devices did not saturate at the highest temperatures of operation. The causes of these changes were postulated to be interrelated in that, in the deep depletion mode, the current flow was through the boron-doped layers in which the resistivity was reduced by the increased thermal energy. Conversely, in the enhancement mode, the drain current was reduced by a decrease in the electron mobility with temperature. The drain current versus voltage characteristics were unchanged after heating the sample to 573 K in air.

Simultaneous research at NCSU by Kong *et al.* [132] and Kelner and coworkers [133] has also resulted in operable MESFET's. These devices were produced in a 300–600-nm thick undoped, n-type β-SiC film epitaxially deposited on a buried 7-μm thick aluminum-doped p-type β-SiC layer previously grown on p-type silicon. The latter layer was used to confine the current to a thin, n-type active layer and to move this active layer away from the defect region which extended about 3 μm from the Si-SiC interface. The carrier concentrations of the n- and p-type layers were both 5×10^{16} cm^{-3}. The sample was subsequently oxidized in flowing dry oxygen at 1373 K for 7.2×10^3 s to grow a 46-nm thick SiO_2 layer to passivate the as-grown surface. A three-level

mask set employing concentric ring geometry was used wherein the gate pattern completely enclosed the central 100 m (drain) contact. The gate length and the source-to-drain distance were 3.5 μm and 10.5 μm, respectively. Sputtered $TaSi_2$ was used as the ohmic contacts for both the source and the drain. These contacts were annealed in a vacuum at 1173 K for 300 s to minimize contact resistance. Thermally evaporated gold was used as the gate rectifying contact. Very good drain-current saturation was achieved as the drain voltage (V_D) increased. The maximum transconductance in the saturated region was 1.6 mS/mm. The threshold voltage was -1.4V. For a V_G less than -2 V, the drain current was virtually independent of the gate voltage, and thus the device could not be fully turned off. The details of the fabrication and the electrical character are provided in [132]. In the research conducted by Kelner *et al.* [133], the carrier concentration of the p-type layer was $(1\text{–}2)\times10^{17}\text{cm}^{-3}$. The gate length and width of the devices were 5 μm and 210μm, respectively, with a source-drain distance of 8 μm. Modulation of the n-type channel current was achieved with an Au Schottky barrier gate. A maximum transconductance of 2.3 mS/mm was obtained. However, the device could not be completely pinched off and displayed a high output conductance due to leakage current in the p-type layer.

Furukawa and coworkers [134] and Kelner *et al.* [133], [135] have fabricated junction-gate (J)FET's using two different structures. That of the former authors consisted of a B-doped, p-layer, an undoped n-layer and an Al-doped top layer on Si (100). The B-containing layer was used under the n-channel to reduce the leakage current through the p-layer. The source and drain regions were reactively ion etched into the n-layer using CF_4 and O_2. The gate length and width were 20 μm and 1.0 mm, respectively. Clear FET characteristics were obtained, but saturation did not occur. The maximum transconductance was in 20 μS/mm.

Kelner *et al.* produced a buried JFET in $\approx$1.2 μm, n-type β-SiC layers deposited both on p-type Si (100) [133], [135] and p-type α-SiC (0001) substrates [136]. A cross-sectional view of the device is shown in Fig. 6. The gate width and source-to-drain distances were 200 μm and 4 μm, respectively. Electrical isolation of the n-type channel was achieved using reactive ion etching with an SF_6 plasma which removed $\approx$1.5 μm of SiC. The measured I_D–V_D curves for the device in material deposited on SiC are shown in Fig. 7. The device showed limited saturation at $V_{DS}\approx8$ V and pinch-off at approximately -10 volts. The maximum measured transconductance was $\approx$20 mS/mm. Analysis of the data using a charge control model showed the effective field-effect mobility ($\approx$560 cm^2/V·s) to be close to the measured Hall mobility ($\approx$470 cm^2/V·s) and the saturated electron drift velocity (V·s) in the channel to be close to the predicted value of 2×10^7 cm/s. The I_D–V_D characteristics of buried JFET's having different gate lengths were also determined. The measured and calculated (V_g=0) values of transconductance as a function of reciprocal gate length are shown in Figs. 8(a), (b). A comparison of the two graphs shows the measured values

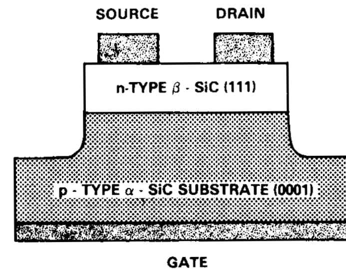


Fig. 6. Cross-sectional schematic of a buried gate junction field effect transistor in β-SiC developed by Kelner *et al.* [136].

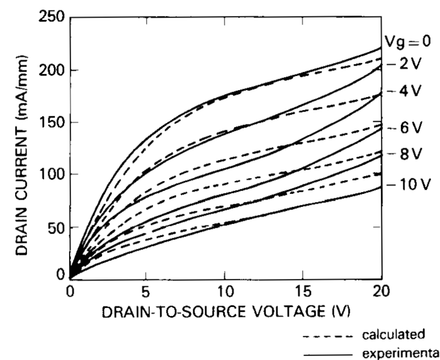


Fig. 7. (a) Measured and (b) calculated room temperature drain current (I_D) versus drain voltage (V_D) characteristics of the buried gate JFET shown in Fig. 6. The parameters used in the calculation were V_{bi} = 2.5 V = 565 cm^2/V·s, v_s = 2×10^7 cm/s,L = 4 μm, d = 1 μm, N_d =2×10^{16} cm^{-3}, ϵ= 9.72 and R_{sh} = 0.32 Ω·mm.

of transconductance to scale with gate length as expected from the calculations. Moreover, the assumption of V_S = 2 $\times$ 10^7 cm/s in the model appears to be supported by the similarity in experimental data. Further improvements in the performance of this device may be obtained by reducing the channel length and optimizing the channel thickness as well as controlling the doping levels. As can be seen from Fig. 8(b), the predicted values of the transconductance for the device with a thin channel (*d*=0.3 m) having a length=1 μm are above 100 mS/mm. Cut-off frequencies as high as 5 GHz may also be achieved.

Shibahara *et al.* [137], Fuma *et al.* [138], and Palmour and coworkers [139] have produced working, enhancement mode (normally off) metal/oxide/semiconductor field effect transistors (MOSFET's) on β-SiC (100) films. The MOS-FET reported by Shibahara *et al.* [137] was fabricated in boron-doped p-type SiC (about 7-m thick and with a carrier concentration of about 1 $\times$ 10^{17} cm^{-3}) with the source and drain formed by ion implantation of P^+ and subsequent annealing at 1353 K for 3.6 $\times$ 10^3 s. The I_L between the source and gate was less than 1 μA for a gate bias of ±10 V. Fuma *et al.* [138] produced their MOSFET device in an n-p-n structure deposited on a p-Si substrate. The p-type dopant was obtained from B_2H_6. A mesa structure was produced using reactive ion etching. Aluminum, annealed at 725 K, served as the source and drain contacts. The

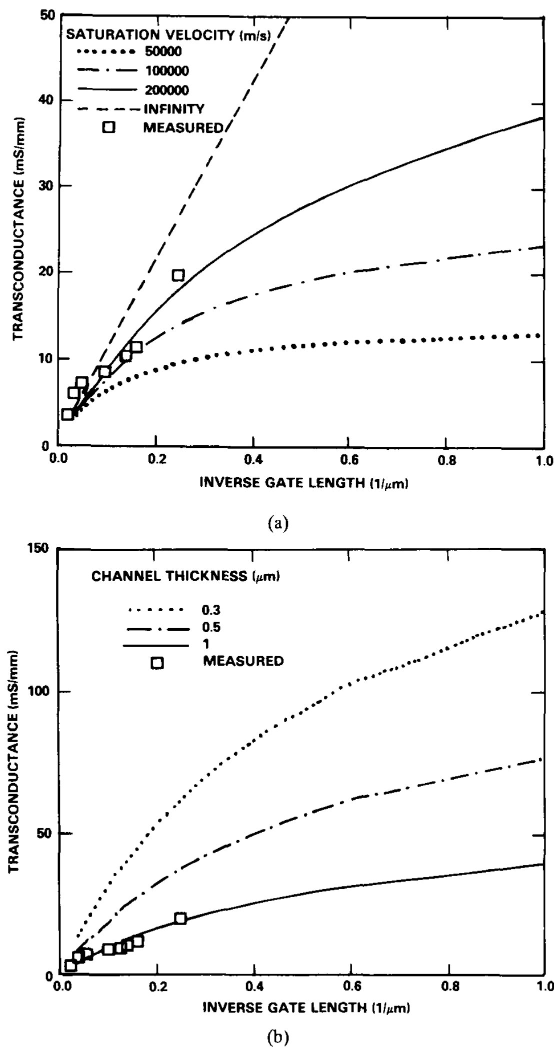


Fig. 8. Transconductance of buried gate β-SiC JFET versus reciprocal gate length: (a) transconductance computed for different values of versus and measured data, (b) transconductance computed for channel thicknesses d=1 m, 0.5 m, 0.3 m, and measured data. Parameters used in the calculation: V_{bi} = 2.5 V = 565 cm^2/Vs, versus = 2×10^7 cm/s, V_{po} = 18.7 V, e = 9.72, R_{sh} (ϵmm) = 0.08 (L(μm)).

drain current tended to saturate at room temperature. The maximum transconductance was 200 μS/mm. These characteristics degraded considerably above 473 K. The devices fabricated by Palmour *et al.* [139] used a p-layer (Al-doped) deposited on n-type Si into which a dual N implant (peak concentration = 5×10^{19} and 3.4×10^{19} cm^{-3}) was produced at 873 K. Phosphorus-doped polysilicon acted as the implant mask and as a self-aligned gate. $TaSi_2$ was used for the contacts. The gate length in this work and that of Fuma *et al.* [138] described above was 20 m. The devices [139] showed good saturation at room temperature and could be pinched off using a V_G of −4 V (V_D = 5 V). The maximum transconductance was 0.335 mS/mm. The devices showed good stability to 673 K; however the I_L increased from 10 μA (298 K) to 80 μA (673 K).

Depletion-mode (normally on) MOSFET's have been fabricated by Kondo *et al.* [140], Furukawa *et al.* [134] and Palmour and coworkers [139], [141]. Kondo's team produced their device on an undoped, n-type SiC layer grown on an aluminum-doped, p-type layer previously deposited on a p-type (40–60·cm) silicon substrate. Polysilicon combined with aluminum metallization was used for the source and drain contacts. Considerable leakage current through the p-type layer was evident, as the I_D did not saturate even at V_D more negative than −12 V. The devices produced by Furukawa *et al.* [134] (and referred to as insulated-gate FET's) were similar to those of Kondo *et al.* [140] except that the final p-layer was doped with B because of the better rectifying characteristics of undoped/B-doped p-n junctions. Depletion character was evident but the devices did not saturate nor could they be turned off. The maximum transconductance was 40 μS/mm.

Palmour *et al.* [139], [141] have produced devices with markedly improved performance. These devices were fabricated in n-type (undoped) layers on p-type (Al-doped) layers on α-SiC substrates. The materials for the gate and the contacts were the same as those for the enhancement-mode devices described above. The N^+ source and drain areas were subsequently formed via dual N^+ implants at 773 K. As shown in Fig. 9, the devices showed very stable drain current saturation to a V_D of 30 V. The maximum transconductance at 298 K at 20 V was 5.32 mS/mm. The most notable attribute of these devices was that the excellent drain character changed only slightly to 923 K, the highest temperature at which any FET has been reported to operate. The transconductance increased to 11.9 mS/mm at 673 K but decreased slightly at higher temperatures. Raising the temperature to 973 K caused the gate oxide to experience breakdown.

Finally, one of the most recent and novel devices incorporating β-SiC layers is the β-SiC/Si heterojunction bipolar transistor (HBT) fabricated by Sugii and coworkers [142], [143]. Phosphorous-doped SiC (the emitter) was initially grown epitaxially on n-type (111) Si substrates. Reactive ion etching removed this layer except for the 250 μm^2 emitter area, and B ions were implanted through the remaining and previously oxidized assembly to form the base region. Sputtered Ni was used for the emitter and base electrodes, and Al was evaporated to form the collector electrode. A schematic of this process and the transistor characteristics are shown in Figs. 10(a), (b). A common-emitter current gain of 800 was attained in the low collection current region. The 1.1 value of the ideality factor of the base current suggests that the diffusion current is dominant. Although the devices exhibited a punch through problem, it did not strongly affect the results. Surprisingly, the large number of misfit dislocations at the SiC/Si interface were ineffective as recombination centers and thus did not deteriorate the character of the HBT.

B. Alpha Silicon Carbide Devices

Some of the first electronic devices fabricated in this new era of α-SiC bulk crystals and films have been fabricated

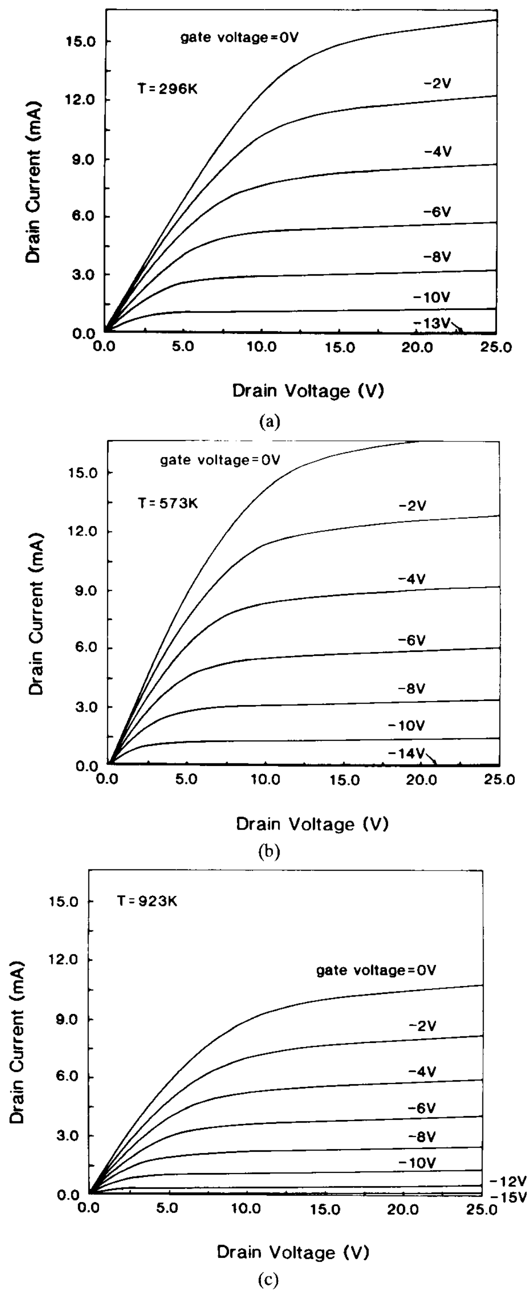


Fig. 9. Drain characteristics of a depletion mode n-channel MOSFET in a β-SiC (111) thin film grown on an α(6H)-SiC (0001) substrate and studied at (a) 296 K, (b) 573 K, and (c) 923 K. The gate length and width of this device were 7.2 μm and 390 μm, respectively.

by Dmitriev *et al.* [82], [83], [144], [145], and Anikin *et al.* [146]. All devices were produced by the container-free liquid phase epitaxial process described above. These investigators initially produced both n^+-n-p^+ and n^+-n-p-p^+ structures on n^+ substrates [82]. These diodes were made using chromium for ohmic contacts to the n-type region and aluminum for ohmic contacts to p-type regions.

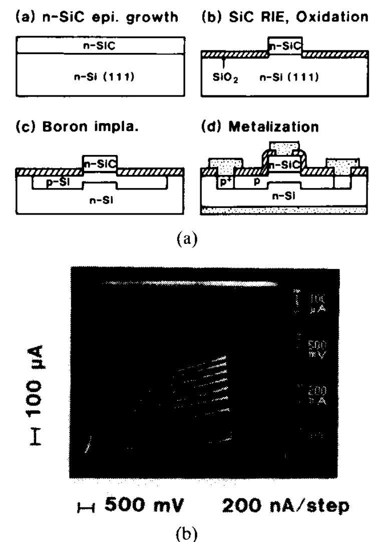


Fig. 10. (a) A schematic of the fabrication procedure for producing a heterojunction bipolar transistor in β-SiC (100) grown on Si (100) and (b) the associated transistor characteristics [142].

The effective donor concentration in the n-region was N_d-N_a = 5×10^{17} to 10^{18} cm^{-3}. The effective acceptor concentration in the p-region was N_a-N_d = 2×10^{18} to 10^{19} cm^{-3} (estimated from the breakdown voltage of point contacts). The critical field of the avalanche breakdown was approximately 1.5×10^6 V/cm. The diode ideality factors range from 1.76 to 1.96. The diode saturation current density was in the range 10^{-14} to 10^{-19} A/cm^2 for a 300-μm diameter diode. The diode cut-in voltage of 2.7 V. Subsequently, better quality diodes of the same types with breakdown fields in the range of (2–3) $\times$ 10^6 V/cm, ideality factors of 1.7 and a saturation current density of 10^{-19} A/cm^2 were grown by investigators in this same group [83] on 4H-SiC Lely substrates. Silicon carbide tunnel diodes were also produced by Dmitriev and his coworkers [144] at about the same time as those noted previously.

Dmitriev and his collaborators have subsequently reported the fabrication on 6H-SiC of a long channel (20 μm gate length) JFET with a buried gate [145]. In the temperature range from 23 K to 773 K, the transconductance varied from 0.25 to 0.5 mS/mm. The maximum value was obtained at 563 K. Subsequently, Anikin *et al.* [146] reported the fabrication of a similar device in 6H-SiC, but with a gate length and width of 10 μm and 400 μm, respectively. Improved performance was achieved including excellent saturation in the I-V characteristics. Other room temperature properties included a maximum drain current of 20 mA at V_{GS} = 2 V and V_{DS} = 40 V, a drain-gate breakdown voltage V_{DGB} of approximately 90 V, a transconductance of 7 mS/mm at V_{GS} = 2 V and V_{DS} = 40 V, and a gate leakage current of 5 $\times$ 10^{-9} A at V_{DS} = 5 V and V_{GS} = 85 V. More recently, Kelner *et al.* [147] have also reported the fabrication and evaluation of α-SiC buried gave JFET's similar in design to those described in [145]

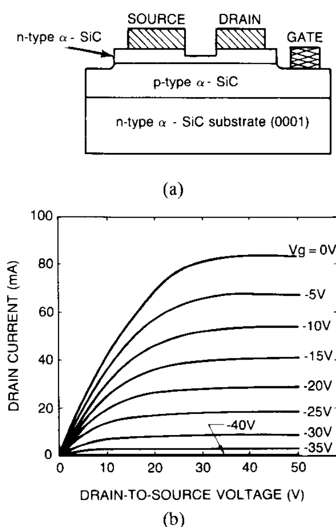


Fig. 11. (a) A schematic of the material structure of a buried-gate JFET in alpha-SiC [147]. (b) Room temperature drain current versus drain voltage ($I_D - V_D$) characteristics of a buried-gate JFET with a four micron gate length. [147].

and [146]. The structure of the device is shown in Fig. 11(a). The substrate and individual layers were produced at Cree Research, Inc. Devices were fabricated with gate widths of 185 and 240 μm and source-to-drain spacings in the range of 4 to 40 μm. The source and drain contacts were electron evaporated Ni. Thermally evaporated Al was used to contact the p-type gate. The channel between the source and the drain contacts was etched to a thickness of approximately 0.3 μm by using $CF_4 + O_2$ reactive ion etching. The current-voltage characteristics of the α-SiC JFET with a 4-μm gate length are shown in Fig. 11(b). The device displayed good saturation characteristics and was completely pinched-off at a gate voltage of -40 V. This device had a maximum transconductance of 71 mS/mm and 1 drain saturation current of 0 V gate voltage of 450 mA/mm. The I-V characteristics for the devices with a 39-μm gate length were measured at temperatures of 297, 543, and 673 K (Fig. 12(a)). Device transconductance dropped with an increase in temperature due to the decrease in the electron mobility. Figure 12(b) shows the temperature dependence of this mobility calculated from the measured values of the device transconductance and drain conductance at low drain voltages and temperature dependent Hall mobilities measured in independent studies [58], [148]. All three mobility curves are in agreement, thus we conclude that the decreasing the transconductance with increasing temperature is strongly related to the decrease in mobility.

Additionally, Dmitriev *et al.* [149] and Vainshtein *et al.* [150] (also in the same group as Dmitriev) have fabricated the first α-SiC dynistors (also known as Shockley diodes). The acceptor concentration in the substrates was $\approx 10^{19}$ cm^{-3}. The initial, unintentionally doped epitaxial layer ($\approx$ 1-μm thick) had the effective donor concentration of approximately 5×10^{17} cm^{-3}. After the growth of this first layer, Al was added to the melt, and the second p-type epitaxial layer ($\approx$ 1.5 μm) was doped n-type with nitrogen ($N_d - N_a \approx 10^{19}$ cm^{-3}). All contacts were made from Al. These structures showed the following features: the turn-on time constant varied from 1 ns to 10 ns; static switching voltage of 10–50 V; inverse voltage to 90 V, switching time of 10–40 ns and recovery time of 150–200 ns.

Additional device efforts in the Soviet Union include a p^+-π-n^+ double injection SiC structure fabricated by Litvin *et al.* [113] using ion implantation. They observed a negative differential resistance related to the filling of the traps in the π layer. This device is the first SiC analog of a p-i-n structure. Anikin *et al.* [151] and Chelnokov [152], [153] have also described α-SiC tunnel diodes and voltage limiters. The former had a peak-to-valley ratio of 2.5 at 300 K with peak currents between 0.01 and 2 mA and peak voltages between 0.2 and 0.4 V. Negative resistance in these diodes was observed to 800 K. The voltage limiters operated from 2.7 to 170 V for different devices. Maximum currents exceeded 20 A with a maximum operating temperature of 820 K.

More recently, a concentrated effort to develop devices in α-SiC has been conducted at Cree Research, Inc. by two of the authors (JWP and JAE). This work is reported here for the first time and thus is presented in greater detail. Figure 13 shows the linear I-V characteristics of a p-n junction diode. A peak inverse voltage of 455 V was reached whereupon avalanche breakdown occurred. The breakdown initially occurred at $\sim$420 V with a reverse I_L of 4 μA, increasing to 50 μA at 450 V. Thereafter the device operated in avalanche with current increasing linearly with voltage. The value of the ideality factor in forward bias was between 1.6–2.0 thus indicating a compromise between diffusion current and generation-recombination dominated processes. Heating the diode to 625 K (Fig. 13(b)) caused 1) a decrease in the turn-on voltage from $\approx$2.4 V to $\approx$2.0 V, due to a reduction in bandgap, and thus an increase in the intrinsic carrier concentration, and 2) a slight increase in the prebreakdown leakage current due to new thermally generated carriers. Otherwise the graphs were identical. Similar diodes fabricated at the Ioffe Institute [152] had forward currents to 8 A with forward voltages less than 4V (decreasing to 2.5 V at 800 K), breakdown voltages to 350 V with a reverse current at 293 K of 10^{-9} A. The maximum operating temperature was 820 K (however, more recently reported data [151] indicates that some diodes have operated to 1050 K).

The average power/area as a function of time required to cause p-n junction failure has also been determined by the Cree investigators. The inherent power pulse resistance of SiC-based electronics has long been a predicted benefit. According to Wunsch and Bell [154], the principle mechanisms of semiconductor junction failure when subjected to an electromagnetic induced power pulse are: 1) surface breakdown around the junction, and 2) internal breakdown through the junction within the body of the device. The problem of surface breakdown has received extensive design consideration and many junctions exhibit

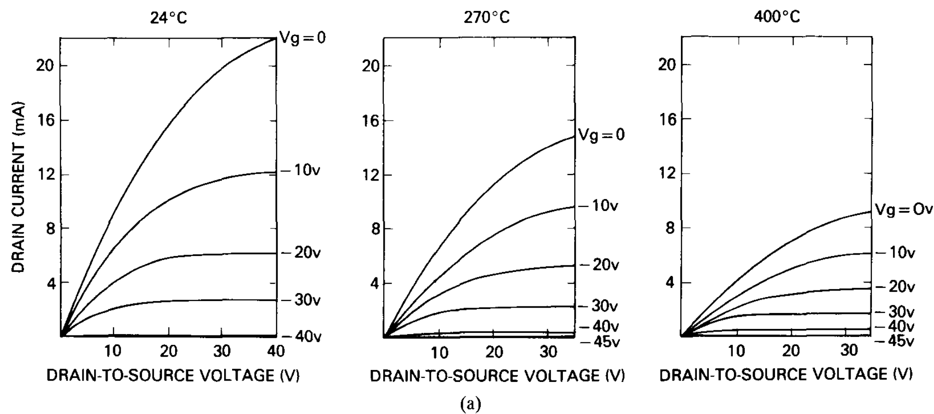


Fig. 12(a). Current-voltage characteristics and of a buried-gate JFET having the same material structure as shown in Fig. 11(a) but with a 39 micron gate length.

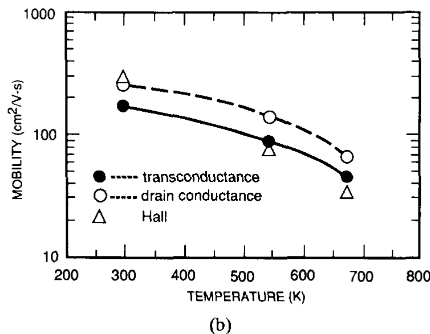


Fig. 12 (b). Temperature dependence of the electron mobility of the same device and deduced from the measured values of the device transconductance and drain conductance and the temperature dependent Hall mobilities measured in independent studies [58], [147]. Data for both (a) and (b) were acquired at 297 K, 543 K, and 673 K [146].

body breakdown prior to surface breakdown. In internal body breakdown, the destructive mechanism usually results from changes in the junction parameters due to the high temperatures locally within the junction area. Therefore, the theoretical treatment of the problem can be reduced to a thermal analysis. The theory is valid whenever high transient voltages appear in a circuit whether the pulse origin is electromagnetic or transient from within the circuit itself. For SiC, the theoretical limit, following the analysis by Wunsch and Bell [154] is:

$$P/A_{\text{avg}} = 9810t^{-1/2} \ \ (\text{kW/cm}^2) \tag{1}$$

where P is the power; A, the junction area; and t, the time. With regard to the theoretical limit, SiC devices should be ~5.4 times more resistant to electromagnetic radiation effects than silicon. This advantage increases to ~17.5 times when comparing the theoretical and experimentally determined expressions for these two materials, respectively. This is because Si devices fail at levels below the theoretical value for P/A due to "hot spot" punch through.

In this research, 6H-SiC diodes with a 60V PIV rating were tested at≈ 1.5 μs, ≈ 10–20 μs and 100 μs pulses. As shown in Fig. 14, averaging the results of the data, one obtains an experimental expression for power pulsing toughness of SiC diodes:

$$P/A_{\text{avg}} = 1805t^{0.63} \ \ (\text{kW/cm}^2). \tag{2}$$

This is an improvement over silicon devices by a factor of 1.8–3.2 in the pulse times tested (1.5–100 μs). However, it is still a factor of 5.4–9.9 below the theoretical limit (in the same pulse time range) for SiC. For this reason, it is postulated that the principle mechanism of failure for the present devices is not localized melting SiC at the junction, but rather breakdown of the junction passivation layer.

In addition to its high operating temperature and resistance to power pulses, 6H-SiC p-n junction rectifiers have an extremely fast switching speed. The minority carrier lifetime in SiC is ≈10 ns. Therefore, these ultrafast diodes feature speeds in the 10–20 ns range while operating at high temperature with low leakage current. Figure 15 illustrates the reverse recovery time for a typical 6H-SiC diode (PIV 50–700 V) operating at RT. At 623 K, the recovery time increased slightly (≈20%). Unlike any other rectifier commercially available today, SiC rectifiers provide the collective combination of high voltage, high speed and high tolerance to transient surges at high temperature.

Although the capabilities of the SiC p-n junction diodes are outstanding for high temperature, high speed applications, the one disadvantage to these is the higher built-in voltage. To overcome the problem of a high forward voltage drop, at least in low reverse voltage applications, SiC Schottky diodes have been fabricated by Cree Research, Inc. investigators. Theoretically, these should provide the same high speed and high temperature operation of the SiC p-n junction diodes, but with about half of their built-in voltage. Experimental devices exhibited a built-in voltage of just 1.1 V, yet were able to withstand reverse-bias voltages of up to 60 V at temperatures as high as 673 K.

Figure 16(a) shows the I-V characteristics of a typical 6H-SiC Schottky diode at room temperature. As shown, the leakage current of this device is 20 μA at −60 V. The ideality factor is very close to unity, ranging from 1.11–1.15.

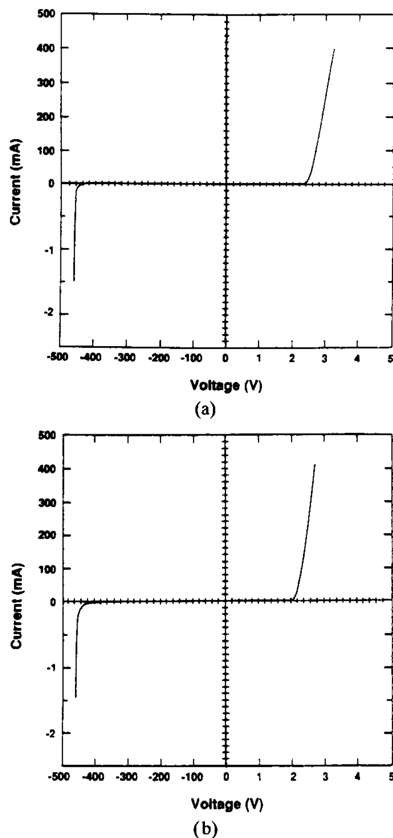


Fig. 13. I-V characteristics of a p-n junction diode fabricated in an α(6H)-SiC film deposited on a vicinal 6H (0001) substrate and obtained at (a) 293 K and (b) 625 K.

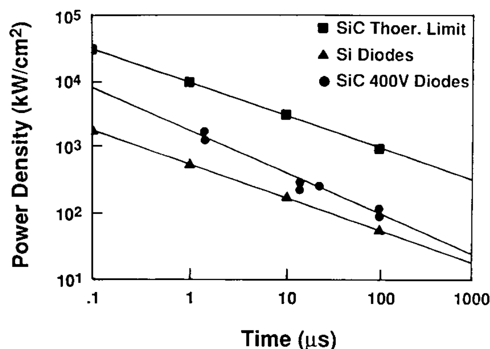


Fig. 14. Average power per unit area as a function of time required to cause junction failure in 6H-SiC and Si diodes.

When heated to elevated temperatures, the leakage current of the diodes increases (Fig. 16 (b)), but the increase is marginal in comparison to the leakage current increase typically observed in silicon Schottky diodes when heated to only 373 K. Above 373 K, the leakage current in Si Schottky diodes makes them virtually useless, but analogous SiC diodes retain very good characteristics. The leakage current at a reverse bias of 60 V increases to only 350 μA.

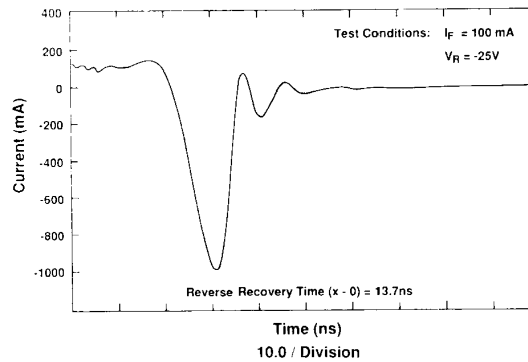
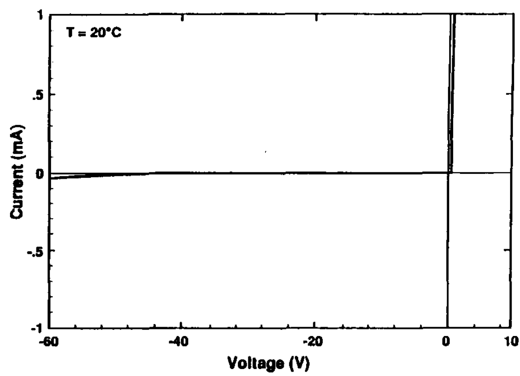


Fig. 15. Switching speed (reverse recovery time) of high-voltage (1200 V) α(6H)-SiC p-n junction diode at 293 K. Test conditions were I_F = 100 mA and V_R = −25 V.

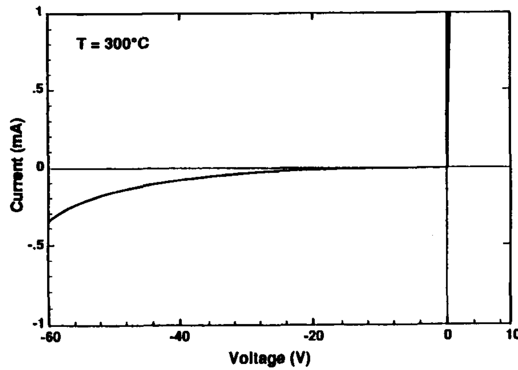
Reverse recovery times of experimental SiC Schottky devices at room temperature are in the range of 4 ns, which is comparable to their silicon counterparts. This is to be expected since the speed of any Schottky diode depends primarily on the simple capacitances of the semiconductor interfaces and not on minority carrier lifetimes. It should be noted that the reverse recovery time of SiC Schottky diodes increases only slightly as the temperature rises; it is 5.3 ns at 623 K.

As a result of the Schottky diode results discussed previously, research on 6H-SiC MESFET's was performed. The material structure and the device characteristics of one of these MESFET's are shown in Figs. 17 and 18, respectively. This device had a gate length of 10 μm, a gate width of 1 mm, and a source to drain distance of 30 μm. At room temperature (293 K) the device showed very good current saturation to a drain voltage (V_D of 40 V, as shown in Fig. 18(a). The maximum transconductance was 2.1 mS/mm with a pinch-off voltage of V_G = 1.85 V. The subthreshold leakage current was quite low, having a value of 60 nA at V_D = 40 V and a gate voltage (V_G) of −2.5 V. The MESFET's continued to operate well when heated to 473 K, as shown in Fig. 18(b). The maximum transconductance decreased to 1.35 mS/mm, but the current saturation remained was very good to V_D = 40 V. The substhreshold leakage current increased to 125 nA at V_D = 40 V and V_G = −2.5 V. The I-V characteristics at 623 K are shown in Fig. 18(c). The subthreshold leakage increased to 3.6 μA at V_D = 40 V and V_G = −1.85 V throughout the measured temperature range. These devices continued to operate well at temperatures up to 773 K.

The material structure and the device I-V characteristics of a 10-μm channel length 6H-SiC inversion-mode MOSFET are shown in Figs. 19 and 20, respectively. Very good current saturation was obtained at room temperature to a V_D = 30 V. A maximum transconductance of 0.27 mS/mm was observed at V_G = 24 V. The threshold voltage was very high, about V_G = 90 V. It is apparent from the high threshold voltage and the relatively low transconductance that the SiC is either filling fast interface states or going



(a)



(b)

Fig. 16. I-V characteristics of an α(6H)-SiC Schottky diode at (a) 293 K and (b) 573 K.

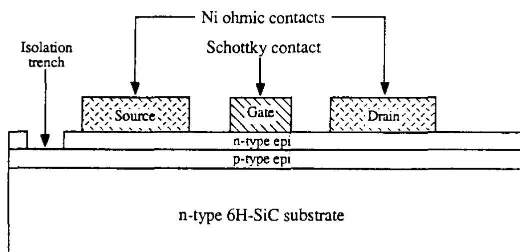
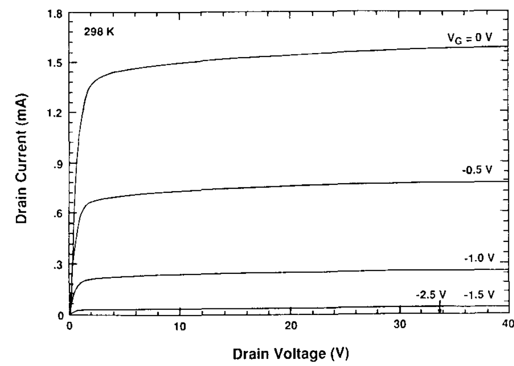
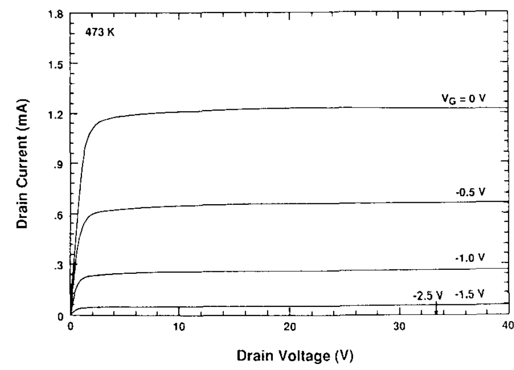


Fig. 17. Material structure of a 6H-SiC MESFET fabricated at Cree Research, Inc.

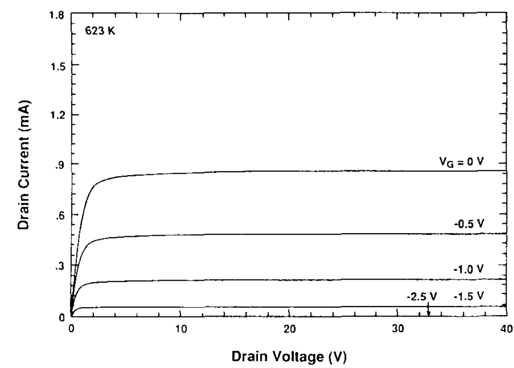
into deep depletion before it is able to form an inversion layer. An increase in temperature caused an increase in the maximum transconductance to 0.9 mS/mm at drain and gate voltages of 30 V and 24 V, respectively. The threshold voltage also decreased from 9 V to 3.8 V. This trand continued with further increases in temperature to 673 K. Under the same bias conditions, the transconductance again increased to 1.03 mS/mm, and the threshold voltage decreased to 0.25 V. Because of the high transconductance, the lower threshold voltage and a relatively low leakage current, it is obvious that this device operated better at 673 K than at room temperature. This device continued to operate very well to 923 K. The leakage current was 2 μA at



(a)



(b)



(c)

Fig. 18. Drain current-voltage characteristics of the SiC MESFET shown in Fig. 17 at (a) 298 K, (b) 473 K, and (c) 673 K.

V_D = 25 V and V_G = 0 V. The maximum transconductance at 923 K was 0.43 mS/mm at V_G = 6 V.

SiC has attracted much interest as a material for visible light emitting diodes (LED's), since different colors of photoluminescence may be produced depending on polytypes and impurities. Since red, orange, yellow and green LED's are well developed using GaP, GaAsP and GaAlAs at present, much attention is given to blue LED's of 6H-SiC for diagnostics/analytical equipment and digital color printing and imaging systems. Blue LED's of n-type SiC with Al and N on p-type SiC with Al have been prepared by Brander and Sutton [155] using liquid phase epitaxy with

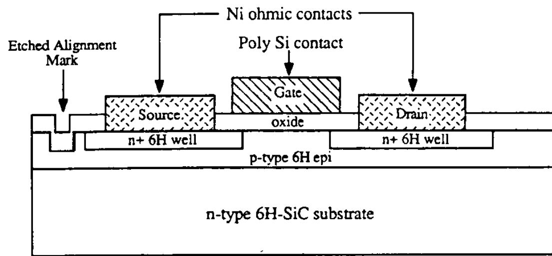


Fig. 19. Material structure of a 6H-SiC MOSFET fabricated at Cree Research, Inc.

a Si melt in a graphite crucible. A brightness of 100 fL at room temperature was reported with no failure for longer than 15 000 h over the temperature range between room temperature and 673 K.

Extensive and more recent research on these devices has also been conducted in Germany by Ziegler *et al.* [25] and Hoffmann *et al.* [156] and in Japan by Suzuki *et al.* [157], Matsunami *et al.* [158], Ikeda *et al.* [159], Matsunami [160] and Koga *et al.* [29]. These investigators have prepared Al/N p-n junctions in 6H-SiC using either the combination of a Si solution contained in a graphite crucible, a rotating dipping method (see Suzuki *et al.* [157] and Ikeda *et al.* [159]) and resulting sequential double epitaxial growth, or double epitaxial growth via CVD. In the former, after p-layer growth in the Si melt doped with Al was achieved, n-layer growth was conducted by introducing N_2 gas into the growth chamber.

The light emission mechanism was investigated through the detailed analyses of temperature and excitation dependences of the spectra and time-resolved spectral change for various SiC LED's emitting different colors. As shown by Ikeda *et al.* [159], the main mechanisms are attributed to i) donor-acceptor (D-A) pair recombination (~480 nm), ii) bound exciton recombination at localized centers related to Al impurities (~455 nm) and iii) free exciton recombination ~425 nm). Since the intensity of the ~425-nm peak increases with an increase in current, the component of short wavelength emission increases and hence the total brightness does not show saturation. If the content of N in n-type SiC is reduced, the main emission peak at ~480 nm shifts to the shorter wavelength side (~460 nm) owing to the lower contribution of D-A pair recombination. The external quantum efficiency of SiC blue LED's prepared by LPE growth using 6H-SiC substrates grown by the Lely sublimation method has been reported by Matsunami *et al.* [160] to be in the range of $2\times10^{-3}\%$. Recent increases in efficiency using transparent substrates produced by the seeded sublimation method have achieved a value of $2\times10^{-2}\%$.

Blue emitting LED's having a 470 nm peak wavelength at 20 mA have also been recently developed at Cree Research, Inc. These diodes feature a 5 V maximum reverse voltage with a typical forward voltage, radiant flux and spectral halfwidth (at this writing) at 20 mA of 3 V, 8.0 μW and 70 nm, respectively.

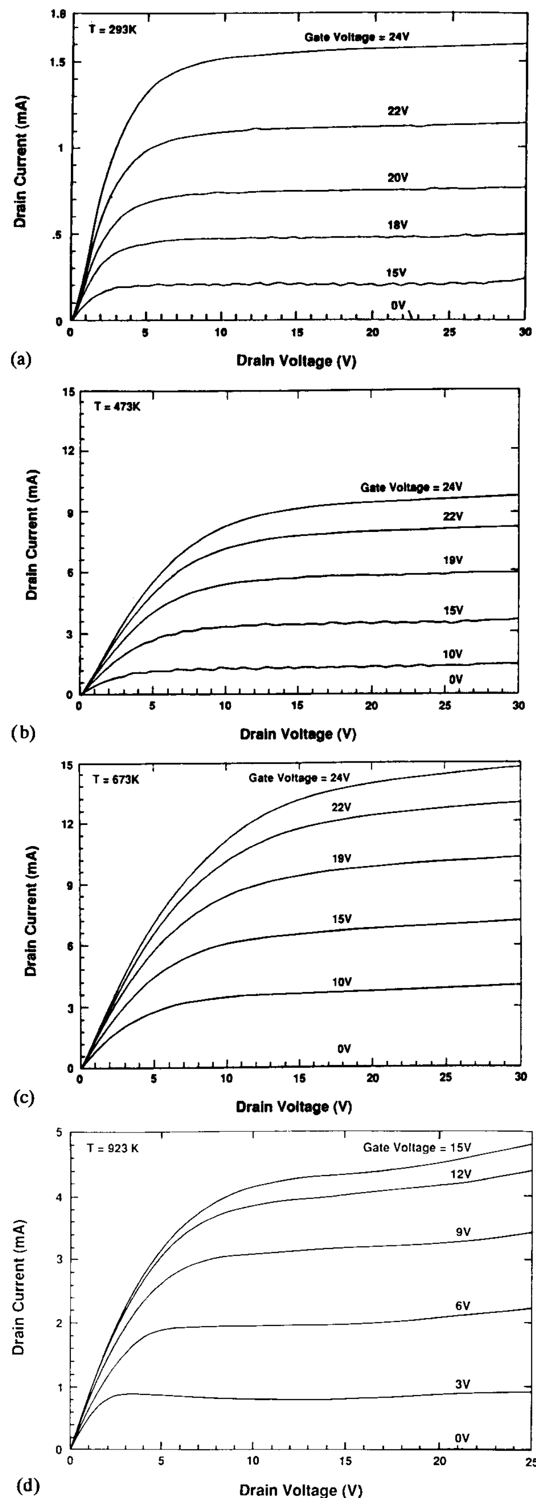


Fig. 20. Drain current-voltage characteristics of an n-channel, inversion-mode MOSFET shown in Fig. 19 at (a) 296 K, (b) 473 K, (c) 673 K, (d) 923 K.

The large bandgap of SiC and the several n- and p-type dopants which can be incorporated also make it a

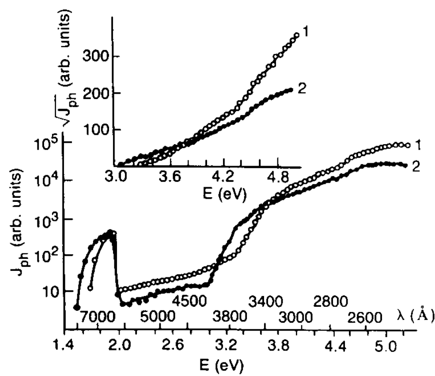


Fig. 21. Short-circuit photocurrent spectra of Schottky barriers for 4H (open dots) and 6H (solid dots) SiC polytypes [168].

suitable material for LED's with wavelengths outside the blue portion of the spectrum. Dimitriev *et al.* [161]–[163] and Vishnevskaya *et al.* [164] in the Soviet Union have produced green, blue and violet LED's. Yellow LED's have been fabricated by Kholuyanov and Vodakov [165] via implantation of β into n-type (N-doped) a (6H)-SiC. The electroluminescence maximum was at 580 nm. Green LED's have also been fabricated by implanting B into 4H polytype, n-type SiC [165]. Doping with Sc in 4H shifted the electroluminescence peak to 520 nm. The quantum yield of this latter polytype is 0.5×10^{-4} at 293 K.

Dmitriev *et al.* [167] have also produced a three color blue (470 nm) green (510 nm) red (650 nm)) SiC single crystal display using epitaxial films grown on a (6H) substrates by the containerless method noted above at 1775 K. The p-regions were produced by ion implantation with subsequent annealing at 2073 for 5 min. The diameter of each diode was 300–500 μm with the distance between emitters of 300 μm.

Finally, Schottky diodes fabricated in both 6H and 4H polytypes have been used for ultraviolet photodetectors [168]. A semitransparent layer of Cr was used as a Schottky contact. The diffusion length of the generated light holes was estimated to be 0.1–0.3 μm. The short-circuit photocurrent spectra of the Schottky barriers for the 4H and 6H-SiC materials are compared in Fig. 21. Glasow *et al.* [169] have also produced photodiodes by N implantation into p-type 6H-SiC. Maximum quantum efficiencies of $\sim$75% were observed around 280 nm; however, the diodes were sensitive in the wavelength range of 250–450 nm.

VII. Summary

Monocrystalline thin films of high purity β-SiC have been grown directly on Si (100) and α-SiC (0001). Problems derived primarily from interface related defects and subboundaries in the material have prevented the optimization of the quality of the films. However, deposition on these materials oriented 2°–4° off-axis allows the elimination of the IDB's in the material grown on Si (100) and the DPB's in the material deposited on SiC (0001); the latter resulting combination of α-SiC on α-SiC appears especially viable for device commercial fabrication. In addition, considerable progress in the understanding of the surface science, ohmic and Schottky contacts and dry etching have recently been made. The combination of these advances has allowed continual improvement in Schottky diode, p-n junciton, MESFET, MOSFET, HBT, and LED devices.

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Robert F. Davis, for a photograph and biography please see page 597 of this issue.

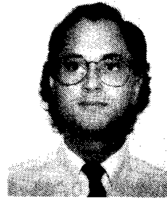
Galina Kelner (Member, IEEE) received the B.S. degree in chemistry in 1956 and the M.S. degree in chemistry in 1958 from the Moscow Mendeleev Institute of Chemical Technology.

In 1959, she joined the Moscow Cathode-Ray Tubes Institute where she worked on the synthesis of various luminescent materials. In 1976, she joined the Research Triangle Institute, Raleigh, NC, where she worked on the growth and characterization of III-V compounds. Since 1980, she had been with the Naval Research Laboratory, Electronics Science and Technology Division. Her current research interests are in characterization and fabrication of SiC devices.

Michael Shur (Fellow, IEEE) received the M.S.E.E. degree (with honors) from Leningrad Electrotechnical Institute in 1965 and the Ph.D. degree in physics from A. F. Ioffe Institute of Physics and Technology in 1967.

From 1965 to 1976 he was with A. F. Ioffe Institute of Physics and Technology. In 1976 he joined the Department of Electrical Engineering of Wayne State University, Detroit, MI. In 1978 he was with the School of Engineering of Oakland University, Rochester, MI. Between 1976 and 1980 he had visiting summer appointments with the School of Electrical Engineering of Cornell University, Ithaca, NY. In the summer of 1979 he was a visiting faculty at IBM T. J. Watson Research Center. From 1979 to 1989 he was with the University of Minnesota. Since 1989, he has been a John Marshall Money Professor of electrical engineering at the University of Virginia. His research has included ferroelectrics, amorphous semiconductors, solar cells, ballistic transport, high speed semiconductor devices, and integrated circuits. He has published several books, including a book on GaAs devices published by Plenum in 1987 and a book on physics of semiconductor devices (with microcomputer programs) published by Prentice Hall in 1990.

Dr. Shur is a member of American Physical Society, a member and a Secretary of the National Chapter of Commission D of the International Union of Radio Science, a member of Electromagnetic Academy, an Associate Editor of the IEEE Transactions on Electron Devices, a member of the Editorial Board of the International Journal of High Speed Electronics, and one of the Contributing Editors of Review of Radio Science, 1990 (published by UNESCO).



John W. Palmour received both the B.S. and the Ph.D. degrees from North Carolina State University, the latter in February 1988. His major was in materials science and engineering, with a minor in electrical engineering.

Since his graduation, he has been a Senior Scientist at Cree Research, Inc., concentrating on device processing techniques and transistor development in SiC. He is a cofounder of Cree Research, Inc., which formed in July of 1987. He has 24 publications and 5 patents concerning semiconducting SiC.

John A. Edmond received the B.S. degree in ceramic engineering from Alfred University, NY and the Ph.D. degree from North Carolina State University, Raleigh, in materials science and engineering, with a minor in electrical engineering.

Since his graduation in September of 1987, he has been a senior scientist at Cree Research, Inc., concentrating on the development of p-n junction diodes and blue LED's and device processing techniques. He is a cofounder of Cree Research, Inc. He has 25 publications and 5 patents concerning semiconducting SiC.