Three-D DWT of Efficient Architecture

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Abstract--- In this paper, the digital data can be transformed using Discrete Wavelet Transform. The images need to be transformed without loosing of information. The Discrete Wavelet Transform was based on time-scale representation, which provides efficient multi-resolution. The lifting based scheme (5, 3) filters give lossless mode of information as per the JPEG 2000 Standard. The lifting based DWT are lower computational complexity and reduced memory requirements. Since Conventional convolution based DWT is area and power hungry which can be overcome by using the lifting based scheme. The DWT is being increasingly used for image coding. This is due to the fact that DWT supports features like progressive image transmission (by quality, by resolution), ease of transformed image manipulation, region of interest coding, etc. DWT has traditionally been implemented by convolution. Such an implementation demands both a large number of computations and a large storage features that are not desirable for either high-speed or low-power applications. Recently, a liftingbased scheme that often requires far fewer computations has been proposed for the DWT. In this paper, the design of Lossless 2-D DWT using Lifting Scheme Architecture will be modeled using the Verilog HDL and its functionality were verified using the Modelsim tool and can be synthesized using the Xilinx tool.

Keywords--- Fourier Transform (FT), Short Time FT (STFT), Discrete Wavelet Transform (STFT), Multi-resolution Analysis (MRA).

I. INTRODUCTION

THE fundamental idea behind wavelets is to analyze according to scale. Indeed, some researchers in the wavelet field feel that, by using wavelets, one is adopting a perspective in processing data. Wavelets are functions that satisfy certain mathematical requirements and are used in representing data or other functions. This idea is not new. Approximation using superposition of functions has existed since the early 1800's, when Joseph Fourier discovered that he could superpose sines and cosines to represent other functions. However, in wavelet analysis, the scale that we use to look at data plays a special role. Wavelet algorithms process data at different scales or resolutions.

FT with its fast algorithms (FFT) is an important tool for analysis and processing of many natural signals. FT has certain limitations to characterize many natural signals, which are non-stationary (e.g. speech). Though a time varying, overlapping window based FT namely STFT is well known for speech processing applications, a time-scale based Wavelet Transform is a powerful mathematical tool for non-stationary signals.

Wavelet Transform uses a set of damped oscillating functions known as wavelet basis. WT in its continuous (analog) form is represented as CWT. CWT with various deterministic or non-deterministic basis is a more effective representation of signals for analysis as well as characterization. Continuous wavelet transform is powerful in singularity detection. A discrete and fast implementation of CWT is known as the standard DWT.With standard DWT, signal has a same data size in transform domain and therefore it is a non-redundant transform. A very important property was Multi-resolution Analysis allows DWT to view and process.

II. DWT

The discrete wavelet transform became a very versatile signal processing tool after Mallat proposed the multiresolution representation of signals based on wavelet decomposition. The method of multi-resolution is to represent a function (signal) with a collection of coefficients, each of which provides information about the position as well as the frequency of the signal (function). The advantage of the DWT over Fourier transformation is that it performs multi-resolution analysis of signals with localization both in time and frequency, popularly known as time-frequency localization. As a result, the DWT decomposes a digital signal into different sub bands so that the lower frequency sub bands have finer frequency resolution and coarser time resolution compared to the higher frequency sub bands. The DWT is being increasingly used for image compression due to the fact that the DWT supports features like progressive image transmission, ease of compressed image manipulation region of interest coding, etc. Because of these characteristics, the DWT is the basis of the new JPEG2000 image compression standard.

1-D DWT: Any signal is first applied to a pair of low-pass and high-pass filters. Then down is applied to these filtered coefficients. The filter pair (h, g) which is used for decomposition is called analysis filter-bank and the filter pair which is used for reconstruction of the signal is called synthesis filter bank.(g`, h`).The output of the low pass filter after down sampling contains low frequency components of the signal which is approximate part of the original signal and

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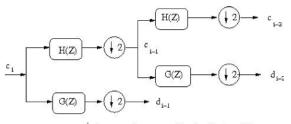
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the output of the high pass filter after down sampling contains the high frequency components which are called details of the original signal.

This approximate part can still be further decomposed into low frequency and high frequency components. This process can be continued successively to the required number of levels. This process is called multi level decomposition, shown in Figure



2 means downsampling by factor of two

Figure 2.1: One Dimensional Two Level Wavelet Decomposition

In reconstruction process, these approximate and detail coefficients are first up-sampled and then applied to low-pass and high-pass reconstruction filters. These filtered coefficients are then added to get the reconstructed version of the original image. This process can be extended to multi level reconstruction i.e., the approximate coefficients to this block may have been formed from pairs of approximate and detail coefficients. Shown in Figure 2.2

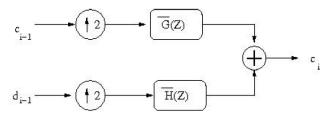




Figure 2.2: One Dimensional Inverse Wavelet Transforms

2-D DWT: One dimensional DWT can be easily extended to two dimensions which can be used for the transformation of two dimensional images. A two dimensional digital image which can be represented by a 2-D array X [m,n] with m rows and n columns, where m, n are positive integers. First, a one dimensional DWT is performed on rows to get low frequency L and high frequency H components of the image. Then, once again a one dimensional DWT is performed column wise on this intermediate result to form the final DWT coefficients LL, HL, LH, HH. These are called sub-bands.

The LL sub-band can be further decomposed into four subbands by following the above procedure. This process can continue to the required number of levels. This process is called multi level decomposition. A three level decomposition of the given digital image is as shown. High pass and low pass filters are used to decompose the image first row-wise and then column wise. Similarly, the inverse DWT is applied which is just opposite to the forward DWT to get back the reconstructed image, shown in Figure 2.3

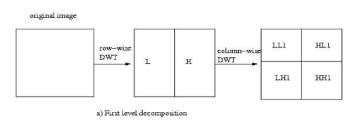




Figure 2.3: Row-Column Computation of 2-D DWT

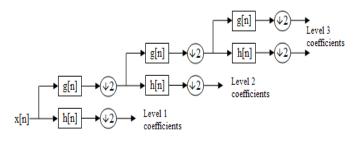


Figure 2.4: Two channel Filter Bank at Level 3

Various architectures have been proposed for computation of the DWT. These can be mainly classified as either Convolutional Architectures or Lifting Based Architectures. The number of computations required to find the DWT coefficients by the filter method is large for higher level of decomposition. This leads to the implementation of new technique called lifting scheme for computing DWT coefficients. This scheme reduces the number of computations and also provides in-place computation of DWT coefficients.

III. DESIGN

The generalized implementation flow diagram of the project is represented as follows.

Initially the market research should be carried out which covers the previous version of the design and the current requirements on the design. Based on this survey, the specification and the architecture must be identified. Then the RTL modeling should be carried out in VERILOG HDL with respect to the identified architecture. Once the RTL modeling is done, it should be simulated and verified for all the cases. The functional verification should meet the intended architecture and should pass all the test cases.

Once the functional verification is clear, the RTL model will be taken to the synthesis process. Three operations will be carried out in the synthesis process such as

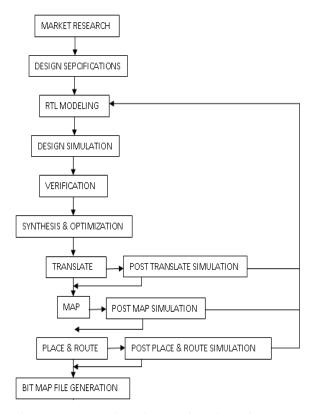


Figure 3.1: General Implementation Flow Diagram

• Translate, Map & Place and Route

The developed RTL model will be translated to the mathematical equation format which will be in the understandable format of the tool. These translated equations will be then mapped to the library that is, mapped to the hardware. Once the mapping is done, the gates were placed and routed. Before these processes, the constraints can be given in order to optimize the design. Finally the BIT MAP file will be generated that has the design information in the binary format which will be dumped in the FPGA board.

IV. IMPLEMENTATION

The 2D (5, 3) wavelet transform block and for the recovery stage 2D (5, 3) Inverse wavelet transform were designed.

A. Integer Wavelet Transform

In conventional DWT realizations, partial transform results need to be represented with a high precision. This raises storage and complexity problems. On the other hand, the Integer Wavelet Transform (IWT) produces integer intermediate results. Thus, it is possible to use integer arithmetic without encountering rounding error problems. There are different types of integer transforms like S(sequential) transform which is popularly known as Haar wavelet transform, S(sequential)+P(prediction) transform, CDF(4,4), CDF(2,2) also known as (5,3) transform etc. The two filter banks supported by JPEG2000 standard are Debauchies (9, 7) and Debauchies (5, 3) filter banks. Since the integer to integer wavelet transform coefficients are integers, it can be used in lossless compression. Since the aim of the thesis is to suggest a reversible (lossless) watermarking method so we will consider only (5, 3) Integer Wavelet Transform.

The analysis and the synthesis filter coefficients for Le Gall 5/3 Integer Wavelet Transform are as shown in the table 3.1.

Table 3.1 Le Gall 5/3 Analysis and Synthesis Filter
coefficients [17]

Analysis	Filter Coefficients	
n	Low Pass filter h(n)	High pass filter g(n)
0	6/8	1
<u>+</u>	2/8	-1/2
<u>+</u>	-1/8	

Equation 3.1 and Equation 3.2 shows the lifting steps for the 5/3 le Gall Integer Wavelet Transform. The rational coefficients allow the transform to be invertible with finite precision analysis, hence giving a chance for performing lossless compression. The equations show the lifting steps for (5, 3) le gall Integer Wavelet Transform. The even and odd coefficient equations for (5, 3) Inverse Integer Wavelet Transform are

$$y(2n+1) = x(2n+1) - \left[\frac{x(2n) + (2n+2)}{2}\right] \quad (3.1)$$
$$y(2n) = x(2n) + \left[y(2n-1) + y(2n+1)\right] \quad (3.2)$$

B. The 2-D (5, 3) DWT

Initially the Pixel values of any image will be taken with the help of MATLAB, which will be used as the primary inputs to the DWT Block.

Basically 1-D (5, 3) DWT block diagram is developed based on the equations (2) and (3). The registers in the top half will operate in even clock where as the ones in bottom half work in odd clock. The input pixels arrive serially row-wise at one pixel per clock cycle and it will get split into even and odd. So after the manipulation with the lifting coefficients 'a' and 'b' is done, the low pass and high pass coefficients will be given out. Hence for every pair of pixel values, one high pass and one low pass coefficients will be given as output respectively.

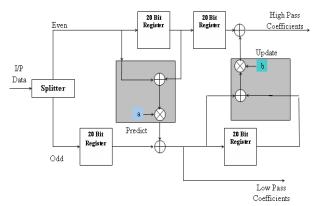


Figure 3.2: Computation of Basic (5, 3) DWT Block in which 'a' and 'b' are lifting coefficients (a = -1/2 and b = 1)

The internal operation of the DWT block has been explained above and hence the high pass and low pass coefficients of the taken image were identified and separated. The generated low pass and high pass coefficients are stored in buffers for further calculations.

V. RESULTS

The test bench is developed in order to test the modeled design. This developed test bench will automatically force the inputs and will make the operations of algorithm to perform.

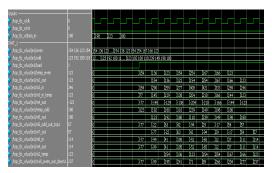


Figure 4.1: Simulation Result of DWT-1 Block with Both High and Low Pass Coefficients

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	-22 42 29 54	-22 x			2 29 x		2 29 54						
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Figure 4.2: Simulation Result of DWT-2 Block with Both High and Low Pass Coefficients

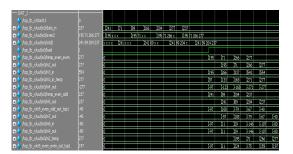


Figure 4.3: Simulation Result of DWT-3 Block with Both High and Low Pass Coefficients

The device utilization summery is shown above in which its gives the details of number of devices used from the available devices and also represented in %. Hence as the result of the synthesis process, the device utilization in the used device and package is shown above.

VI. SYNTHESIS RESULT

tst1 Project Status (04/21/2010 - 17:41:36)							
Project File:	tst1.ise	Current State:	Placed and Routed				
Module Name:	top_dwt	• Errors:	No Errors				
Target Device:	xc3x500e-4fg320	• Warnings:	<u>5 Warnings</u>				
Product Version:	ISE 10.1 - Foundation Simulator	 Routing Results: 	All Signals Completely Routed				
Design Goal:	Balanced	 Timing Constraints: 	All Constraints Met				
Design Strategy:	Xilinx Default (unlocked)	 Final Timing Score: 	0 (Timing Report)				

tst1 Partition Summ

No partition information was found.

Device Utilization Summary						
Logic Utilization	Used	Available	Utilization	Note(s)		
Number of Slice Flip Flops	386	9,312	4%			
Number of 4 input LUTs	532	9,312	5%			
Logic Distribution						
Number of occupied Slices	446	4,656	9%			
Number of Slices containing only related logic	446	446	100%			
Number of Slices containing unrelated logic	0	446	0%			
Total Number of 4 input LUTs	532	9,312	5%			
Number used as logic	292					
Number used for Dual Port RAMs	240					
Number of bonded IOBs	104	232	44%			
Number of BUFGMUXs	1	24	4%			

C. Timing Summary

Speed Grade: -4

Minimum period: 10.081ns (Maximum Frequency: 99.197MHz)

Minimum input arrival time before clock: 4.252ns Maximum output required time after clock: 14.421ns Maximum combinational path delay: No path found

In timing summery, details regarding time period and frequency is shown are approximate while synthesize. After place and routing is over, we get the exact timing summery. Hence the maximum operating frequency of this synthesized design is given as 99.197 MHz and the minimum period as 10.081ns. Here, OFFSET IN is the minimum input arrival time before clock and OFFSET OUT is maximum output required time after clock.

D. RTL Schematic

The RTL (Register Transfer Logic) can be viewed as black box after synthesize of design is made. It shows the inputs and outputs of the system. By double-clicking on the diagram we can see gates, flip-flops and MUX.

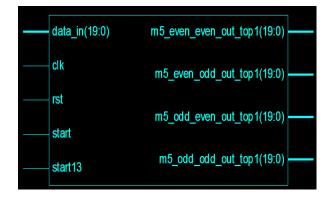


Figure 4.9: DWT Schematic with Basic Inputs and Output

Here in the above schematic, that is, in the top level schematic shows all the inputs and final output of DWT design.

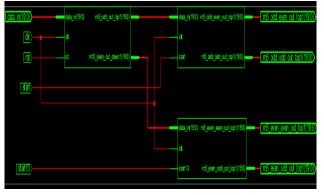


Figure 4.10: Blocks inside the Developed Top Level DWT Design

The internal blocks available inside the design includes DWT-1, DWT-2 and DWT-3 which were clearly shown in the above schematic level diagram. Inside each block the gate level circuit will be generated with respect to the modelled HDL code.

VII. CONCLUSIONS

Basically the medical images need more accuracy without loosing of information. The Discrete Wavelet Transform (DWT) was based on time-scale representation, which provides efficient multi-resolution. The lifting based scheme (5, 3) filters give lossless mode of information. A more efficient approach to lossless whose coefficients are exactly represented by finite precision numbers allows for truly lossless encoding. In this work ensures that the image pixel values given to the DWT process which gives the high pass and low pass coefficients of the input image. The simulation results of DWT were verified with the appropriate test cases. Once the functional verification is done, discrete wavelet transform is synthesized by using Xilinx tool in Spartan 3E FPGA family. Hence it has been analyzed that the discrete wavelet transform (DWT) operates at a maximum clock frequency of 99.197 MHz respectively.

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