Three-Dimensional and 2.5 Dimensional Interconnection Technology: State of the Art

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Three-dimensional (3D) packaging with through-silicon-vias (TSVs) is an emerging technology featuring smaller package size, higher interconnection density, and better performance; 2.5D packaging using silicon interposers with TSVs is an incremental step toward 3D packaging. Formation of TSVs and interconnection between chips and/or wafers are two key enabling technologies for 3D and 2.5D packaging, and different interconnection methods in chip-to-chip, chip-to-wafer, and wafer-to-wafer schemes have been developed. This article reviews state-of-the-art interconnection technologies reported in recent technical papers. Issues such as bump formation, assembly/bonding process, as well as underfill dispensing in each interconnection type are discussed.
[DOI: 10.1115/1.4026615]

1 Introduction

In recent years, driven by the demand for new electronic products with smaller size, lower power consumption, and better performance, 3D packaging is attracting more and more attention from academia and industry. Traditional electronics are integrated in the 2D scheme, and in the early days, usually only one chip was encapsulated in a package. Later, the system in package (SiP) technology brought several chips into a single package, which increases the speed while reducing the size of the package.

Some of the earliest 3D packages were stacked die SiP packages with wire bond connection. In these packages, different dies might be connected either directly with each other or indirectly by way of the substrate. In some types of packages, wire bonding and flip-chip technologies can be used together. The bottom-most chip is connected to the substrate with flip-chip solders, while other chips are connected using wire bonding (Fig. 1). However, the density of the wire bonds is restricted by the dimension of the peripheral of the dies, and a relatively long wiring path also prohibits further improvement in performance. Therefore, 3D interconnection technology using TSVs is the most promising solution for next-generation packages. Compared with the wire bonding method, TSV-based approaches provide shorter wiring distances and higher density, and therefore have a smaller form factor and better electrical performance.

In recent years, methods for fabricating TSVs have been extensively investigated, and different types of TSVs have been developed. From the geometry point of view, annular or fully filled vias with different taper angles were manufactured [2]. The filling material might be copper (Cu), tungsten (W), polysilicon [3], solder material with Cu particles [4], and conductive adhesive [5], etc. Some TSVs serve as electrical connections while some are designed as thermal TSVs (TTSVs) to dissipate the heat and improve thermal management [6,7]. Various manufacturing processes have been studied to create a void-free TSV as quickly and cheaply as possible. At the current stage, although 3D packages with TSVs have not been widely used in products, electronic packages with silicon interposers containing TSVs (such as Xilinx Virtex-7 FPGA [8], etc.) are already on the way to market. Because the coefficient of thermal expansion of the silicon interposer is closer to the die, the silicon interposer can prevent the brittle ultra-low-κ dielectric material of the die from cracking. Packages with TSV interposers are regarded as 2.5D packages. Figure 2 shows a cross section image of the Xilinx Virtex-7 FPGA product, and the Si interposer with TSVs can be clearly seen.

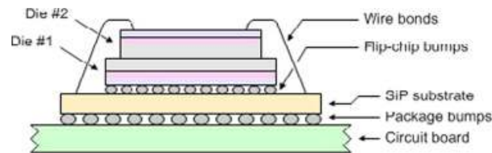

Fig. 1 3D SiP with wire bonds and flip-chip bumps [1]

For the electronics manufacturing industry, 3D packaging is a brand-new area that is much more than creating TSVs through wafers or dies. It involves challenges in various aspects such as materials [9], process control, supply chain, thermal management [6], reliability [10], as well as design guidelines. Among 3D integration processes, creating interconnections between the stacked dies or wafers has crucial importance. A reliable, low-cost, high-performance 3D package must be assembled with a reliable interconnection technology. Generally, technologies for 3D interconnection are categorized into three stacking schemes: chip-to-chip (C2C), chip-to-wafer (C2W), and wafer-to-wafer (W2W). In each scheme, the interconnection technologies differ from each other in terms of the interconnection structures, interconnection and underfill materials, process flows, etc. In journals and at conferences that focus on 3D packaging, many novel types of interconnections have been reported. In this paper, recent advances in 3D and 2.5D interconnection technologies are summarized, and the similarities, differences, advantages, and potential drawbacks of these approaches are discussed briefly.

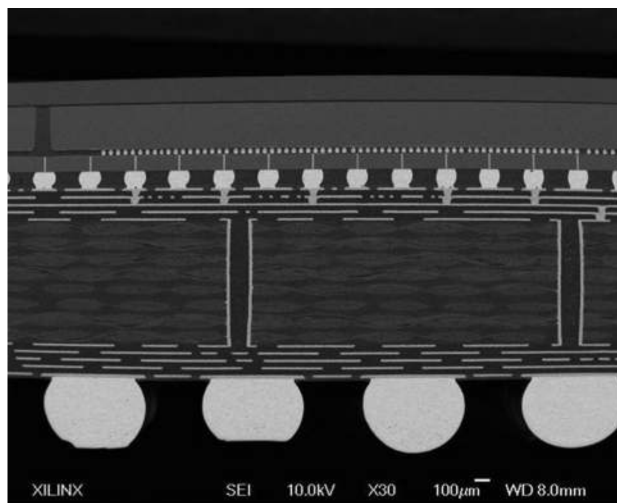

Fig. 2 Cross section of a package with an interposer containing TSVs developed by Xilinx [8]

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Contributed by the Electronic and Photonic Packaging Division of ASME for publication in the Journal of Electronic Packaging. Manuscript received May 7, 2013; final manuscript received January 27, 2014; published online February 18, 2014. Assoc. Editor: Shidong Li.

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2 Chip-to-Chip and Chip-to-Wafer Interconnection

Currently, chip-to-chip (also known as die-to-die or D2D in some literature) stacking is being widely researched in 3D interconnection. In this stacking scheme, although the TSVs are usually fabricated at the wafer level, the wafer is diced into chips before the stacking process. This technology not only minimizes the change in bonding tools but also ensures that only "known good dies" (KGDs) are used in the assembly, which leads to a high yield. Chip-to-chip stacking is a very flexible technology, and chips with different sizes can be integrated in one package. Chip-to-wafer (also known as die-to-wafer, D2W) approaches may also share these advantages. The difference is, in the chip-to-wafer approach, the chips are connected to the wafer, and the singulation of each stack is performed after the assembly, or even after the underfill dispensing and molding process [11]. Multiple chips can be bonded to a temporary carrier and then assembled to the wafer simultaneously. Therefore, chip-to-wafer stacking can achieve higher throughput than chip-to-chip stacking. In addition, a specially designed template can be used as the carrier to improve the precision of the alignment [12]. In recent years, there have been numerous advances in chip-to-chip and chip-to-wafer approaches, many of which use fine-pitch microbumps or Cu pillars for interconnection and adopt improved underfill dispensing technologies.

2.1 Bump Structure. Various interconnection types with different materials, sizes, and even structures have been reported in recent years. Common interconnection structures such as microbumps and Cu pillars have been used in 3D chip-stacking structures [13–22]. Generally, the trend of the interconnection is becoming smaller in dimension, finer in pitch, and higher in interconnection density. Bumps with 10 μm pitch have already been studied [14]. Some innovative bump structures invented in recent years, such as the Ni micro-insert [23–25] and the Cu/Sn interlocking bump [26,27], have also been applied to 3D interconnections. Figure 3 shows a cross section view of interlocking bumps fabricated by Jang et al. [28]. Sn bumps (25 μm in diameter and 15 μm high) were fabricated on one chip, and the Cu interlocking bumps on the other chip were inserted into the larger Sn bumps using the flip-chip bonding process. Planar bumps (70 μm in diameter and 10 μm high) directly fabricated on Cu TSV were also used in the same paper (Fig. 3). Souriau et al. used micro-insert interconnection technology in their chip-to-wafer stacking study [29]. In that process, a matrix of micro-inserts made of Ni was inserted in the soft NiSn material, which was formed on the corresponding location on the wafer (or on other dies). An image of the micro-inserts matrix is shown in Fig. 4. These novel structures have several benefits. First, they meet the trend of miniature in the packaging industry and enable high-density interconnection, one of the driving forces of TSV-based 3D integration. Small bump size not only reduces the distance between dies but also leaves more space on the die so that more TSVs can be fabricated. Second, these structures are compatible with mature flip-chip bonding techniques for chip-to-chip or chip-to-wafer connections. In addition, the mechanical robustness and electrical performance have

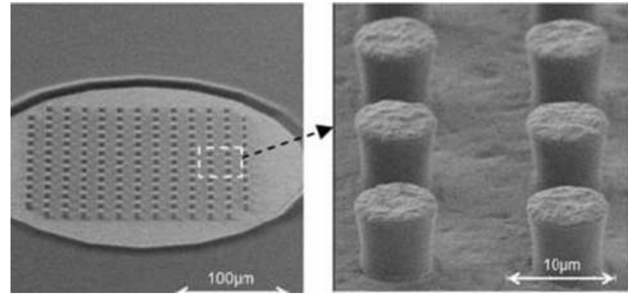

Fig. 4 Image of fabricated micro-inserts [29]

been tested by the inventors [28,30]. Some disadvantages of these novel structures have also been pointed out in publications. For instance, the micro-insert approach is sensitive to planarity, and nonflatness may increase electrical resistivity [23].

The Cu pillar bump technology has emerged in recent years. This technology enables small pitch size and high interconnection density. Compared with the solder-bump-based interconnection, a Cu pillar with a solder cap has many advantages such as higher standoff, less solder spread out [31,32], etc. Though this technology was invented not long ago, it has already been used in 3D/2.5D packaging [19,33], and the effect of solder capping material has been studied [34]. Direct Cu to Cu bonding using the thermo-compression method, which can connect two Cu pillars (or studs) without using any solder material, has also been researched [35,36].

2.2 Bumping and Assembly Process. Formation of the bumps or pads is an important step in the packaging process. Various bumping methods have been investigated to make the process more efficient and reliable.

The controlled collapse chip connection (C4) technology, which was invented by IBM in the 1960s, is a well-established interconnection technology. Different methods of making C4 bumps, such as masked evaporation [37], paste screening [38], and photolithographic electroplating [39], have been developed since its invention. A current C4 bumping technology developed by IBM, the C4-New Process (C4NP), has already been used in 3D chip-stacking [21,22,40]. The C4NP process utilizes a glass mold with cavities to transfer solder to the wafer. Molten solder is injected in the cavities of the mold, and then the mold is aligned below the wafer. Then, the wafer and the mold are heated above the solder's melting temperature in a sealed-off manufacturing environment so that the solder will wet the underbump metallization (UBM) and attach to the wafer. The C4NP process flow is schematically depicted in Fig. 5. Compared with other bumping methods, this approach combines several advantages, such as the capability of fabricating fine-pitch bumps in volume production, easy change of solder materials, environmentally friendly manufacturing (no plating chemical), low cost, etc. [40].

Due to the capability to fabricate tiny bumps, plating is another popular method for bumping and forming UBM. Electrolytic and

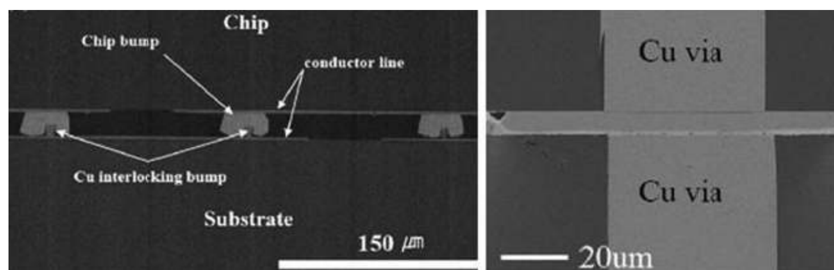

Fig. 3 Cross section image showing interlocking Sn/Cu bumps (left) and a Cu planar bump with TSVs (right) [28]

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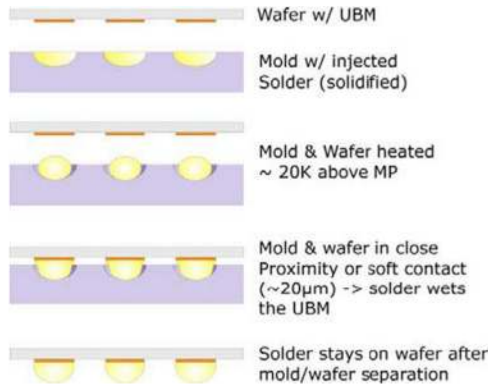

Fig. 5 Solder transfer process in C4NP technology [21]

electroless plating processes are widely used; for example, Cu pillars with different solder caps can be formed by electroplating [41]. Reflow and plasma cleaning that removes contamination and the oxidation layer might be conducted after plating [42]. Various deposition methods are also commonly used. For example, in Souriau et al.'s micro-inserts approach, the Ni and NiSn layers were formed by the electroplated chemical deposition method on a Ti/Cu seed layer, while the seed layer was deposited by physical vapor deposition [29].

The conventional approach for making TSVs includes a process (usually chemical–mechanical planarization, CMP) for removing the overburden Cu. However, a recent study has shown that by improving the TSV filling process, the Cu microbumps on the active side of the TSV can be directly formed by the electroplating method in the TSV-filling process, so there is no need to remove Cu and perform extra bumping on that side [43]. The TSVs and Cu microbumps fabricated by this novel process are shown in Fig. 6.

A solder bump maker (SBM) technology that does not require solder mask has also been reported [44–46]. The SBM is made up of resin, additives, and Sn58Bi solder powder. A guide is used to control the thickness of the SBM layer, and excessively printed SBM materials are removed with a blade. Then, the guide is removed, the chip is reflowed, and the bumps are formed. A coining process is applied to guarantee the uniformity of the height by compressing the bumps at elevated temperature. The SBM bumps have low volume and can be formed directly on top of the TSVs. The schematic diagram of the bumping process is shown in Fig. 7, and a cross section image of the bumps after the coining process is shown in Fig. 8.

New interconnection materials and bonding techniques are emerging, and various new processes have been developed. Traditional flip-chip bonding approaches and many novel technologies have been introduced in the 3D chip-to-chip or chip-to-wafer packaging area.

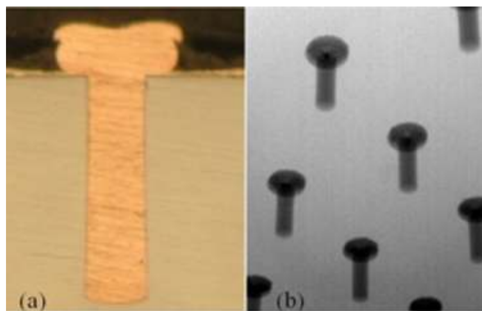

Fig. 6 Cross section image of Cu-filled TSV with Cu microbump (*a*) and X-ray photo of TSVs after Sn plating (*b*) [43]

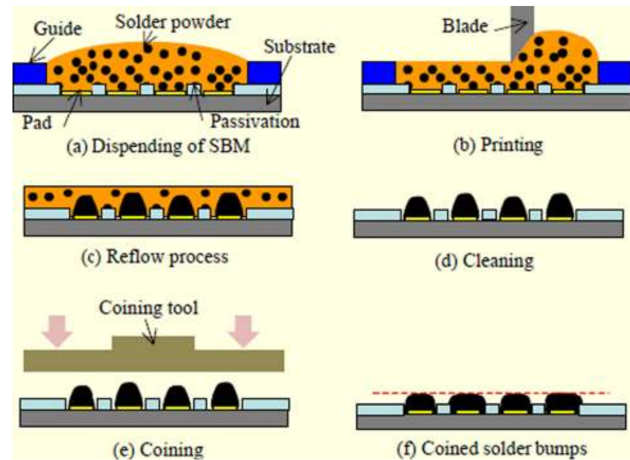

Fig. 7 Schematic diagram of the SBM bumping process [45]

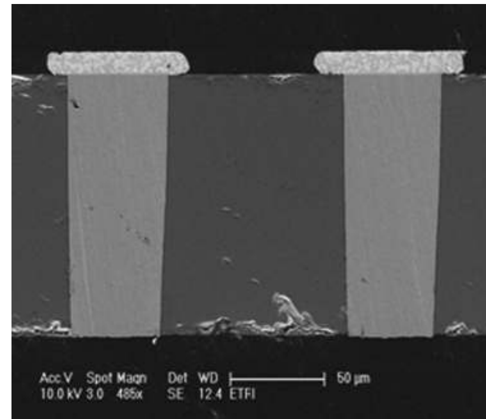

Fig. 8 Cross section image showing TSVs and coined bumps [44]

2.2.1 Bonding With C4 Reflow Process. Due to numerous advantages such as low cost and the ability to rework, C4 is a very successful technology widely used in flip-chip packaging. Since flip-chip bonding techniques were used in 3D chip stacking, C4 interconnections in 3D chip-stacks have also been studied [15–18,21,22]. In the C4 assembly approach, solders are fabricated on the chip, and then the chip is positioned and placed on the substrate. Finally, the interconnection is created by a reflow process.

Reflow is one of the most important steps in the C4 process. For 3D assembly, multiple chips must be stacked one over another, and two different joining strategies may be used. One way is to use sequential reflow. In sequential reflow, the bottom chips are mounted first, followed by a reflow process. Then, other chips are assembled sequentially from the bottom to the top, and the reflow process is repeated after each chip is mounted. In parallel reflow, an alternative approach, several chips are mounted together, and then all the chips are joined in a single reflow process. Parallel reflow leads to higher manufacturing throughput; however, this approach requires better control of the placement process, because the solder bumps are not connected until reflow. In contrast, for sequential reflow, the relative displacement between each layer can be controlled in each joining process, at the cost of time and the risk of dissolving more UBM material in the solder [21]. Both approaches have been successfully implemented in experiments, and a three-layer stack by IBM using sequential reflow is demonstrated in Fig. 9.

As the size of the microbumps decreases, flux cleaning becomes more and more difficult, especially for large dies. Two

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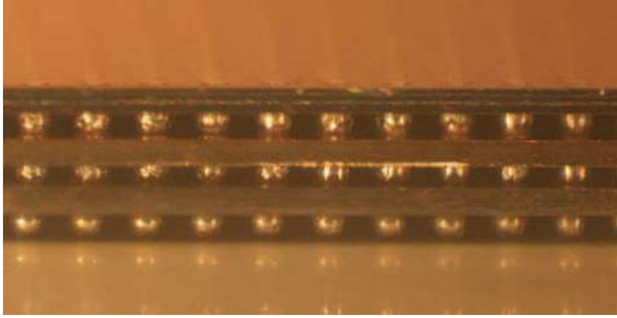

Fig. 9 A three-layer chip-stack fabricated with sequential reflow process by IBM [17]

approaches have been studied to resolve this issue. One improves the flux-cleaning tools or processes, and the other approach adopts a fluxless bumping method. Au et al. applied an additional force-flow system to the inline pressurized spray system in their research, and a test on a four-layer stacked-chip module with a 30 μm gap showed that the force-flow system is four times more efficient than inline pressurized spray only [15]. Maria et al. tried two approaches: a fluxless bonding approach with formic acid ambient and flux bonding with a water-soluble flux. Both led to successful results [18].

2.2.2 Bonding With Thermocompression. In the thermocompression method, interconnection materials are pressed together at elevated temperature to form the joints. The process temperature and pressure depend on the material and geometry of the joints. Various studies have been conducted on creating interconnections between stacked strata using thermocompression. For instance, micro-inserts and interlocking bump structures (Sec. 2.1) have been assembled in this way [28,29]. The thermocompression method does not require the reflow process and has been used to create tiny, fine-pitch interconnections [13]. Zhan et al. compared two thermocompression bonding methods: conventional thermocompression in which the top chip was compressed continuously and gap-control thermocompression containing two separate compressions, while each compression had its own pressure and duration value. The experiment showed that novel gap-control bonding might prohibit the solder squeezing issue and lead to better bonding results [42].

Direct Cu–Cu bonding with thermocompression offers several benefits such as low electrical resistivity, high thermal conductivity, and low susceptibility to electromigration. Key parameters of this process include temperature, pressure, duration, and surface cleanness of Cu [47]. The variation of Cu pillar/pad height is a concern, and a method for compensating the bump height variation was proposed by Lee et al. using electroless Ni plating [35]. In Lee et al.'s approach, the Cu pillars and Cu studs were formed on two chips. After bonding with thermocompression, the bonded parts were put through cleaning, surface roughening, catalyst and conditioning process, and then immersed in the Ni-P solution for plating. As a result, the electroless plating process led to improved interconnection quality by filling the gap between the Cu pillars and the studs, thus reducing the resistance by 15%.

2.2.3 Low-Temperature Interconnection Methods. In addition to traditional thermocompression and reflow soldering processes, novel low-temperature interconnecting processes have also been developed [48]. In C2C and C2W approaches, low-temperature soldering processes such as the transient liquid phase (TLP) and solid state diffusion bonding usually feature a low melting point at bonding but a high remelting temperature due to the formation of an intermetallic layer. These methods may greatly reduce the temperature required at assembly, and therefore reduce the stress induced by thermal mismatch. Bonding materials reported in the literature include InSn by Morinaga et al. [49], AuInSn by Xie et al. [50], CuSn by Zhang, Agarwal et al. [51,52] and Sakuma et al. [53], CuInNi by Sakuma et al. [53], etc. Agarwal et al. used two relatively low-temperature processes for the CuSn material, TLP and solid metal bonding (SMB). The SMB bonding has a lower processing temperature than TLP, which is below the melting point of Sn [51]. Sakuma et al. compared the reliability of CuInNi and CuSn bonding with finite element analysis (FEA) and experiments, and results indicated that the NiCuIn solder showed better thermomechanical reliability than the CuSn solder. Different failure modes were associated with two material combinations. For CuInNi, the failure was found on In; while for CuSn, failures such as die-cracking were found [53].

One point worth mentioning is that the advantage of these low-temperature bonding methods is not just low-temperature processing. The trends in the packaging industry are higher density, more controllable processes, higher thermomechanical reliability, and these goals have been achieved by these novel approaches. For example, in Ref. [53], low-volume CuNiIn solder only 6 μm high was successfully made on an annular, tungsten-filled TSV, and the samples exhibit good reliability in the thermal cycling tests.

2.3 Issues on Underfill. Underfill is a key technology for improving the thermal–mechanical reliability of flip-chip packages. Many variations of underfill have been developed to increase reliability, simplify the process, achieve higher yield, and reduce the voids [54]. As the industry began to use flip-chip technologies to create the chip-stacking structure, this reliability-enhancing technology was applied to 3D packaging as well. However, as the distances between chips decrease, dispensing underfill is becoming more challenging. Yet many researchers have successfully dispensed the underfill into the small gaps [15,16,18,53]. Au et al. filled all the gaps in a four-die stack package through a multiple line/multiple needle height dispensing process, so that the encapsulation of all gaps between the joints can be done simultaneously [15]. Au et al. also found that the corner fillet value of conventional filling would expose the top-most solder joint gap interface (Fig. 10). In contrast to the traditional capillary underfill process in which the flow of underfill is driven by the surface tension, a vacuum filling approach was developed by researchers at IBM [18,55]. In the vacuum filling approach, the flow of underfill is driven by the pressure difference, and this change in the dispensing mechanism led to better filling quality. A scanning acoustic microscope (SAM) image shows that the vacuum filling technology can fill a 14 μm gap without leaving a visible void in the underfill, while in its counterpart, the small voids appear clearly in the SAM image (Fig. 11).

Instead of dispensing underfill after stacking, another approach uses no-flow underfill or adhesive to fill the gaps between the chips. No-flow underfill is dispensed before the chip-attachment process and cured after the assembly. The solder reflow and cure process can be integrated, leading to a more efficient manufacturing process. Adhesive materials that are pre-applied before the assembly process may serve a similar function as underfill; therefore, in this paper, the term "simultaneous underfill" is used to describe the materials that fill the space between Si chips or wafers simultaneously with the assembly process.

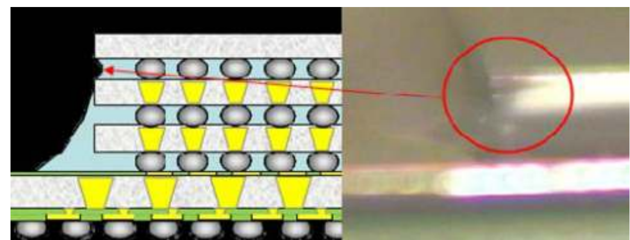

Fig. 10 A gap exposed by using a typical 50% corner fillet value in underfill dispensing [15]

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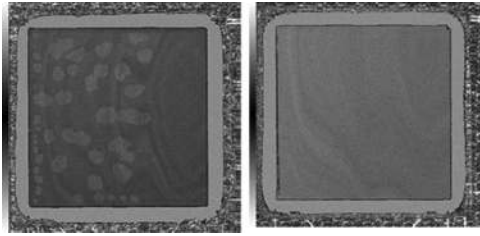

Fig. 11 SAM image of flip-chip samples after capillary (left) and vacuum (right) underfill dispensing [55]

Myo et al. combined In-based low temperature with no-flow underfill [56]. In that study, the chip-stacking structure was fabricated by attaching the chips sequentially. In each step, the underfill was dispensed onto the substrate (or lower chips), and then the chip was placed and bonded. A similar underfill approach was performed by Agarwal et al. in low-temperature chip-to-wafer bonding with CuSn microbumps [51].

Hybrid bonding using metallic materials for interconnection and adhesive materials as simultaneous underfill has also been investigated. For example, the Cu/Sn interlocking bump technology in Sec. 2.1 uses adhesive to fill the gap and secure the structure [28]. Some scholars use the term "wafer-level underfill" (WLUF) for the pre-applied material on the wafer that glues the chips or wafers together in the assembly process and serves the same function as regular underfill afterward [54]. In the manufacturing process with wafer-level underfill, the bumping is performed at the wafer level, and then the wafer-level underfill is applied on the wafer, usually by spin coating (or vacuum lamination, screen printing, stencil printing). A B-stage cure process follows if the underfill is initially in a liquid state. Then, the wafer is diced for assembly if chip-to-chips or chip-to-wafer stacking is used [57].

The resin or filler on the bump surface is a problem that potentially affects the connection. To get rid of these materials, hybrid bonding technology with a planarization process was developed. The planarization process is usually CMP or diamond bit cutting. Nimura et al. developed a low-cost thermal pressure planarization process. In their approach, the resin was compressed by a silicon substrate coated with a release agent. The solder/adhesive and Au/adhesive bonding were successfully implemented after this novel planarization process [58–60].

Because of the difficulty in underfill dispensing, 3D chip-stacking structures without underfill were also studied [34,61]. Researchers have used FEA and experimental methods to study the reliability of 3D packages with and without underfill materials. Although producing packages without underfill is usually not preferable, in some cases the reliability appears acceptable. For example, Kohara et al. showed that samples with a thin die ($50\,\mu$m or $70\,\mu$m thick, 7.3 mm by 7.3 mm chip area) connected to a silicon interposer by $40\,\mu$m pitch solder joints could survive 1000 thermal cycles even without underfill. However, with a thick die ($725\,\mu$m thick with the same chip area), the parts failed shortly after the test, but the parts with underfill passed. Finite element simulation reached consistent results with the reliability test [61]. Therefore, experiments must be performed to carefully evaluate the reliability, and numerical simulation is also suggested.

3 Wafer-to-Wafer Interconnection

Unlike chip-to-chip or chip-to-wafer stacking, the wafer-to-wafer process is performed completely at the wafer level, and only one singulation process is performed after all wafer-stacking steps have been completed. In this aspect, the wafer-to-wafer process has a high manufacturing throughput. However, the problem with the wafer-to-wafer approach is yield. Because there is no way to cherry-pick the KGDs, the yield for wafer-to-wafer stacking is lower than chip-to-chip or chip-to-wafer stacking, and the yield decreases as the number of stacked layers increases. The cost-effectiveness of wafer-to-wafer stacking has been analyzed and compared with the chip-to-wafer approach [62,63]. On one hand, the analysis in Ref. [63] shows that either chip-to-wafer or wafer-to-wafer stacking might be more cost-effective, depending on the chip area and production volume; on the other hand, for the wafer-to-wafer approach, low yield could greatly increase the cost due to the loss of good dies, especially for large chips [64].

Due to the dimension of the wafer, dispensing underfill into the narrow gaps between wafers is very difficult, if not impossible. And even after wafer-dicing, filling underfill into the narrow gaps inside the chip-stacks is still challenging (Sec. 2.3). Therefore, recent studies of wafer-to-wafer interconnection focus on processes using simultaneous underfill or techniques that do not necessitate underfill at all [65].

3.1 With Simultaneous Underfill.

The simultaneous underfill approach is an emerging technology that has attracted many researchers. Once the bonding process is finished, the gap between wafers is occupied by the filled materials simultaneously, and the filled materials act as a stress-redistribution layer to alleviate the reliability risk at the electrical joints. Depending on the interconnection structure and the TSV formation process, wafer-to-wafer bonding with simultaneous underfill can be divided mainly into two categories: One is the metal bump interconnection with adhesive or polymer as simultaneous underfill, and the other is adhesive bonding followed by the TSV formation process, which is supported by the wafer-on-wafer (WOW) Alliance and also known as the WOW approach.

Hybrid bonding combines the interconnection process of metal bumps with simultaneous adhesive attachment between wafers. Therefore, the adhesive acts as both bonding material and "underfill." A great advantage of hybrid bonding is that the old technologies and experiences for creating metal-to-metal joint can be applied to this new method. Ko et al. and Chang et al. worked on the wafer-to-wafer hybrid bonding with CuSn and benezocyclobutene (BCB) [66,67], and the process flow is shown in Fig. 12. The Cu bumps were formed on the top wafer, and the CuSn bumps were fabricated on the bottom wafer. Then, the BCB adhesive were applied to both wafers by spin-coating and lithography, followed by a postlithographic treatment process for cleaning the bump surface. The bonding process was carried out at 250 °C. The wafer-thinning and backside metallization were conducted after the bonding. Unlike other wafer-handling processes that require temporal bonding to silicon or glass carrier, this approach features a carrier-less wafer-handling process that can simplify the process flow. Cross-sectional scanning electron microscope

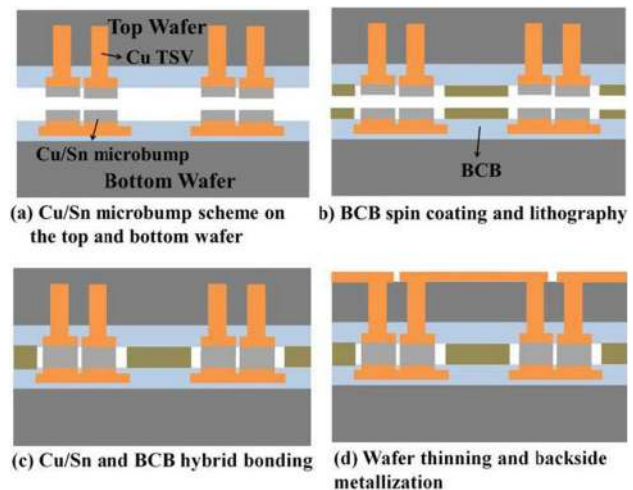

Fig. 12 Schematic diagram of the process flow of wafer-to-wafer hybrid bonding [66]

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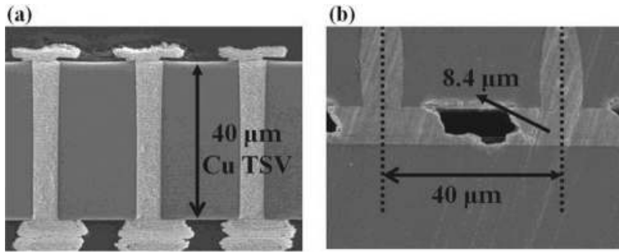

Fig. 13 Cross section images of TSVs and microbumps [67]

(SEM) images showing the TSVs and microbumps are given in Fig. 13.

In addition to forming interconnections with eutectic solder materials, the Cu–Cu [47,68–70] or Au–Au [59,60] connection process with adhesive (also known as transfer-join process or TJ) has also been developed. IBM researchers fabricated joints with a mechanical lock-and-key structure using this process. In the structure shown in Fig. 14, a Cu stud was made on the top wafer, and a recess was made on the bottom wafer. A polyimide (PI) layer was coated on the top wafer. After the PI on the Cu studs was removed, the wafers were aligned and bonded by thermocompression in vacuum.

Hybrid bonding, like many commonly used packaging methods, utilizes metal bumps for interconnection. These metal bumps are not only part of the electrical circuit but also an important mechanical structure that provides support and endures stresses and strains. The bump structure is a potential failure location under mechanical or thermomechanical loadings. The adhesive bonding followed by TSV formation is a low-temperature, bumpless process. This process is also referred to as WOW because of the support of the wafer-on-wafer alliance. The difference between a bump-based joint and a bumpless joint is illustrated in Fig. 15.

Several technical papers have been published on fabrication with WOW technology, and the electrical and mechanical properties have also been studied [71–73]. A detailed schematic diagram of the process is shown in Fig. 16. The wafer is first temporally bonded to the support glass wafer and then undergoes the thinning process. Usually the wafer is thinned down to less than 20 μm, or even 10 μm. Then, the wafer is bonded with BCB/Cyclotene™ adhesive, and the TSV etching and filling processes are then performed. Figure 17 shows stacked wafers with TSV fabricated by this process.

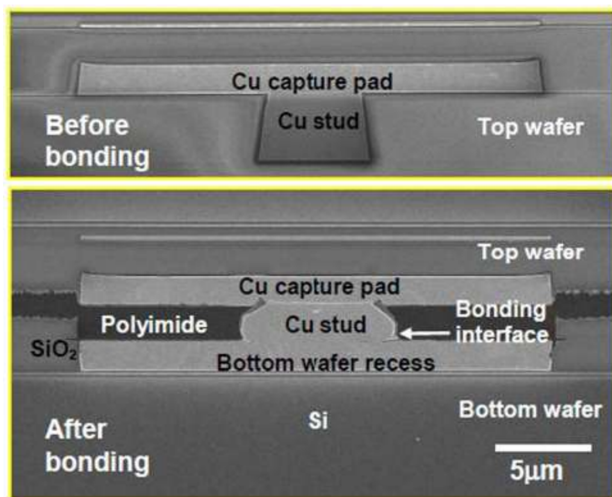

Fig. 14 SEM cross section image of the joint structure before (top) and after bonding (bottom) [69]

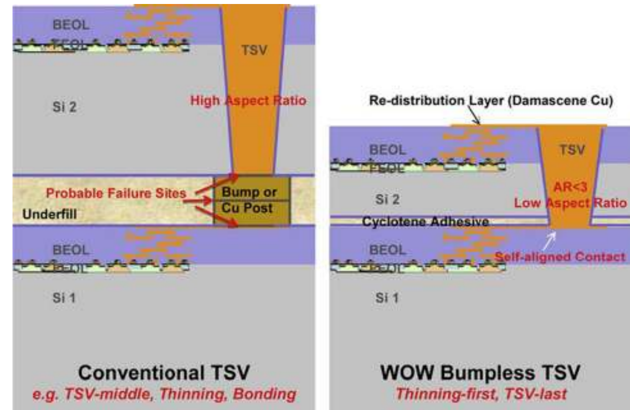

Fig. 15 Comparison of the conventional joint structure and the WOW bumpless structure [71]

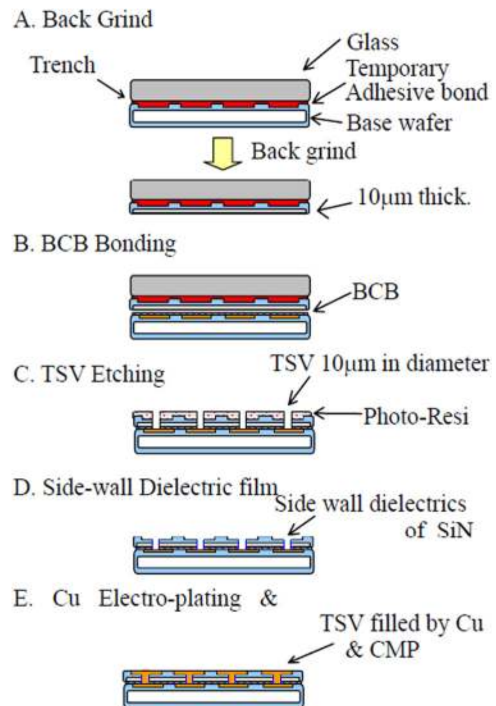

Fig. 16 Process flow of the WOW bumpless interconnection technology [72]

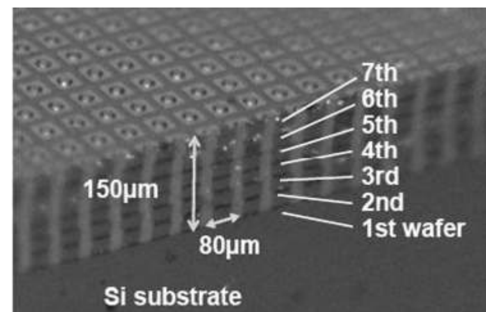

Fig. 17 A seven-layer wafer-stacking structure using the WOW process [73]

3.2 Without Underfill. Underfill is applied to fill the gaps between Si chips or wafers to enhance the reliability of electronic packages. If two wafers with active circuits can be directly bonded together without any gap, there is no need for underfill. For

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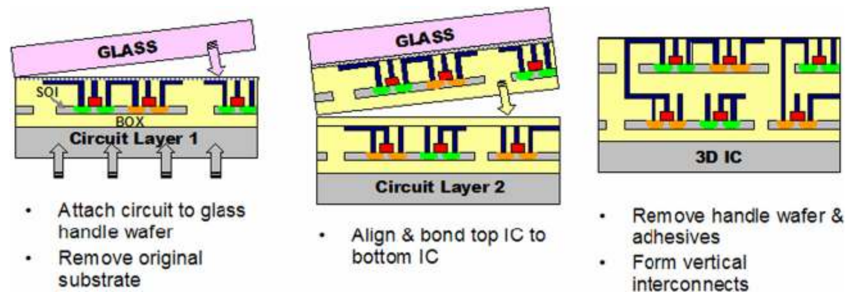

Fig. 18 Schematic diagram of bonding an SOI wafer to the bottom wafer based on the IBM platform [76]

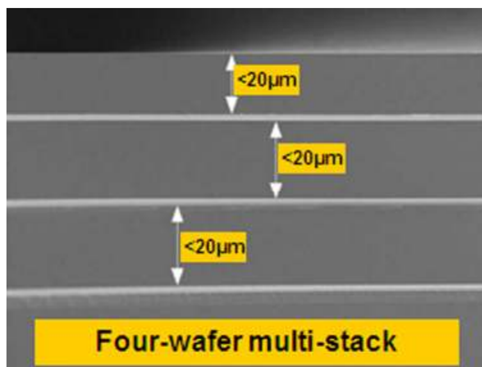

Fig. 19 SEM image of a four-layer stack fabricated with SiO_2 fusion bonding [77]

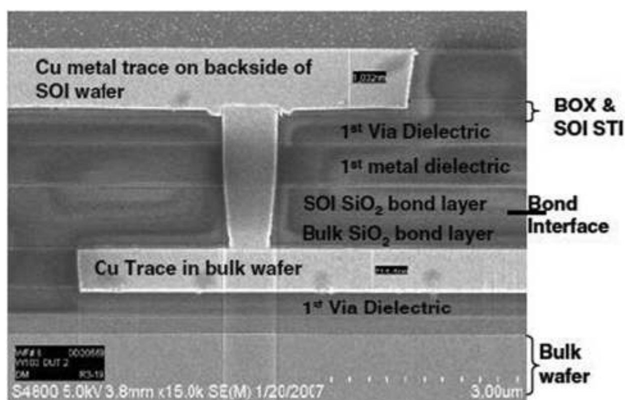

Fig. 20 SEM cross section image showing a TSV connecting two bonded wafers [78]

example, silicon direct bonding is a technology that directly puts two wafers into contact by either Si-Si or Si-SiO_2-Si fusion. The bonding surface of the wafers must be very flat and clean. The bonding process can be processed at room temperature, but high-temperature (above 800 °C) annealing is required to formulate strong covalent bonds at the interface. Low-temperature solutions can be obtained by activating the wafer surface using wet chemical or plasma before bonding [48,74]. Three-dimensional integration using silicon direct bonding has been studied by organizations such as IBM, Freescale, etc. Face-to-face and face-to-back joining are both applicable [75–78]. A face-to-back joining process to stack a silicon-on-insulator (SOI) wafer to another wafer based on the IBM platform is schematically shown in Fig. 18. First, the top wafer is temporally attached to a carrier glass wafer, and then thinned down, aligned, and bonded to the bottom wafer, while the bottom wafer usually remains at full thickness to support the stacking structure. After the bonding process, the TSVs are formed through the thinned wafer to create electrical paths. The SEM image of a four-layer stack fabricated with SiO_2 fusion bonding is shown in Fig. 19, and a cross section SEM image showing the TSV is shown in Fig. 20. In addition to the TSV-last option in Fig. 18, creating metal-to-metal interconnections simultaneously with the wafer bonding process has also been proven feasible experimentally [79–81].

4 Summary

This paper summarizes state-of-the-art technologies in chip-to-chip, chip-to-wafer, and wafer-to-wafer interconnection schemes. Different interconnection structures with different fabrication processes are compared. In chip-to-chip and chip-to-wafer stacking, many flip-chip packaging technologies have been applied to 2.5D and 3D processes, and various innovational approaches have been explored in bump formation, low-temperature assembly process, flux cleaning, underfill dispensing, etc. At the wafer-to-wafer level, technologies such as silicon/oxide fusion, wafer-on-wafer adhesive bonding with the via-last approach, and hybrid bonding using metallic interconnection with adhesive have been developed. Regardless of the TSV fabrication and assembly process, wafer-thinning is commonly performed in wafer-level processes, and thin-wafer handling techniques have been studied extensively. Although each interconnection method listed in this article has its advantages and drawbacks, all of the 3D packaging technologies share a common goal: to create reliable, high-density interconnections for 3D applications productively and cost-effectively.

Acknowledgment

The authors would like to thank all the members of the Opto-Mechanics and Physical Reliability Laboratory in the Department of Mechanical Engineering at SUNY-Binghamton for their helpful support.

References

[1] Maxfield, C., 2012, "2D vs. 2.5D vs. 3D ICs 101," EE Times, http://www.eetimes.com/design/programmable-logic/4370596/2D-vs–2-5D-vs–3D-ICs-101
[2] Lu, K. H., 2010, "Thermo-Mechanical Reliability of 3-D Interconnects Containing Through-Silicon-Vias (TSVs)," Ph.D. thesis, University of Texas at Austin, Austin, TX.
[3] Pares, G., De Crecy, F., Moreau, S., Maurice, C., Borbely, A., Mazuir, J., Chapelon, L. L., and Sillon, N., 2011, "Assessment and Characterization of Stress Induced by Via-First TSV Technology," J. Microelectron. Electron. Packag., **8**(4), pp. 129–139.
[4] He, R., Wang, H., Zhou, J., Guo, X., Yu, D., and Wan, L., 2011, "Nonlinear Thermo-Mechanical Analysis of TSV Interposer Filling With Solder, Cu and Cu-Cored Solder," 12th International Conference on Electronic Packaging Technology and High Density Packaging (ICEPT-HDP), Shanghai, August 8–11.
[5] Lee, S. W. R., Hon, R., Zhang, S. X. D., and Wong, C. K., 2005, "3D Stacked Flip Chip Packaging With Through Silicon Vias and Copper Plating or Conductive Adhesive Filling," 55th Electronic Components and Technology Conference (ECTC), Lake Buena Vista, FL, May 31–June 5, pp. 795–801.
[6] Venkatadri, V., Sammakia, B., Srihari, K., and Santos, D., 2011, "A Review of Recent Advances in Thermal Management in Three Dimensional Chip Stacks in Electronic Systems," ASME J. Electron. Packag., **133**(4), p. 041011.

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[7] Onkaraiah, S., and Chuan Seng, T., 2010, "Mitigating Heat Dissipation and Thermo-Mechanical Stress Challenges in 3-D IC Using Thermal Through Silicon Via (TTSV)," 60th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, June 1–4, pp. 411–416.
[8] Santarini, M., 2011, "Stacked & Loaded: Xilinx SSI, 28-Gbps I/O Yield Amazing FPGAs," Xcell J., **74**(1), pp. 8–13.
[9] Tu, K. N., Hsiao, H.-Y., and Chen, C., 2012, "Transition From Flip Chip Solder Joint to 3D IC Microbump: Its Effect on Microstructure Anisotropy," Microelectron. Reliab., **53**(1), pp. 2–6.
[10] Tu, K. N., 2011, "Reliability Challenges in 3D IC Packaging Technology," Microelectron. Reliab., **51**(3), pp. 517–523.
[11] Dunne, R., Takahashi, Y., Mawatari, K., Matsuura, M., Bonifield, T., Steinmann, P., and Stepniak, D., 2012, "Development of a Stacked WCSP Package Platform Using TSV (Through Silicon Via) Technology," IEEE 62nd Electronic Components and Technology Conference (ECTC), San Diego, CA, May 29–June 1, pp. 1062–1067.
[12] Chen, Q., Zhang, D., Xu, Z., Beece, A., Patti, R., Tan, Z., Wang, Z., Liu, L., and Lu, J.-Q., 2012, "A Novel Chip-to-Wafer (C2W) Three-Dimensional (3D) Integration Approach Using a Template for Precise Alignment," Microelectron. Eng., **92**, pp. 15–18.
[13] Yu, A., Lau, J. H., Ho, S. W., Kumar, A., Hnin, W. Y., Yu, D.-Q., Jong, M. C., Kripesh, V., Pinjala, D., and Kwong, D.-L., 2009, "Study of 15μm Pitch Solder Microbumps for 3D IC Integration," 59th Electronic Components and Technology Conference (ECTC), San Diego, CA, May 26–29, pp. 6–10.
[14] Lee, C.-K., Zhan, C.-J., Lau, J. H., Huang, Y.-J., Fu, H.-C., Huang, J.-H., Hsiao, Z.-C., Chen, S.-W., Huang, S.-Y., Fan, C.-W., Lin, Y.-M., Kao, K.-S., Ko, C.-T., Chen, T.-H., Lo, R., and Kao, M. J., 2012, "Wafer Bumping, Assembly, and Reliability Assessment of μ bumps With 5μm Pads on 10 μm Pitch for 3D IC Integration," 62nd Electronic Components and Technology Conference (ECTC), San Diego, CA, May 29–June 1, pp. 636–640.
[15] Au, K. Y., Beleran, J. D., Yang, Y. B., Zhang, Y. F., Kriangsak, S. L., Wilson, P. L. O., Drake, Y. S. K., Toh, C. H., and Surasit, C., 2011, "Thru Silicon Via Stacking & Numerical Characterization for Multi-Die Interconnections Using Full Array & Very Fine Pitch Micro C4 Bumps," 61st Electronic Components and Technology Conference (ECTC), Lake Buena Vista, FL, May 31–June 3, pp. 296–303.
[16] Au, K. Y., Kriangsak, S. L., Zhang, X. R., Zhu, W. H., and Toh, C. H., 2010, "3D Chip Stacking & Reliability Using TSV-Micro C4 Solder Interconnection," 60th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, June 1–4, pp. 1376–1384.
[17] Dang, B., Wright, S. L., Andry, P. S., Sprogis, E. J., Tsang, C. K., Interrante, M. J., Webb, B. C., Polastre, R. J., Horton, R. R., Patel, C. S., Sharma, A., Zheng, J., Sakuma, K., and Knickerbocker, J. U., 2008, "3D Chip Stacking With C4 Technology," IBM J. Res. Dev., **52**(6), pp. 599–609.
[18] Maria, J., Dang, B., Wright, S. L., Tsang, C. K., Andry, P., Polastre, R., Liu, Y., Wiggins, L., and Knickerbocker, J. U., 2011, "3D Chip Stacking With 50 μm Pitch Lead-Free Micro-C4 Interconnections," 61st Electronic Components and Technology Conference (ECTC), Lake Buena Vista, FL, May 31–June 3, pp. 268–273.
[19] Patterson, D. S., 2012, "2.5D/3D Packaging Enablement Through Copper Pillar Technology," Chip Scale Review, **16**(3), pp. 20–26.
[20] Farooq, M. G., Graves-Abe, T. L., Landers, W. F., Kothandaraman, C., Himmel, B. A., Andry, P. S., Tsang, C. K., Sprogis, E., Volant, R. P., Petrarca, K. S., Winstel, K. R., Safran, J. M., Sullivan, T. D., Chen, F., Shapiro, M. J., Hannon, R., Liptak, R., Berger, D., and Iyer, S. S., 2011, "3D Copper TSV Integration, Testing and Reliability," 2011 IEEE International Electron Devices Meeting (IEDM), Washington, DC, December 5–7, pp. 7.1.1–7.1.4.
[21] Busby, J., Dang, B., Gruber, P., Hawken, D., Shah, J., Weisman, R., Perfecto, E., Ruhmer, K., and Buchwalter, S., 2008, "C4NP Lead Free Solder Bumping and 3D Micro Bumping," IEEE/SEMI Advanced Semiconductor Manufacturing Conference (ASMC 2008), Cambridge, MA, May 5–7, pp. 333–339.
[22] Shih, D. Y., Dang, B., Gruber, P., Lu, M., Kang, S., Buchwalter, S., Knickerbocker, J., Perfecto, E., Garant, J., Knickerbocker, S., Semkow, K., Sundlof, B., Busby, J., Weisman, R., Ruhmer, K., and Hughlett, E., 2008, "C4NP for Pb-Free Solder Wafer Bumping and 3D Fine-Pitch Applications," International Conference on Electronic Packaging Technology and High Density Packaging (ICEPT-HDP), Shanghai, July 28–31.
[23] Mathewson, A., Brun, J., Ponthenier, G., Franiatte, R., Nowodzinski, A., Sillon, N., Poupon, G., Deputot, F., and Dubois-Bonvalot, B., 2007, "Detailed Characterisation of Ni Microinsert Technology For Flip Chip Die on Wafer Attachment," 57th Electronic Components and Technology Conference (ECTC), Reno, NV, May 29-June 1, pp. 616–621.
[24] Mathewson, A., Brun, J., Puget, C., Franiatte, R., Sillon, N., Depoutot, F., and Dubois-Bonvalot, B., 2006, "Microstructured Interconnections for High Security Systems," 1st Electronics Systemintegration Technology Conference, Dresden, Germany, September 5–7, pp. 126–132.
[25] Poupon, G., Sillon, N., Henry, D., Gillot, C., Mathewson, A., Di Cioccio, L., Charlet, B., Leduc, P., Vinet, M., and Batude, P., 2009, "System on Wafer: A New Silicon Concept in SiP," Proc. IEEE, **97**(1), pp. 60–69.
[26] Park, S.-H., Lee, K.-Y., Won, H.-J., Oh, T.-S., and Kim, Y.-H., 2007, "Flip Chip Process Using Mushroom Bumps and Interlocking Bumps," 40th International Symposium on Microelectronics (IMAPS 2007), San Jose, CA, November 11–15, pp. 723–727.
[27] Oh, T. S., Lee, K.-Y., and Won, H.-J., 2009, "Flip-Chip Process Using Interlocking-Bump Joints," IEEE Trans. Compon. Packag. Technol., **32**(4), pp. 909–914.
[28] Jang, D. M., Ryu, C., Lee, K. Y., Cho, B. H., Kim, J., Oh, T. S., Lee, W. J., and Yu, J., 2007, "Development and Evaluation of 3-D SiP With Vertically Interconnected Through Silicon Vias (TSV)," 57th Electronic Components and Technology Conference (ECTC), Reno, NV, May 29–June 1, pp. 847–852.
[29] Souriau, J. C., Castagne, L., Liotard, J., Inal, K., Mazuir, J., Le Texier, F., Fresquet, G., Varvara, M., Launay, N., Dubois, B., and Malia, T., 2012, "3D Multi-Stacking of Thin Dies Based on TSV and Micro-Inserts Interconnections," 62nd Electronic Components and Technology Conference (ECTC), San Diego, CA, May 29–June 1, pp. 1047–1053.
[30] Nowodzinski, A., Boutry, H., Franiatte, R., Mandrillon, V., Anciant, R., Verrun, S., and Simon, G., 2012, "Reliability Tests on Micro-Insert Die Bonding Technology," International Semiconductor Conference Dresden-Grenoble (ISCDG), Grenoble, France, September 24–26, pp. 83–87.
[31] Ebersberger, B., and Lee, C., 2008, "Cu Pillar Bumps as a Lead-Free Drop-In Replacement for Solder-Bumped, Flip-Chip Interconnects," 58th Electronic Components and Technology Conference (ECTC), Lake Buena Vista, FL, May 27–30, pp. 59–66.
[32] Lee, C. H., 2009, "Interconnection With Copper Pillar Bumps: Process and Applications," IEEE International Interconnect Technology Conference (IITC 2009), Sapporo, Japan, June 1–3, pp. 214–216.
[33] Chang, J. Y., Cheng, R. S., Kao, K. S., Chang, T. C., and Chuang, T. H., 2012, "Reliable Microjoints Formed by Solid–Liquid Interdiffusion (SLID) Bonding Within a Chip-Stacking Architecture," IEEE Trans. Compon., Packag. Manuf. Technol., **2**(6), pp. 979–984.
[34] Sa, Y.-K., Yoo, S., Shin, Y.-S., Han, M.-K., and Lee, C.-W., 2010, "Joint Properties of Solder Capped Copper Pillars for 3D Packaging," 60th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, June 1–4, pp. 2019–2024.
[35] Lee, J., Fernandez, D. M., Paing, M., Yeo, Y. C., and Gao, S., 2012, "Electroless Ni Plating to Compensate for Bump Height Variation in Cu-Cu 3-D Packaging," IEEE Trans. Compon., Packag. Manuf. Technol., **2**(6), pp. 964–970.
[36] Tang, Y.-S., Chang, Y.-J., and Chen, K.-N., 2012, "Wafer-Level Cu–Cu Bonding Technology," Microelectron. Reliab., **52**(2), pp. 312–320.
[37] Miller, L. F., 1969, "Controlled Collapse Reflow Chip Joining," IBM J. Res. Dev., **13**, pp. 239–250.
[38] Kripesh, V., Wong Wai, K., and Iyer, M., 2003, "Ultra-Fine Pitch Pb-Free & Eutectic Solder Bumping With Fine Particle Size Solder Paste for Nano Packaging," 5th Electronics Packaging Technology Conference (EPTC 2003), Singapore, December 10–12, pp. 732–737.
[39] Gan, H., Wright, S. L., Polastre, R., Buchwalter, L. P., Horton, R., Andry, P. S., Patel, C., Tsang, C., Knickerbocker, J., Sprogis, E., Pavlova, A., Kang, S. K., and Lee, K. W., 2006, "Pb-Free Microjoints (50 μm Pitch) for the Next Generation Microsystems: the Fabrication, Assembly and Characterization," 56th Electronic Components and Technology Conference (ECTC), San Diego, CA, May 30–June 2.
[40] Dang, B., Shih, D.-Y., Buchwalter, S., Tsang, C., Patel, C., Knickerbocker, J., Gruber, P., Knickerbocker, S., Garant, J., Semkow, K., Ruhmer, K., and Hughlett, E., 2008, "50 μm Pitch Pb-Free Micro-Bumps by C4NP Technology," 58th Electronic Components and Technology Conference (ECTC), Lake Buena Vista, FL, May 27–30, pp. 1505–1510.
[41] Yin, W., Yu, D., Dai, F., Song, C., Bo, Z., Wan, L., Yu, H., and Sun, J., 2012, "Development of Micro-Alloying Method for Cu Pillar Solder Bump by Solid Liquid Interaction," 62nd Electronic Components and Technology Conference (ECTC), San Diego, CA, May 29–June 1, pp. 1709–1714.
[42] Zhan, C.-J., Chuang, C.-C., Juang, J.-Y., Lu, S.-T., and Chang, T.-C., 2010, "Assembly and Reliability Characterization of 3D Chip Stacking With 30 μm Pitch Lead-Free Solder Micro Bump Interconnection," 60th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, June 1–4, pp. 1043–1049.
[43] Ma, S., Sun, X., Zhu, Y., Zhu, Z., Cui, Q., Chen, M., Xiao, Y., Chen, J., Miao, M., Lu, W., and Jin, Y., 2012, "Design and Process Development of a Stacked SRAM Memory Chip Module With TSV Interconnection," 62nd Electronic Components and Technology Conference (ECTC), San Diego, CA, May 29–June 1, pp. 1925–1929.
[44] Bae, H.-C., Choi, K.-S., Eom, Y.-S., Lim, B.-O., Sung, K.-J., Jung, S., Kim, B.-G., Kang, I.-S., and Moon, J.-T., 2010, "3D SiP Module Using TSV and Novel Solder Bump Maker," 60th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, June 1–4, pp. 1637–1641.
[45] Sung, K.-J., Choi, K.-S., Bae, H.-C., Kwon, Y.-H., and Eom, Y.-S., 2012, "Novel Bumping and Underfill Technologies for 3D IC Integration," ETRI J., **34**(5), pp. 706–712.
[46] Sung, K.-J., Choi, K.-S., Lim, B.-O., Bae, H.-C., Choo, S.-W., Moon, J.-T., Kwon, Y. H., Nam, E. S., and Eom, Y.-S., 2010, "Solder Bump Maker With Coining Process on TSV Chips for 3D Packages," 11th International Conference on Electronic Packaging Technology and High Density Packaging (ICEPT-HDP), Xi'an, China, August 16–19, pp. 185–189.
[47] Xie, Y., Cong, J. J., and Sapatnekar, S., 2010, *3D Process Technology Considerations, Three-Dimensional Integrated Circuit Design: EDA, Design and Microarchitectures*, Springer, New York.
[48] Ko, C.-T., and Chen, K.-N., 2012, "Low Temperature Bonding Technology for 3D Integration," Microelectron. Reliab., **52**(2), pp. 302–311.
[49] Morinaga, E., Oka, Y., Nishimori, H., Miyagawa, H., Satoh, R., Iwata, Y., and Kanezaki, R., 2012, "Study of Low Temperature and High Heat-Resistant Fluxless Bonding Via Nanoscale Thin Film Control Toward Wafer-Level Multiple Chip Stacking for 3D LSI," 62nd Electronic Components and Technology Conference (ECTC), San Diego, CA, May 29–June 1, pp. 14–19.
[50] Xie, L., Choi, W. K., Premachandran, C. S., Selvanayagam, C. S., Bai, K. W., Zeng, Y. Z., Ong, S. C., Liao, E., Khairyanto, A., Sekhar, V. N., and Thew, S., 2011, "Design, Simulation and Process Optimization of AuInSn Low Temperature

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TLP Bonding for 3D IC Stacking," 61st Electronic Components and Technology Conference (ECTC), Lake Buena Vista, FL, May 31–June 3, pp. 279–284.

[51] Agarwal, R., Zhang, W., Limaye, P., Labie, R., Dimcic, B., Phommahaxay, A., and Soussan, P., 2010, "Cu/Sn Microbumps Interconnect for 3D TSV Chip Stacking," 60th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, June 1–4, pp. 858–863.

[52] Zhang, W., Limaye, P., Civale, Y., Labie, R., and Soussan, P., 2010, "Fine Pitch Cu/Sn Solid State Diffusion Bonding for Making High Yield Bump Interconnections and Its Application in 3D Integration," 3rd Electronic System-Integration Technology Conference (ESTC), Berlin, September 13–16.

[53] Sakuma, K., Sueoka, K., Kohara, S., Matsumoto, K., Noma, H., Aoki, T., Oyama, Y., Nishiwaki, H., Andry, P. S., Tsang, C. K., Knickerbocker, J. U., and Orii, Y., 2010, "IMC Bonding for 3D Interconnection," 60th Electronic Components and Technology Conference (ECTC), Las Vegas, NV, June 1–4, pp. 864–871.

[54] Zhang, Z., and Wong, C. P., 2004, "Recent Advances in Flip-Chip Underfill: Materials, Process, and Reliability," IEEE Trans. Adv. Packag., **27**(3), pp. 515–524.

[55] Sakuma, K., Kohara, S., Sueoka, K., Orii, Y., Kawakami, M., Asai, K., Hirayama, Y., and Knickerbocker, J. U., 2011, "Development of Vacuum Underfill Technology for a 3D Chip Stack," J. Micromechan. Microeng., **21**(3), p. 035024.

[56] Myo, P., Chong, S. C., Xie, L., Ho, S. W., Toh, W. H. S., and Chai, T. C., 2010, "3D Stacking by Hybrid Bonding With Low Temperature Solder," 12th Electronics Packaging Technology Conference (EPTC), Singapore, December 8–10, pp. 246–250.

[57] Gregory, C., Lueck, M., Huffman, A., Lannon, J. M., and Temple, D. S., 2012, "High Density Metal-Metal Interconnect Bonding With Pre-Applied Fluxing Underfill," 62nd Electronic Components and Technology Conference (ECTC), San Diego, CA, May 29–June 1, pp. 20–25.

[58] Nimura, M., Mizuno, J., Sakuma, K., and Shoji, S., 2011, "Solder/Adhesive Bonding Using Simple Planarization Technique for 3D Integration," 61st Electronic Components and Technology Conference (ECTC), Lake Buena Vista, FL, May 31–June 3, pp. 1147–1152.

[59] Nimura, M., Mizuno, J., Shigetou, A., Sakuma, K., Ogino, H., Enomoto, T., and Shoji, S., 2013, "Hybrid Au-Au Bonding Technology Using Planar Adhesive Structure for 3D Integration," 63rd Electronic Components and Technology Conference (ECTC), Las Vegas, NV, May 28–31, pp. 1153–1157.

[60] Nimura, M., Mizuno, J., Shigetou, A., Sakuma, K., Ogino, H., Enomoto, T., and Shoji, S., 2013, "Study on Hybrid Au-Underfill Resin Bonding Method With Lock-and-Key Structure for 3-D Integration," IEEE Trans. Compon., Packag. Manuf. Technol., **3**(4), pp. 558–565.

[61] Kohara, S., Horibe, A., Sueoka, K., Matsumoto, K., Yamada, F., Orii, Y., Sakuma, K., Kinoshita, T., and Kawakami, T., 2012, "Thermal Stress Analysis of Die Stacks With Fine-Pitch IMC Interconnections for 3D Integration," IEEE International 3D Systems Integration Conference (3DIC), Osaka, Japan, January 31–February 2.

[62] Dong, X., and Xie, Y., 2009, "System-Level Cost Analysis and Design Exploration for Three-Dimensional Integrated Circuits (3D ICs)," 14th Asia and South Pacific Design Automation Conference (ASP-DAC 2009), Yokohama, Japan, January 19–22, pp. 234–241.

[63] Chen, Y., Niu, D., Xie, Y., and Chakrabarty, K., 2010, "Cost-Effective Integration of Three-Dimensional (3D) ICs Emphasizing Testing Cost Analysis," IEEE/ACM International Conference on Computer-Aided Design (ICCAD), San Jose, CA, November 7–11, pp. 471–476.

[64] Lecarpentier, G., Agarwal, R., Wenqizhang, Limaye, P., Labie, R., Phommahaxay, A., and Soussan, P., 2010, "Die-to-Wafer Bonding of Thin Dies Using a 2-Step Approach; High Accuracy Placement, Then Gang Bonding," 6th International Conference and Exhibit on Device Packaging, Scottsdale/Fountain Hills, AZ, March 7–11.

[65] Ko, C.-T., and Chen, K.-N., 2010, "Wafer Level Bonding/Stacking Technology for 3D Integration," Microelectron. Reliab., **50**(4), pp. 481–488.

[66] Ko, C.-T., Hsiao, Z.-C., Chang, Y.-J., Chen, P.-S., Hwang, Y.-J., Fu, H.-C., Huang, J.-H., Chiang, C.-W., Sheu, S.-S., Chen, Y.-H., Lo, W.-C., and Chen, K.-N., 2012, "A Wafer-Level Three-Dimensional Integration Scheme With Cu TSVs Based on Microbump/Adhesive Hybrid Bonding for Three-Dimensional Memory Application," IEEE Trans. Device Mater. Reliab., **12**(2), pp. 209–216.

[67] Chang, Y. J., Ko, C. T., Hsiao, Z. C., Yu, T. H., Chen, Y. H., Lo, W. C., and Chen, K. N., 2012, "Electrical Characterization and Reliability Investigations of Cu TSVs With Wafer-Level Cu/Sn-BCB Hybrid Bonding," International Symposium on VLSI Technology, Systems, and Applications (VLSI-TSA), Hsinchu, Taiwan, April 23–25.

[68] Huyghebaert, C., Van Olmen, J., Civale, Y., Phommahaxay, A., Jourdain, A., Sood, S., Farrens, S., and Soussan, P., 2010, "Cu to Cu Interconnect Using 3D-TSV and Wafer to Wafer Thermocompression Bonding," 2010 International Interconnect Technology Conference (IITC), Burlingame, CA, June 6–9.

[69] Liu, F., Yu, R. R., Young, A. M., Doyle, J. P., Wang, X., Shi, L., Chen, K. N., Li, X., Dipaola, D. A., Brown, D., Ryan, C. T., Hagan, J. A., Wong, K. H., Lu, M., Gu, X., Klymko, N. R., Perfecto, E. D., Merryman, A. G., Kelly, K. A., Purushothaman, S., Koester, S. J., Wisnieff, R., and Haensch, W., 2008, "A 300-mm Wafer-Level Three-Dimensional Integration Scheme Using Tungsten Through-Silicon Via and Hybrid Cu-Adhesive Bonding," IEEE International Electron Devices Meeting (IEDM 2008), San Francisco, CA, December 15-17.

[70] Swinnen, B., Ruythooren, W., De Moor, P., Bogaerts, L., Carbonell, L., De Munck, K., Eyckens, B., Stoukatch, S., Sabuncuoglu Tezcan, D., Tokei, Z., Vaes, J., Van Aelst, J., and Beyne, E., 2006, "3D Integration by Cu-Cu Thermo-Compression Bonding of Extremely Thinned Bulk-Si Die Containing 10 μm Pitch Through-Si Vias," International Electron Devices Meeting (IEDM '06), San Francisco, CA, December 11–13.

[71] Diehl, D., Kitada, H., Maeda, N., Fujimoto, K., Ramaswami, S., Sirajuddin, K., Yalamanchili, R., Eaton, B., Rajagopalan, N., Ding, R., Patel, S., Cao, Z., Gage, M., Wang, Y., Tu, W., Kim, S. W., Kulzer, R., Drucker, I., Erickson, D., Ritzdorf, T., Nakamura, T., and Ohba, T., 2012, "Formation of TSV for the Stacking of Advanced Logic Devices Utilizing Bumpless Wafer-on-Wafer Technology," Microelectron. Eng., **92**, pp. 3–8.

[72] Fujimoto, K., Maeda, N., Kitada, H., Kim, Y. S., Kodama, S., Nakamura, T., Suzuki, K., and Ohba, T., 2012, "Development of Cost-Effective Wafer Level Process for 3D-Integration With Bump-Less TSV Interconnects," 62nd Electronic Components and Technology Conference (ECTC), San Diego, CA, May 29–June 1, pp. 537–540.

[73] Kitada, H., Maeda, N., Fujimoto, K., Suzuki, K., Kawai, A., Arai, K., Suzuki, T., Nakamura, T., and Ohba, T., 2009, "Stress Sensitivity Analysis on TSV Structure of Wafer-on-a-Wafer (WOW) by the Finite Element Method (FEM)," IEEE International Interconnect Technology Conference (IITC), Sapporo, Japan, June 1–3, pp. 107–109.

[74] Ramm, P., Lu, J. J.-Q., and Taklo, M. M. V., 2012, *Handbook of Wafer Bonding*, Wiley-VCH, Weinheim, Germany.

[75] Chatterjee, R., Fayolle, M., Leduc, P., Pozder, S., Jones, B., Acosta, E., Charlet, B., Enot, T., Heitzmann, M., Zussy, M., Roman, A., Louveau, O., Maitrejean, S., Louis, D., Kernevez, N., Sillon, N., Passemard, G., Po, V., Mathew, V., Garcia, S., Sparks, T., and Zhihong, H., 2007, "Three Dimensional Chip Stacking Using a Wafer-to-Wafer Integration," IEEE International Interconnect Technology Conference (IITC), Burlingame, CA, June 4–6, pp. 81–83.

[76] Bernstein, K., Andry, P., Cann, J., Emma, P., Greenberg, D., Haensch, W., Ignatowski, M., Koester, S., Magerlein, J., Puri, R., and Young, A., 2007, "Interconnects in the Third Dimension: Design Challenges for 3D ICs," 44th ACM/IEEE Design Automation Conference (DAC '07), San Diego, CA, June 4–8, pp. 562–567.

[77] Skordas, S., Tulipe, D. C. L., Winstel, K., Vo, T. A., Priyadarshini, D., Upham, A., Song, D., Hubbard, A., Johnson, R., Cauffman, K., Kanakasabapathy, S., Lin, W., Knupp, S., Malley, M., Farooq, M. G., Hannon, R., Berger, D., and Iyer, S. S., 2012, "Wafer-Scale Oxide Fusion Bonding and Wafer Thinning Development for 3D Systems Integration: Oxide Fusion Wafer Bonding and Wafer Thinning Development for TSV-Last Integration," 3rd IEEE International Workshop on Low Temperature Bonding for 3D Integration (LTB-3D), Tokyo, May 22–23, pp. 203–208.

[78] Pozder, S., Chatterjee, R., Jain, A., Huang, Z., Jones, R. E., and Acosta, E., 2007, "Progress of 3D Integration Technologies and 3D Interconnects," IEEC International Interconnect Technology Conference (IITC), Burlingame, CA, June 4–6, pp. 213–215.

[79] Enquist, P., Fountain, G., Petteway, C., Hollingsworth, A., and Grady, H., 2009, "Low Cost of Ownership Scalable Copper Direct Bond Interconnect 3D IC Technology for Three Dimensional Integrated Circuit Applications," IEEE International Conference on 3D System Integration (3DIC 2009), San Francisco, CA, September 28–30.

[80] Donabedian, D. L., Enquist, P., and Sanders, C., 2008, "Ziptronix Pioneering 3D Integrated Circuit Process Technology," i-Micronews, http://www. i-micronews.com/lectureArticle.asp?id=2009

[81] Radu, I., Landru, D., Gaudin, G., Riou, G., Tempesta, C., Letertre, F., Di Cioccio, L., Gueguen, P., Signamarcheix, T., Euvrard, C., Dechamp, J., Clavelier, L., and Sadaka, M., 2010, "Recent Developments of Cu-Cu Non-Thermo Compression Bonding for Wafer-to-Wafer 3D Stacking," IEEE International 3D Systems Integration Conference (3DIC), Munich, Germany, November 16–18.

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