Open access • Book Chapter • DOI:10.1007/978-3-7091-0624-2_17

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Published on: 01 Jan 2004

Topics: Shallow trench isolation, Dram and Trench

Three-Dimensional Characterization and Modeling of Stress Distribution in High-Density DRAM Memory Cells

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Abstract

The retention time characteristics in DRAM cells are strongly influenced by various leakage mechanisms near the storage node junction. In this work, we present a full three-dimensional analysis of stress distributions in and around the active area of high-density memory cells. We use a combination of high-resolution metrology analysis and 3D numerical modeling to provide quantitative estimates. Since shallow-trench isolation (STI) process used in high-density cells is one of the major contributors to stress, we study the effects of various materials used to fill the trench. Our electron diffraction contrast (EDC) methodology provides a spatial resolution on the order of 10 nm with sensitivity on of the order of tens of MPa and therefore useful for the analysis of scaled high density memory cells.

1. Introduction

Aggressive scaling of cell size in gigabit density DRAM design places an increasing demand in modeling both the process flow and the electrical characteristics of devices. In particular, since the array transistor in a DRAM cell has both small gate length and small width, it requires sophisticated 3D modeling. In a stacked capacitor cell technology, mechanical stress in the active area near the cell capacitor junction significantly affects the refresh characteristics of the memory cell. This is a growing concern for sub-100nm gate length DRAM devices. Earlier work in this area is far from adequate in quantitatively understanding the stress distributions in high-density DRAM cells [1-4]. Therefore, it is necessary to quantitatively model and measure the stresses as well as analysis of its origin, which can provides us a guideline for future device design and process development. In this paper, we present a technique that combines Focused Ion Beam (FIB) technique, quantitative Electron Diffraction Contrast (EDC) and Finite Element modeling (FEM) to measure stresses with a spatial resolution on the order of 10 nm and sensitivity on the order of tens of MPa.

2. Experimental and Simulations

As a first part of the experiment, FIB is used to make a cross-section of the device of interest with the uniform thickness. An experimental EDC image of the device is obtained under known TEM conditions by using charge coupled device (CCD) camera to minimize any nonlinear effects from the photographic processing. Then an accurate 3D FEM structure was built using ANSYS 7.1 [5] by knowing the

topography information from multiple TEM cross sections and the thickness of the thin films used in the process flow. Tencor FLX -2320 system was used for the wafer curvature measurements to provide us the intrinsic stress values for each of the component material, which was deposited on the bare silicon wafer at exact process condition. Table 1 shows the intrinsic stress value for materials used in the FE analysis. Stress is introduced in the ANSYS model by applying an artificial temperature change and modified thermal expansion coefficient, which are both scaled to represent blanket wafer stress. Then we used SIMCON [6] to do the EDC image simulations. SIMCON uses FEM field output data including the original position and displacement vectors for each of the nodes in the FE model, the experimental data obtained from TEM and resulting EDC, to create a simulated EDC image. The principle of the simulation method is to let the electrons to pass through the discrete columns in the material under the Howie–Whelan equations for 2-beam dynamical electron diffraction condition [7]. A difference map is then created and calibrated in terms of stress differences between the resulting simulated image and the experimental image. Stresses of all component materials are varied in ANSYS simulations, and then a series of SIMCON images are produced until the closest match is found between these two images. By plugging these best conditions back to ANSYS 3D stress simulation, a final quantitative stress distribution is obtained [8].

3. Results and Discussion

Fig. 1 is a schematic top-down view of AA in an $8F^2$ DRAM cell and a complex 3D model built using the above method. Fig. 2 shows similar views for a $6F^2$ DRAM cell. The experimental TEM dark field image and SIMCON modeled image are shown in Fig. 3 (a) and (b) respectively. A close pixel-to-pixel match between these two images gives us confidence in our methodology. In Fig. 4, one can see the average difference of the gray scale between the real and simulated image with the uniform change of the wafer curvature load of gate stacks and STI fill materials. The minimum of the average gray scale difference occurs at 130% of the blank wafer curvature load of those materials. Fig. 5 shows stress-xx (lateral in plane of the page) and stress-yy (vertical in plane of the page) profiles along the cut line CD and AB in Fig. 1 (b) respectively with the different STI fill option. Our results show that the mechanical stress in the AA mainly comes from the shallow trench isolation (STI) regions. Gate stacks also have some impact. The fill material used inside the STI has a large impact on stress. While some of the films considered here lead to compressive stress, others lead to tensile stress. If the region is filled with larger compressive stress oxide, the cell transistor threshold voltage increase is observed due to the higher stress inside AA [2]. Stress cancellation effects when multiple films are used can be adequately characterized by our methodology. Fig. 6 shows the effect of a tensile film inside the STI, which can reduce the stress by 40% in the AA region near the STI boundary region. When a compressive oxide film is deposited on top of this film, the compensation effects can be clearly seen. The difference in stress contours between two different DRAM cell architectures for identical gate length and STI trench depth are shown in Figs. 7 and 8. It is clear that the layout of the cell influences the stress characteristics in the active area. Figs. 9 and 10 show experimental results for the storage node diode leakage current and data retention time for two different STI fills with varying compressive stress. It is clear that optimized STI fills lead to improved leakage current and retention time characteristics.

4. Conclusion

Stress profiles in a high density DRAM array are simulated and characterized by a combination of complex 3D ANSYS simulation and quantitative EDC method leading to a the spatial resolution of 10nm and sensitivity of order 10MPa. Our results show that stress in the AA is mainly from STI region, if the STI region is filled with lower compressive stress oxide or add a tensile stress film, the diode leakage current will reduce which improves the data retention time.

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Materials	Si	Poly-Si	Nitride	STI Fill-A	STI Fill-B	STI Fill-C	SiO2
Intrinsic Stress (Mpa)	0 (As reference)	190	-1020	220	108	53	105

Table 1. The intrinsic stresses measured for some materials for FE analysis. Positive value means compressive stress.

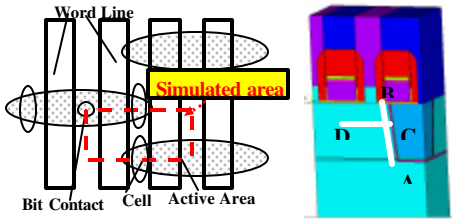

Fig. 1 (a) A schematic top-down view of AA in an $8F^2$ DRAM cell. (b) 3-D ANSYS model of the DRAM array. AB and CD are the cut lines used for the stress analysis in Fig. 5.

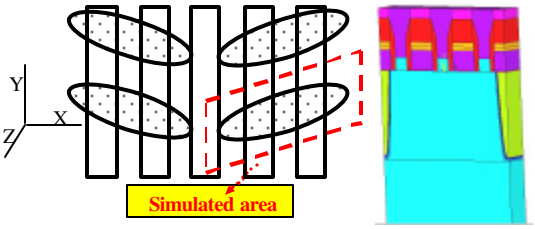

Fig. 2 (a) A schematic top-down view of AA in a $6F^2$ DRAM cell. (b) 3-D ANSYS model of the DRAM array.

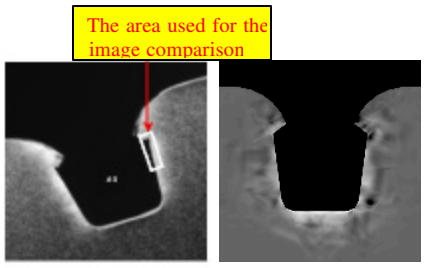

Fig. 3 Experimental (a) and simulated (b) (220) Dark Field TEM image of STI region in $8F^2$ DRAM array.

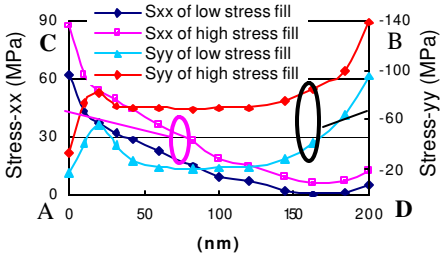

Fig. 5 ANSYS stress-xx and yy profile along cut line CD and AB respectively with different STI fills.

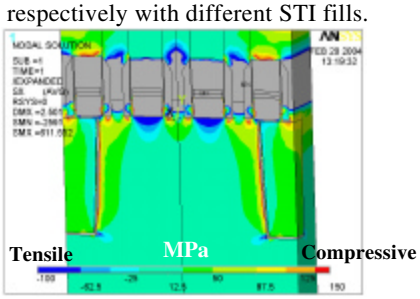

Fig. 7 σxx direction (horizontal) stress tensor component from FEM analysis of $8F^2$ DRAM cell.

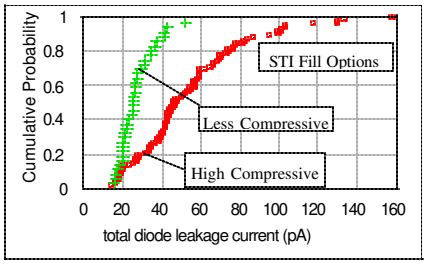

Fig. 9 Diode leakage (cell side) current characteristics from a test structure containing multiple memory cells.

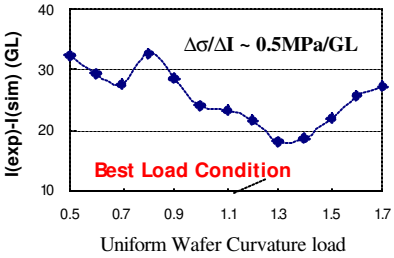

Fig. 4 Plot of average grayscale difference between Fig. 3(a) and (b) as a function of uniform change of stress load of the component materials. Wafer curvature load of 1.0 represents the blanket film wafer stress.

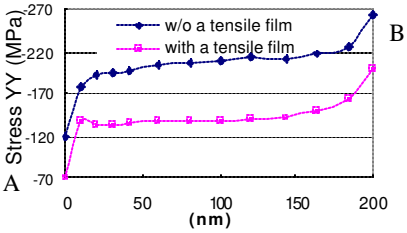

Fig. 6 The stress-yy along AB with and without a tensile film in the STI

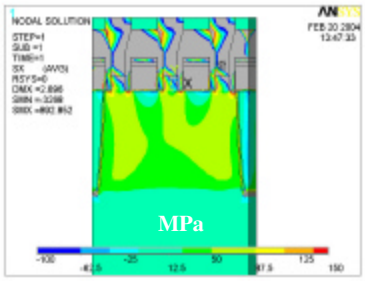

Fig. 8 σxx direction (horizontal) stress tensor component from FEM analysis of $6F^2$ DRAM cell.

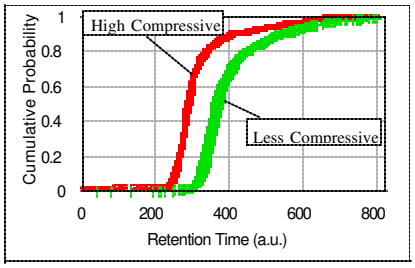

Fig. 10 Data retention time improvement with optimized STI fills.