Three-Dimensional System-in-Package Using Stacked Silicon Platform Technology

Vaidyanathan Kripesh, *Member, IEEE*, Seung Wook Yoon, *Member, IEEE*, V. P. Ganesh, *Member, IEEE*, Navas Khan, Mihai D. Rotaru, *Member, IEEE*, Wang Fang, and Mahadevan K. Iyer, *Senior Member, IEEE*

***Abstract*—In this paper, a novel method of fabricating three–dimensional (3-D) system-in-package (SiP) using a silicon carrier that can integrate known good dice with an integrated cooling solution is presented. The backbone of this stacked module is the fabrication of a silicon carrier with through-hole conductive interconnects. The design, process, and assembly to fabricate silicon through-hole interconnect using a wet silicon etching method is discussed in this paper. The process optimization to fabricate silicon carriers with solder through-hole interconnect within the design tolerance has been achieved. The design and modeling methodology to optimize the package in terms of electrical aspects of the stacked module is carried out to achieve less interconnect parasitics. An integrated cooling solution for 3-D stacked modules using single-phase and two-phase cooling solutions is also demonstrated for high-power applications. Known good thin flip-chip devices with daisy chain are fabricated and attached to the silicon carrier by flip-chip processes making it a known good carrier after electrical testing. Individual known good carriers are vertically integrated to form 3-D SiP.**

***Index Terms*—Three-dimensional system-in-package (3-D SiP), stacked modules, through wafer interconnection, wafer thinning, integrated cooling solution.**

I. Introduction

PORTABLE electronic products demand integration of different functional chips like digital, RF, and optical in a single module. Integration of multifunctional chips on silicon, organic, and ceramic substrates for system-in-package (SiP) is a fast emerging technology. Presently, chip-level and package-level stacked modules are primarily used for memory modules [1]. In chip stacking technology, different size dies are stacked in a pyramid structure or same size dice are stacked with spacer technology [2]. In package-level stacking, thin packages are stacked one over the other [3]. However, mass manufacturability, quick turn-around time, integrated thermal management, and electrical testing are the major bottlenecks for the above technologies.

Wafer-level stacking technologies are also being researched [4], [5] for memory modules and system-level integration. The key challenges are integration of cooling solutions, stacking of different size devices, interconnect reliability, and process compatibility to wafer-level integration. Novel methods of stacking different size dies vertically on silicon carriers with an integrated cooling solution are presented in this paper.

SiP technologies of the future will require integration of silicon, GaAs, Si–Ge chips for multiple functionalities like digital, RF, optical, and bio microelectromechanical systems (MEMS). The interposer should have good electrical, thermal, and mechanical properties and shall be manufacturable at low cost. This paper addresses some of these challenges, and the results are reported.

II. Silicon Stacked Modules: Concept and Test Vehicle Description

A three-layer stacked module is developed using silicon as a carrier. The interconnections through the silicon carrier are developed by solder via fill technology (SVFT). Fig. 1 shows a schematic of the test vehicle designed for the research. The test vehicle has 11 thin chips of 100 μm thickness. Three silicon carriers of 10 $\times$ 10 mm are designed for routing the signals and interconnection from one layer to another. Each carrier has 100 through-hole vias along the periphery of the carrier, vias are etched using KOH having dimensions of 630 μm at the bottom side is known as bumps-side of the carrier and 100 μm at the top side is known as chip-side of the carrier. The bottom and top carrier are assembled with one flip-chip each of size 8 $\times$ 8 mm, the middle carrier has nine dice of size 3 $\times$ 3 mm. The flip-chip dice are bumped at 200-μm pitch using eutectic SnPb solder. Three carriers are stacked on an organic substrate for electrical and reliability characterization.

Electrical performance of the interconnects are optimized using a 3-D full wave solver. Interconnects in the silicon carrier are designed to have low insertion loss and maximum operating frequency up to 10 GHz. The processes for the SVFT and vertical stacking of silicon carriers are challenging. Novel processes are developed for realizing SVFT. Typically, total heat dissipation from the stacked module is about 1 watt in natural convection. Integrated cooling solutions are required for high-performance applications. A detailed study conducted on electrical, process, and assembly and cooling solution for the silicon stacked module and the results obtained are reported under the following sections:

1) interconnect electrical design and characterization;
2) process and assembly;
3) integrated cooling solutions.

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V. Kripesh, S. W. Yoon, V. P. Ganesh, N. Khan, M. D. Rotaru, and M. K. Iyer are with the Institute of Microelectronics, Singapore Science Park II, Singapore 117685 (e-mail: kripesh@ime.a-star.edu.sg).

W. Fang is with the Institute of High Performance Computing, Singapore Science Park II, Singapore 117528.

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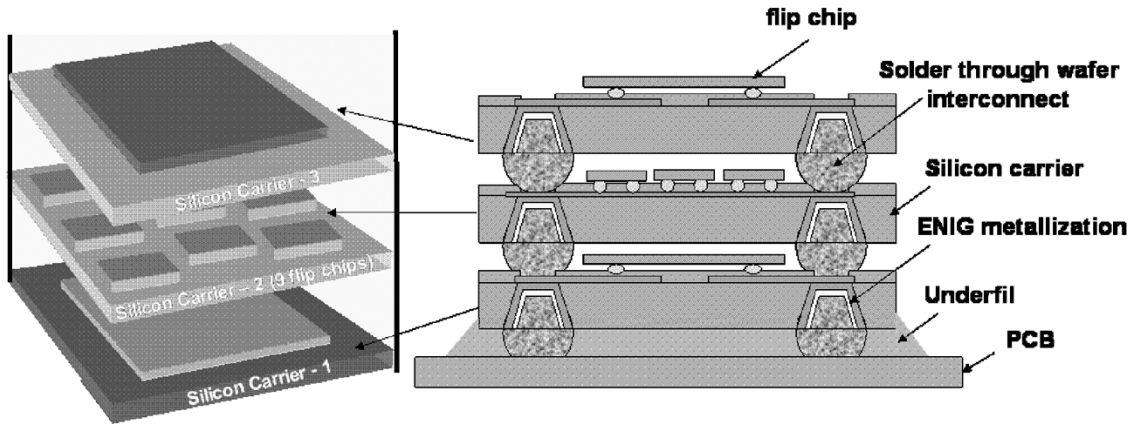


Fig. 1. Three-dimensional SiP test vehicle chosen for the study.

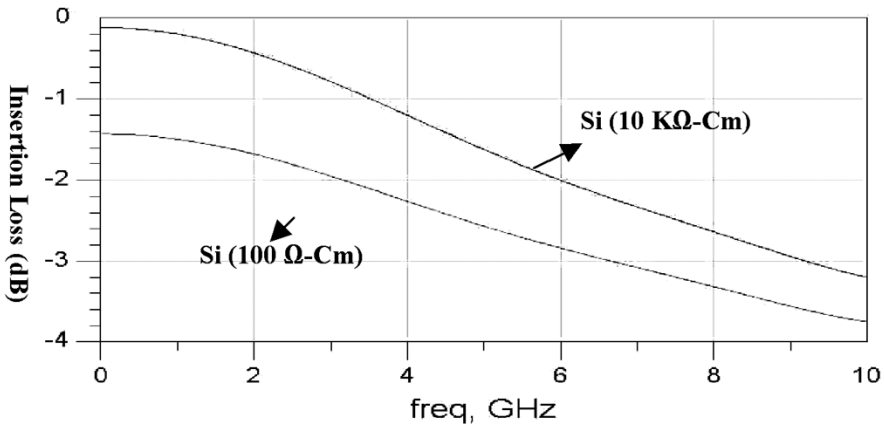


Fig. 2. Influence of the silicon substrate over the transmission loss of the 3-D through-wafer interconnects.

III. Interconnect Electrical Design and Characterization

Electrical characterization of the through-hole via interconnects plays a significant role in the high-frequency performance assessment of 3-D modules. In order to compare the behavior and performance of the through-hole via with respect to other types of interconnect, a simple ground, signal, ground (GSG) configuration has been chosen. This configuration can be easily integrated with transmission line structures like microstripline or coplanar wave guide (CPW) through which the via through interconnect can be excited.

One of the most important factors of an interconnect is matching its impedance with the transmission lines. For high-speed applications, the mismatch in the interconnect chain is one of the limiting factors. A 3-D full-wave solver has been used for this purpose. Three-dimensional models of the GSG via interconnect with a diameter of 600 μm on a 50-Ω CPW transmission line has been developed. The distance between signal and ground has been used as the variable parameter in optimizing the pitch.

Another important factor that has been studied by the full-wave simulation is the influence of silicon electrical resistivity. The simulation results showed that a high-resistive silicon substrate is required for high-frequency signal transmission. Typically, 10 kΩ-cm resistivity silicon wafer is required, and the insertion losses are compared with a normal silicon wafer in Fig. 2. Based on our simulation results, a wafer with through-hole vias has been fabricated for the electrical characterization and measurements. An FR4 test board with 50-ΩCPW transmission line has been fabricated. The test chips with the GSG configuration have been mounted on the board and measured in the frequency domain. The influence of the board over the measured results has been removed through a deembedding procedure in the post processing stage. The measured data have been used to extract an equivalent lumped circuit of the through-hole via interconnect, and the results showed a very small resistance and self inductance ($R = 15$ mΩ, $L = 0.09$ nH) which are ideal for high-speed interconnect applications.

IV. Process and Assembly

For realizing a stacked silicon module, process development and optimization in each of the assembly processes are carried out. The process and assembly details are discussed in the following three sections:

1) Si carrier with through-wafer interconnection fabrication using solder via fill technology;
2) wafer thinning—carrier wafer and thin bumped test devices fabrication;
3) stacking and module integration.

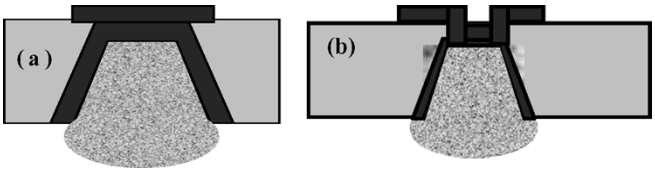


Fig. 3. (a) Via structure for coarse pitch using total wet etch process. (b) For fine-pitch applications, a combination wet etch and dry processes are carried out.

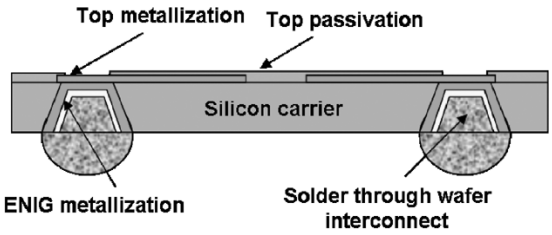


Fig. 4. Carrier with solder interconnect [8].

A. Silicon Carrier Fabrication Using Solder Via Fill Technology

Silicon carrier with through-hole interconnect is the key element in the test vehicle. The wet etch method is used to form the through-hole via in the carrier and the via is filled and bumped using our novel approach of SVFT. The four-step process developed for the carrier fabrication is: 1) through-hole via formation by KOH wet etch; 2) via metallization and under bump metallization; 3) carrier thinning and via exposure; and 4) via filling and bumping. Two types of via designs are evaluated for fine-pitch and coarse-pitch applications. Fig. 3 shows a cross section of both the via designs. Suitable via is selected depending on the chip size and I/O density. For coarse-pitch applications, the single wet etch process approach is adopted [Fig. 3(a)], and for fine-pitch applications, a combination of wet etch and the front-side dry etch pad exposing method is adopted [Fig. 3(b)]. Fig. 4 shows the schematics of the silicon carrier with top metallization, top passivation, and through-hole interconnections. The advantage of SVFT is that the through hole can be filled and bumped in a single process step.

The process sequence for the silicon carrier fabrication and via filling is shown in Fig. 5. KOH is used to etch the via trenches in a 650-μm-thick 6-in wafer. Low pressure (LP) nitride over thermal oxide is used as the etch mask, and it is patterned using dry etch at the via trench opening locations. A controlled KOH etch batch process is carried out in a custom-made etching chamber, followed by the removal of etch mask. Then, the wafer is passivated by plasma-enhanced tetraethylorthosilicate (PETEOS) oxide of 5000 Å thickness. A blanket Ti/Cu seed layer is then sputtered on top of the PETEOS oxide. The sputtered Ti/Cu is patterned to deposit a thick electroless nickel immersion gold (ENIG) metallization along the walls of the through-hole vias. Ti/Cu is patterned using spin-coated photo resist (PR) that resulted in defects such as streak formation and accumulation of resist at the bottom of the through-hole via leading to nonuniform Cu/Ti etching. A novel PR printing process is developed to overcome the non uniform Ti/Cu etching. The PR chemical is deposited and

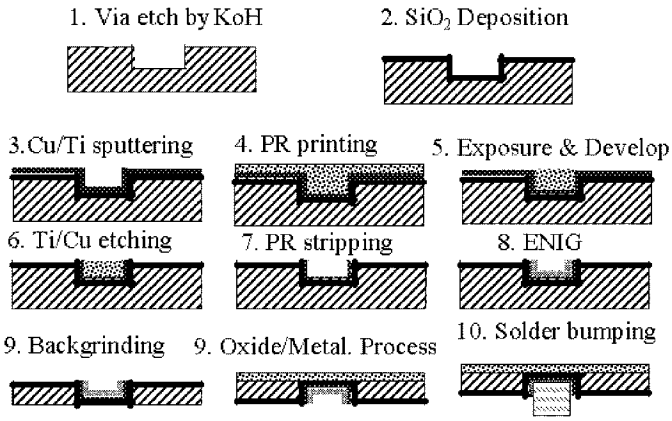


Fig. 5. Schematic wafer process flow for SVFT.

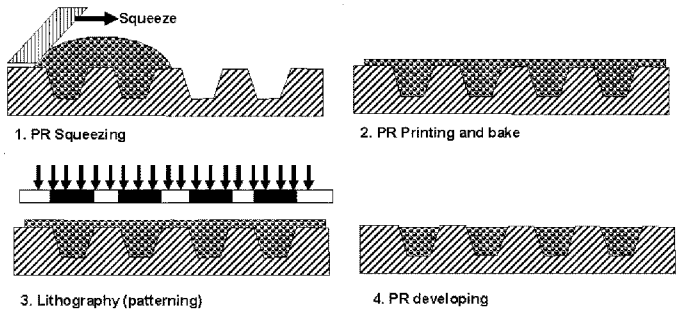


Fig. 6. Process steps for PR printing process. 1) PR squeezing. 2) PR printing and bake. 3) Lithography (patterning). 4) PR developing.

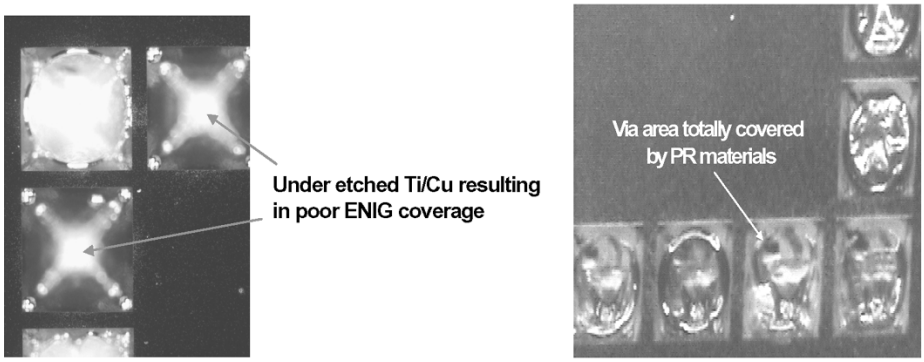
squeezed with a rubber blade then baked on a hot plate, which is followed by the lithography process, and the Ti/Cu is etched using a wet etch process as shown in Fig. 6. The ENIG-plated vias by the conventional process and new process is compared in Fig. 7.

A thick ENIG layer is deposited on the patterned Ti/Cu to form wetting layer for the solder fill. The via is exposed at the back side of the wafer by grinding and polishing. The thick ENIG is required to withstand the grinding and polishing forces. The via exposure process is an important process step and requires good thickness monitoring while back grinding. After the via exposure, the PETEOS oxide of 5000Å is deposited and patterned for electrical isolation. Ti/Al is deposited on the chip side of the carrier and patterned to connect the device bump pads to the through hole interconnect. Then, the via is filled with SnPb eutectic solder by the ball placement or stencil printing process. Fig. 8 shows the cross-section view and top view of final solder interconnection after the reflow process.

B. Wafer Thinning

Wafer thinning is one of the important steps for silicon carrier and flip-chip fabrication. In this paper, conventional and low-cost mechanical back grinding (BG) with stress relieving by slurry polishing process is used.

1) Silicon Carrier: Mechanical BG and polishing is done on the back side of the wafer, after the via etched wafer is plated with the thick ENIG. The purpose of BG and polishing is to expose via from the backside of the wafer so that further processes of silicon carrier fabrication can be done. Two schemes



(a) (b)

Fig. 7. (a) Shows the improper ENIG plating in the via walls when Cu/Ti is patterned by conventional photo resist spin-coating method. (b) Picture of via totally covered with PR material after lithography and developing.

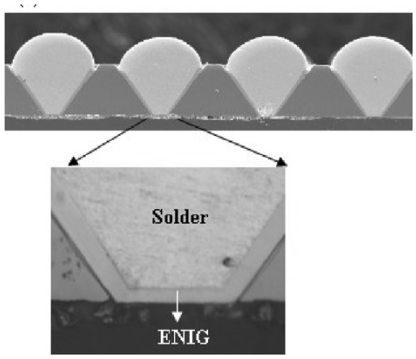


Fig. 8. Micrographs of solder via interconnection.

are evaluated for via exposure: 1) direct via exposure by BG and polishing and 2) combination of BG, polishing, and dry etching. The comparison of both schemes is shown in Fig. 9. Via depth variation and good total thickness variation (TTV) control in the BG and polishing process determines the yield and success of via exposure directly by grinding and polishing. During the via exposure process punctured via, unexposed via are observed as common defects in this method as shown in Fig. 10.

Energy-dispersive X-ray (EDX) analysis is carried out in the properly exposed via to understand the composition of the metallization after BG and polishing. Fig. 11 shows the EDX results that reveal the presence of Ni in the via-exposed area. In the combination of BG, polishing, and dry etching method, thinning is done until a desired thickness of silicon is left on top of the via, so that further via exposure is continued by the dry etching process. In this method, the problem of punctured via and unexposed via are eliminated. Fig. 12 shows the result of via exposure by this method. Both the schemes have their own advantages and disadvantages. Comparison of via exposure directly by BG and polishing and combination of BG, polishing, and dry etching is given in Table I.

2) Thin Bumped Test Devices: Test wafers with four daisy chain chips with peripheral, depopulated, and fully populated test structures are fabricated by conventional wafer bumping processes. The bump pitch for the entire test die is 200 μm with bump height of 80 μm. Eutectic tin/lead is used for the solder bumping. BG tape selection is done considering the bump height

TABLE I
COMPARISON OF VIA EXPOSURE BY TWO SCHEMES

Direct via exposure by BG and polishing	Combination of BG, polishing and dry etching
Reduced process steps and time	Increased process steps and time
Mask less process	Requires litho processes for silicon etch followed by SiO2 etch
Does not take care of via depth variation caused during KOH trench etching of wafer	Even if there is via depth variation dry etching process can be continued until all the via are exposed
Yield loss due to some via unexposed or over grinded	No Yield loss
Needs thicker Electroless Ni layer to take the grind and polish load and to act as a buffer layer to take care of via depth variation	Thin Electroless Ni can be used
For coarse pitch application	Fine pitch through hole via can be fabricated

Fig. 9. (a) Showing via exposure directly by grinding and polishing. (b) Via exposure by combination of BG, polishing, and dry etching.

and the cushion layer thickness of the BG tape. The bumped wafer is laminated with the selected BG tape. Tthe tape lamination process is optimized to obtain bubble-free lamination. Fig. 13 shows a BG tape laminated bumped wafer without entrapped air. Wafers are thinned to 100 μm with optimized BG process parameters [6]. Total thickness variation (TTV) across the wafer is measured by the "TTV measurement by dicing" method [7]. A TTV value of 1.8 μm in a 6-in wafer is achieved through process optimization, and the measured TTV graph is shown in Fig. 14. The thinned bumped wafer with the BG tape is laminated onto the dicing tape after which the BG tape is removed and the test wafer is diced. Fig. 15 shows a picture of the thinned test die fabricated for the research.

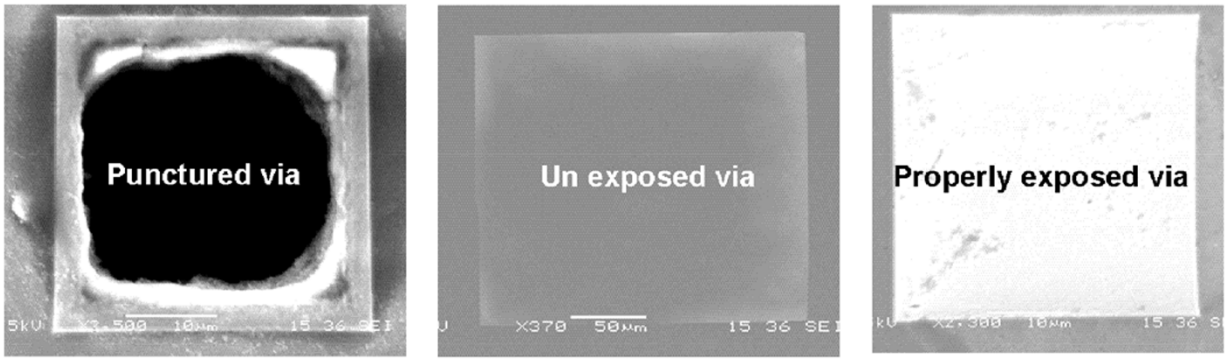


Fig. 10. SEM of punctured, unexposed, and properly exposed via during direct via exposure by BG and polishing method.

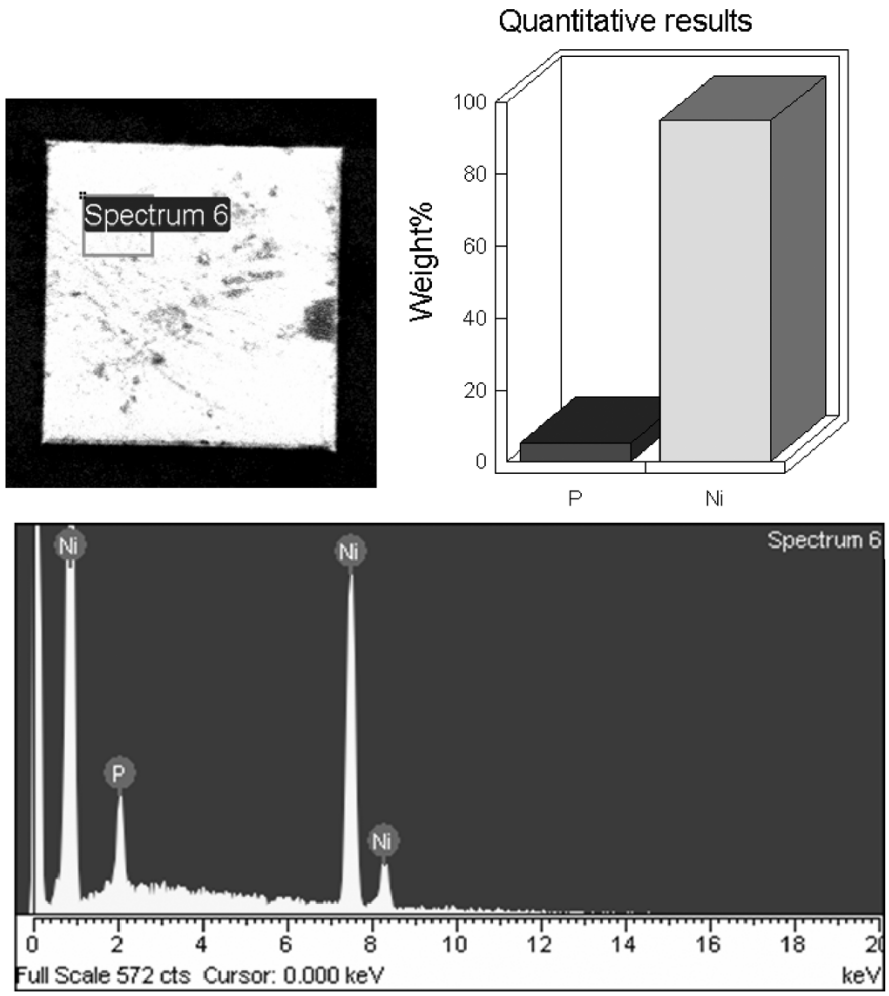


Fig. 11. EDX results of the via by direct via exposure by BG and polishing method.

C. Stacking and Module Integration

Thin test devices are flip-chip attached onto the silicon carrier using conventional a flip-chip attach process. The test devices are tested by conventional wafer-level testing for known good die (KGD). Flip-chip attach is done in an automatic flip-chip bonder where the chip in the waffle pack is picked up by a pickup tool followed by prealign, flux dip, align with silicon carrier wafer, and bonding processes. Once the flip-chip is placed on the silicon carrier wafer, the carrier is reflowed in a reflow oven. Each stack assembly is checked for electrical resistance continuity by probing the daisy chain from each flip-chip dies on each silicon carrier wafer and from the bump of the through wafer interconnects. The assembled carrier wafer is tested for known good carrier assembly and sorted before the module stacking.

Three silicon carriers with flip-chip are stacked vertically to make the 3-D stacked module. First, the bottom carrier assembly is attached to the PCB and under filled. The middle carrier and top carrier assembly is attached over the bottom stack assembly using the flip-chip bonder. Fig. 16 shows the cross-section view of the stacked module assembled. The assembled module is tested for the electrical continuity through the three levels of SVFT interconnections and found to have a good yield.

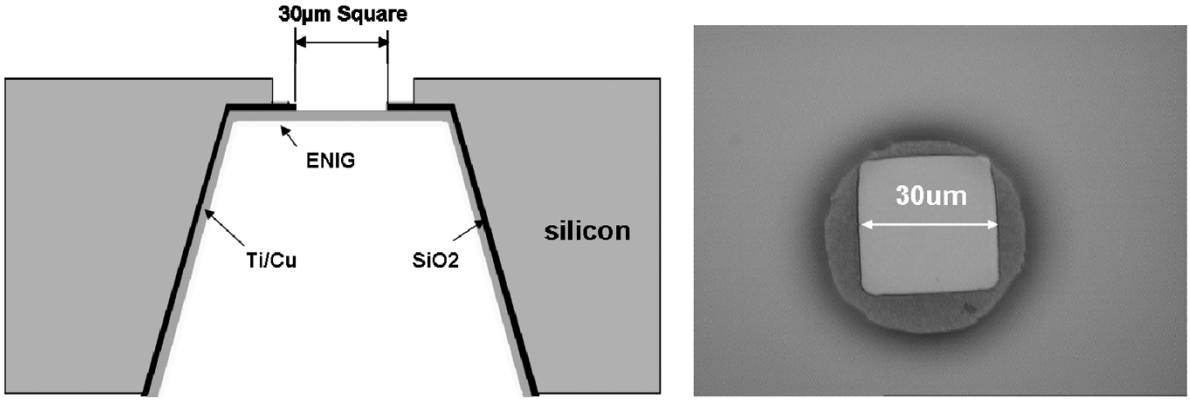


Fig. 12. Via exposed by combination of BG, polishing, and dry etching method is shown.

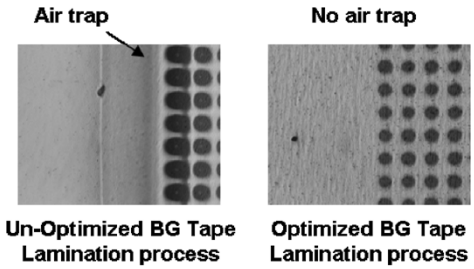


Fig. 13. Bumped wafer laminated with unoptimized and optimized BG tape lamination processes.

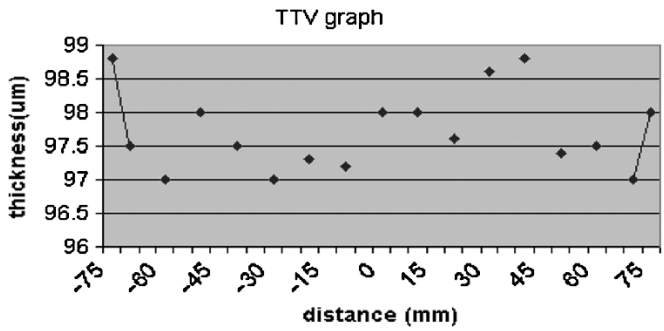


Fig. 14. TTV graph of thinned bumped wafer measured by the "TTV measurement by dicing" method [7].

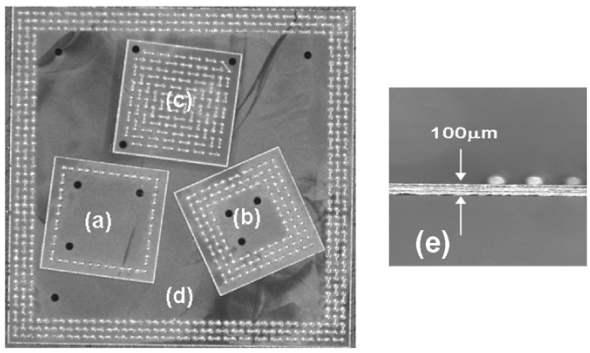


Fig. 15. (a)–(c) Peripheral, depopulated, and full array 3 × 3 mm die. (d) Depopulated 8 × 8 mm die. (e) Ultrathinned test die.

Assembled 3-D stacked modules are subjected to a thermal shock (TS) reliability test. The condition for the TS test is $-55^{\circ}\mathrm{C}/125^{\circ}$ C (JESD22-A106-A, Condition C) for 1000 cycles. Electrical daisy probing is done at an interval of 200 cycles to detect any failures in the modules. During environmental test, no major catastrophic failure is observed and the one failure after 800 cycles has been analyzed for failure. Further detailed reliability studies are ongoing.

V. Integrated Cooling Solutions

Thermal design of the 3-D stacked module is challenging; heat removal from the stacked chips is difficult due to vertical stacking of the heat sources and narrow space between the stacks. Thermal resistance of the intermediate and top chip is high in natural convection cooling due to high heat resistive path to the main heat sink (PCB). Fig. 17 shows a schematic of the test vehicle developed for the research; three layers of stacked module is assembled on a 27 × 27 mm two-layer test vehicle PCB and mounted on a 100 × 100 mm thermal test board. Junction-to-ambient thermal resistance of the three chips was tested in a still air environment and found to be 180 °C/W, 191 °C/W, and 284 °C/W for Chip_B, Chip_M and Chip_T, respectively. Heat dissipation from the module can be marginally increased using forced-air cooling. Three-dimensional stacked module has many advantages over other multichip package formats, but its high thermal resistance is a deterrent factor. A compact and efficient thermal solution is required for its acceptance by the industry. Liquid cooling is a preferred technique for such requirements, and it has high heat transfer coefficient and requires a small cooling space. We have studied two types of liquid-cooled thermal solutions in this research *viz.* 1) single-phase forced liquid cooling and 2) two-phase gravity-driven cooling.

A. Single-Phase Integrated Cooling System

1) Thermal Analysis: Single-phase liquid cooled thermal solution has been optimized using the computational fluid dynamics (CFD) tool Flotherm [9]. Fig. 18 shows the 3-D model of the liquid-cooled thermal solution developed for the research. Plastic housing is designed to encompass the stacked module, and it is represented as solid block in the thermal model. The liquid inlet and outlet port of size 3.2 × 3.2 mm are provided on the top side of the package housing. The inlet and outlet port are connected to a plenum with in the package

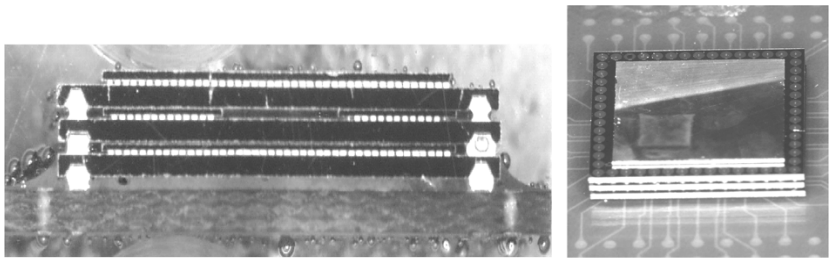


Fig. 16. Cross-sectional view of the 3-D stacked module using silicon carrier with through-hole interconnects.

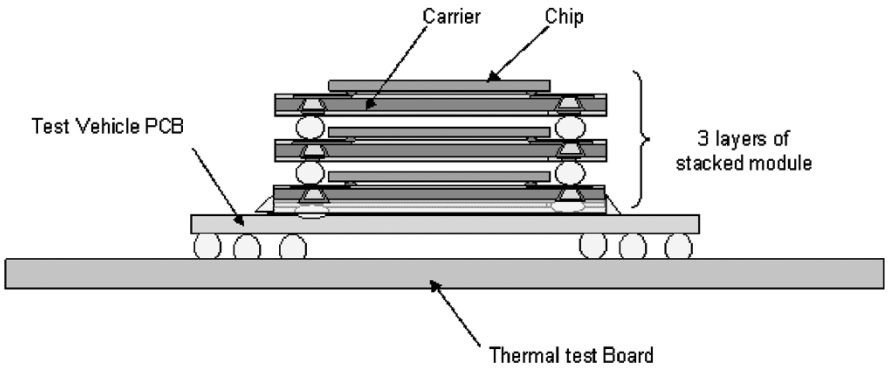


Fig. 17. Schematic of thermal test vehicle.

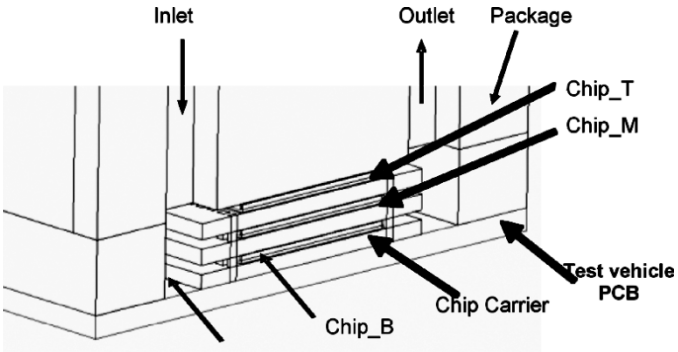


Fig. 18. Three-dimensional CFD model of the thermal test vehicle.

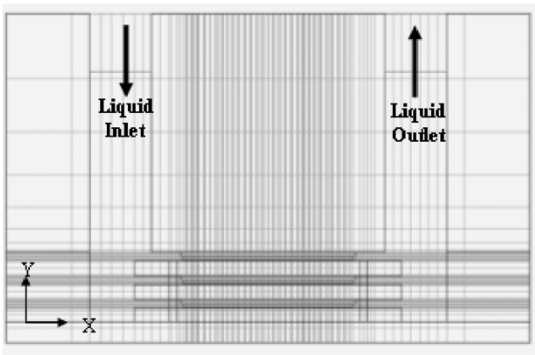


Fig. 19. CFD model showing the computation grids.

housing for flow stabilization. Gaps between the carriers and package housing are critical for the thermal performance. Space between Carrier 1, 2, and 3 is 450 μm and Carrier 3 and housing is 500 μm. Chip thickness of 150 μm with bump height of 50 μm is modeled as per the test vehicle design. The gap between the package housing and carrier edges has to be small for minimum flow bypass and better thermal performance; therefore, the housing is designed with only 25-μm clearance. However, the gap is not considered for the modeling; the carriers are modeled as they are in contact with the package housing. As the test vehicle design is axis symmetry, only a half model is constructed for the analysis. Symmetry boundary condition is applied along the mid XY plane of the model. Ambient condition of 1 atm and inlet liquid temperature of 25 °C is assigned as the initial condition. The heat loss from the package housing external surface to the surrounding air is found to be very small compared to the heat transfer by single-phase liquid cooling; therefore, the thermal analysis is limited to the heat transfer from the stacked module to the liquid with in the package housing. The computational domain size is $27 \times 20 \times 13.5$ mm along the X, Y, and Z directions, respectively. Dielectric liquid FC-72 is chosen as the cooling liquid for the study, and the material properties provided by the supplier is used in the analysis. Fig. 19 shows the computational grid distribution along the XY plane. Sufficient grids are generated to resolve the flow fields between the carrier and the chip; the solution domain has $186 \times 53 \times 120$ structured grids along X, Y, and Z directions, respectively. Table II shows material property assigned for various elements in the model. A uniform heat source of 6 W is applied on each chip, and it is collapsed on the bump side of the chip. A fixed-flow device is modeled at the inlet port, and a constant flow rate of 0.6 L/min is applied. Rise in the chip temperature above the inlet liquid temperature is used for thermal resistance calculations. Thermal resistance of the individual chip has been calculated based on the maximum chip temperature. The chip temperature varied along the flow direction, and the maximum chip temperature is assumed to be at 3/4 of the chip length from the liquid inlet end.

TABLE II
MATERIAL PROPERTIES FOR THERMAL MODELING

Item s	Thermal conductivity (W/mK)
Chip carrier	100
Chip	100
Solder ball and Solder bump	50
Interconnect via in the carrier	50
Test vehicle PCB	In plane : 0.8 Through plane : 0.3
Package housing	0.2
FC-72	0.056
Copper traces in the Test vehicle PCB	Volume averaged thermal conductivity

TABLE III
THERMAL PERFORMANCE OF THE MODULE WITH PLAIN CHIP

	Chip temperature along the flow direction for the heat load of 6 watts on each chip				Estimated maximum power dissipation for 30° C temperature rise (W)
	Chip temperature at $1/4^{th}$ length (° C)	Chip temperature at $1/2^{th}$ length (° C)	Chip temperature at $3/4^{th}$ length (° C)	Thermal resistance based on chip temperature at $3/4^{th}$ length (° C/W)	
Chip-B	42.3	45.6	48.5	3.92	7.7
Chip-M	45.9	50.8	54.0	4.83	6.2
Chip-T	39.8	43.1	45.4	3.4	8.8

Maximum chip power dissipation has been estimated based on the chip temperature rise of 30 °C above the inlet liquid temperature. Simulation results of the chip temperatures at 1/4, 1/2, and 3/4 of the chip length, and thermal resistance and maximum power dissipation from each chip are listed in Table III. The pressure drop across inlet and outlet port is 35 mbar, and maximum liquid velocity is 1.6 m/s along the top carrier.

Thermal limits by the single-phase forced-liquid cooling from the plain chip surface is not meeting our research objective. Therefore, the heat transfer has been enhanced by designing microchannels on the back side of the chip. Design optimization is conducted using the CFD tool; thermal performance of the module with microchannels of width 50, 100, and 150 μm and fin width of 50 μm has been analyzed. The chip thickness for the microchannel design is 375 μm with bump height of 50 μm as shown in Fig. 20. An optimum channel size of 100-μm width has been chosen for the research based on the simulation results. Approximately 300% increase in chip surface area is achieved with 60 fins, as compared to the plain chip surface. A uniform heat source of 20 W is applied on each chip, and it is collapsed on the bump side of the chip. A fixed flow device with constant flow rate of 0.6 L/min is modeled. Rise in the chip temperature above the inlet liquid temperature is used for thermal resistance calculation. The chip temperatures at 1/4, 1/2, and 3/4 of the chip length are extracted from the simulation results. Thermal resistance and maximum power dissipation using microchannel design are listed in

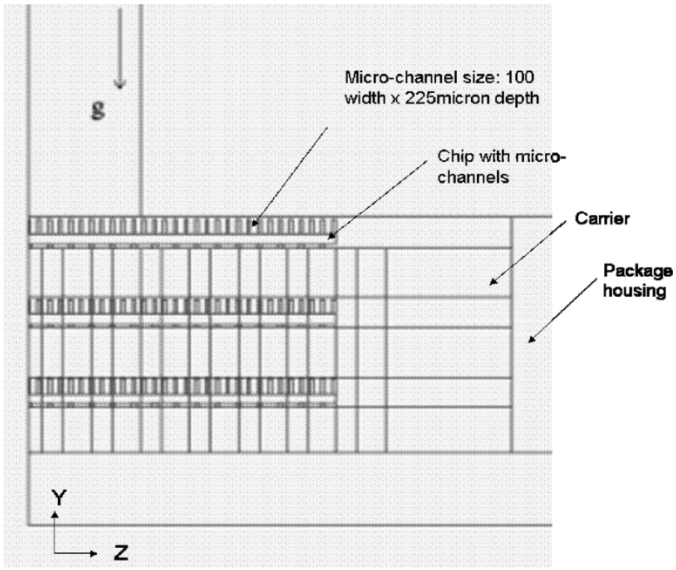


Fig. 20. Stacked module with microchannels for heat transfer enhancement.

TABLE IV
THERMAL PERFORMANCE OF THE MODULE WITH MICROCHANNELS

	Chip temperature along the flow direction for the heat load of 20 watts on each chip				Estimated maximum power dissipation for 30° C temperature rise (W)
	Chip temperature at $1/4^{th}$ length (° C)	Chip temperature at $1/2^{th}$ length (° C)	Chip temperature at $3/4^{th}$ length (° C)	Thermal resistance based on chip temperature at $3/4^{th}$ length (° C/W	
Chip-B	44.1	48.4	52.4	1.37	21.9
Chip-M	44.5	49.9	54.7	1.49	20.1
Chip-T	41.1	45.1	48.7	1.19	25.2

Table IV. The simulation results shows that ~280% increase in heat dissipation from the stacked module with microchannels and the chips thermal limits are meeting the research objective. The pressure drop across the inlet and outlet ports is 54 mbar, and the maximum liquid velocity is 1.6 m/s along the top carrier. Chip temperature variation along the flow direction is small with the microchannels design due to the enhanced heat transfer.

2) Thermal Characterization: A thermal test vehicle with three stacked layers has been fabricated for characterization and model validation. A thermal test chip with microchannels of 100-μm width $\times$ 275-μm depth is designed and fabricated for the research. The chip size is 8.75 $\times$8.75 mm and 0.375-mm thick. The chip consists of polysilicon resistor covering more than 85% of the chip surface area and multiple diodes for temperature sensing. The diodes are placed at 1/4, 1/2, and 3/4 of the chip length. The optimized thermal enhancement structures are micromachined using deep reactive ion etching (DRIE) on back of the chip. A plastic housing with inlet and outlet ports is attached to the 3-D stacked module using structural adhesive. We observed small gap between the chip carrier and the plastic housing due to fabrication and assembly tolerances which could be estimated during the design stage.

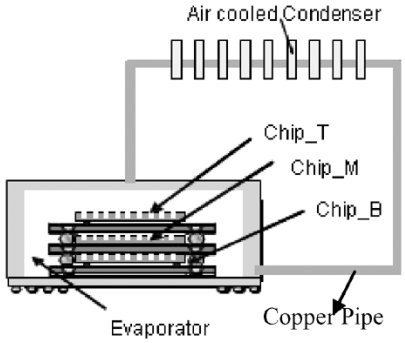


Fig. 21. Two-phase cooling system.

A custom-built test jig is used for thermal characterization. Dielectric fluid FC-72 from 3M is used as cooling liquid, and a constant liquid flow rate of 0.6 L/min is maintained using a minigear pump. The liquid inlet temperature, chip temperatures, and pressure drop across the inlet and outlet are recorded. The measured pressure drop between the inlet and outlet port is 46 mbar as compared to 54 mbar by simulation. The measured pressure drop is lower because of flow bypass through gaps around the carriers and the housing. Thermal resistance of each chip with constant power dissipation has been extracted at 0.6-L/min flow rate. It is difficult to adjust the individual chip power to its maximum limit in a multistack module during the thermal characterization; therefore, one constant heat load has been applied in all the three chips and tested. The chip maximum power dissipation has been extrapolated from the measured chip thermal resistance for 30 °C chip temperatures rise over the inlet liquid temperature. The maximum power dissipation from the Chip_T is 20.0 W and Chip_M is 14.6 W with microchannel design. The measured chip thermal limits are lower than the simulation results, and the difference is mainly because of flow bypass through the gaps due to manufacturing and assembly tolerances. It is difficult to estimate all theses gaps and incorporate in the thermal analysis.

B. Two-Phase Integrated Cooling System

Two-phase cooling capacity is higher due to boiling of the liquid from the chips surface. Also the chip temperature is quite uniform on the entire surface. Fig. 21 shows arrangement of a gravity-driven thermosyphon loop integrated with the 3-D stacked module. A copper housing is attached to the module to function as evaporator of the loop. The evaporator and the condenser are connected by copper tube of 4-mm internal diameter. Condenser length and loop height are estimated using analytical correlations [10], [11]. A gravity head of 50 mm is sufficient to drive the loop to dissipate 25 W of power. Plate-fin air-cooled condenser of 100-mm length and 50-mm size has been used for the experiments. The loop is charged with 20 cc of FC72 under atmospheric pressure and tested. Heat input to the three chips has been adjusted for the chip surface super heat of 25 °C maximum. Amount of heat removed from Chip_B and Chip_M are limited due to insufficient gap for the bubble growth and departure, and it is found to be $\sim$ 1 W from each chip. Heat input to the Chip_T is increased in steps along with constant 1 W of power in Chip_B and Chip_M. The loop is characterized until the Chip_T surface super heat is 25 °C, and maximum heat dissipation from the Chip_T is found to be 20.2 W.

Two types of compact thermal solutions have been designed and characterized in this paper. The thermal limit of the stacked module with single-phase forced liquid cooling is about 65 W and two-phase thermosyphon cooling is about 22 W.

VI. Discussion

A novel method of 3-D packaging using silicon carrier is developed. In this paper, silicon carrier with through hole conductive interconnects is fabricated. The KGDs are either flip-chip attached or wire bonded onto the silcon carriers and then stacked one over the other. Stacked silicon module offers short interconnect paths, heterogeneous integration of different size device (KGD), higher silicon efficiency, reduced real estate area, ease of testability, and miniaturized package format. Major challenges described in the introduction can be solved by this technology. The carrier wafer is functionally tested at the wafer level, thus increasing the assembly yield. In summary, the stacked silicon module described in this paper with enabling technologies such as SVFT and integrated cooling solution has the advantages of a heterogeneous and multifunctional device integrated in a SiP.

VII. Conclusion

This research paper has addressed electrical, thermal, assembly, and process challenges of a novel 3-D stacked SiP using stacked silicon platform technology. Electrical characterization and measurement results prove that the silicon through-hole interconnections are suitable for high-speed applications with very low parasitics. Integrated cooling solutions are meeting the high power requirements from the stacked module. A novel low-cost method to fabricate silicon through-hole vias using solder via fill technology is developed. Preliminary reliability results shows that stack module developed in the research is meeting the Joint Electron Device Engineering Council (JEDEC) thermal shock condition. Further research to implement this 3-D stack technology for hand-held applications is ongoing through a multicompany consortium.

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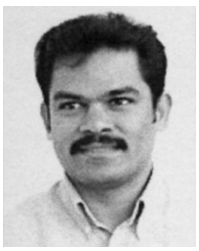
Vaidyanathan Kripesh (M'99) received the M.S. degree in physics from the University of Madras, Madras, India, in 1987.

He carried out his doctoral work at the Max-Planck Institute for Metalforschung, Stuttgart, Germany, in the area of thick- and thin-film passives for microelectronics modules in 1995. He has 16 years research experience in the area of advanced packaging. He worked as a Visiting Scientist at Infineon Technologies, Corporate Research, Munich, Germany, in the area of 3-D integrated circuits. Since March 2000, he has been with the Institute of Microelectronics, Singapore, heading a group of researchers in area of 3-D stacked silicon micromodules and wafer-level packaging processes. He has authored more than 40 journal and conference publications and holds 12 patents to his credit. His research interests are 3-D silicon stacked modules, Cu/low-k packaging and wafer-level packaging. He is also an Adjunct Faculty in the Mechanical Engineering Department, National University of Singapore.

Dr. Kripesh is a Member of IMAPS, and he is currently the President of IMAPS, Singapore Chapter.

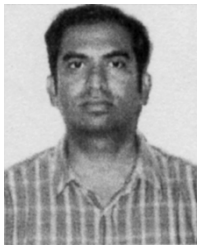
Seung Wook Yoon (M'05) received the Ph.D. degree in materials science and engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Korea, in 1998.

He joined the Hyundai Electronics (Hynix Semiconductor), Ichon, Korea, in 1998 and worked as a Member of Technical Staff at Advanced Electronic Packaging and Module Development. He worked for the development of lead-free solder applications, multichip packaging, CSPs, wafer-level CSP and was involved in JEDEC 11 activity. He joined the Institute of Microelectronics, Singapore, in 2002 and works in the Microsystems, Modules, and Components Laboratory as a Senior Research Engineer. His major interest fields are Cu/low-k/ultralow-k packaging, 3-D silicon micromodule technology, and wafer-level integration and microsystem packaging. He has over 30 conference and journal papers on microelectronic materials and electronic packaging.



V. P. Ganesh (M'04) received the B.Eng. degree in mechanical engineering from Bharathiar University, Coimbatore, India.

He is a Researcher from a materials, process, and assembly background working in the Microsystems Modules and Components Laboratory at the Institute of Microelectronics (IME), Singapore. He has been involved in wafer thinning process development and process integration for 3-D SiPs. Currently, his research focus includes Cu/Low-k device packaging, large-wafer ultrathinning, and development of 3-D SiP based on a silicon platform.



Navas Khan received the B.Eng. degree from Bangalore University, Banglalore, India, in 1993.

He is a Research Engineer at the Institute of Microelectronics, Singapore. His industrial experience has been in the area of system-level thermal design and analysis for communication systems. Currently, he is working on a cooling solution design for system-in-package. His main research focus is heat transfer by boiling and the study of boiling enhancement.

Mihai D. Rotaru (M'01) received the B.S. and M.S. degrees in electrical engineering from the Technical University of Cluj, Cluj, Romania, in 1996 and 1997, respectively, and the Ph.D. degree in electrical engineering from the University of Southampton, Southampton, U.K., in 2000.

From 2000 to 2001, he was with the School of Engineering and Mathematical Science, University of London, London, U.K., where he worked in simulation and modeling of electromagnetic problems. Since May 2001, he has been with Institute of Microelectronics, Singapore, working on design, simulation and analysis of advanced packaging solutions for microelectronics. His professional interest includes efficient modeling techniques for complex electromagnetic problems and lateral and 3-D system-in-package integration RF front end.

Wang Fang received the B.Eng. degree from Tsinghua University, Beijing, China, the M.Eng. degree from Xian Jiaotong University, Xian, China, and the Ph.D. degree from Nanyang Technological University, Singapore.

She is a Senior Research Engineer at the Institute of High Performance Computing, Singapore. Her research interest is in constitutive modeling and finite-element analysis of concrete structures, strength theory, microelectromechanical system (MEMS), electronic packages, and molecular dynamics.

Mahadevan K. Iyer (M'96–SM'03) received the M.S. degree in integrated circuits and systems from the Indian Institute of Technology, Kharagpur, India, and the Ph.D. degree in electronics and electrical communication from the Loughborough University of Technology, Leicestershire, U.K.

He has 12 years of industry research and development experience in the areas of design and development of microcircuits and modules for defense and aerospace applications prior to joining the Institute of Microelectronics (IME), Singapore, in 1996. He is currently the Head of the Microsystems, Modules, and Components Division in IME, where his group focuses on the design and development of RF and optoelectronic packaging and module development in silicon and organic substrate platform technologies. His research interests are in the area of design, modeling, and characterization of RF modules and microsystems. He has authored or coauthored more than 120 research publications and holds eight U.S. patents.

Dr. Iyer has received four Best Paper Awards in international conferences. He has been the Technical Chair and General Chair for many international conferences and workshops in electronic packaging and microsystems