

Three-level inverter configuration cascading two two-level inverters

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Abstract: A power circuit configuration to realise three-level inversion is proposed. Three-level inversion is realised by connecting two two-level inverters in cascade, in the proposed configuration. An isolated DC power supply is used to supply each inverter in this power circuit. Each DC-link voltage is equal to half of the DC-link voltage in a conventional NPC (neutral point clamped) three-level inverter topology. Neutral point fluctuations are absent, and fast recovery neutral clamping diodes are not needed. The proposed inverter scheme produces 64 space-vector combinations distributed over 19 space-vector locations as compared to 27 combinations in a conventional three-level topology. The present power circuit can be operated as a two-level inverter in the range of lower modulation, by clamping one inverter to a zero state and by switching the other inverter. When compared to the H-bridge topology, this circuit needs one power supply less. A space vector based PWM scheme is used for the experimental verification of the proposed topology.

1 Introduction

Three-level inverters have been extensively researched ever since they were introduced by Nabae *et al.* [1]. The advantage of the three-level topology is that multi-level voltage waveforms can be synthesised using devices with lower voltage ratings. The neutral-clamped circuit topology suggested in [1], although simple and elegant, has some disadvantages. The DC-bus capacitors in this circuit configuration carry load currents causing a fluctuating neutral point. The H-bridge topology [2, 3] eliminates this problem, but requires three isolated power supplies and hence is an expensive proposition. A modification of the conventional neutral-clamped inverter has been suggested in [4], in which a capacitor is added across the neutral clamping diodes, to ensure a dynamic balancing of the DC-bus capacitors. However, this method does not eliminate the neutral-point fluctuations completely although it effectively reduces them. Two two-level inverters connected at either end of an open-end winding induction motor drive also achieve three-level inversion [5, 6]. These schemes also require transformer isolation for the elimination of the harmonic currents of the triplen order in the phases. However, to implement these schemes, one needs to open the neutral point of the stator windings.

In this paper, an alternative circuit topology for three-level inversion is proposed. In this circuit configuration, three-level inversion is achieved by connecting two two-level inverters in cascade.

achieved by connecting two two-level inverters in cascade. From Fig. 1, it may be seen that the output phases of inverter-1 are connected to the DC-input points of the corresponding phases in inverter-2. Each inverter is operated with an isolated DC power supply, with a voltage of $V_{dc}/2$ (Fig. 1). The output voltages of inverter-1 (the voltages of the individual phases A_1 , B_1 and C_1 of inverter-1), with respect to the point O , are denoted as v_{A1O} , v_{B1O} and v_{C1O} respectively (Fig. 1). The pole voltages of inverter-2 (the voltages of the individual phases A_2 , B_2 and C_2 of inverter-2, with respect to the point O) are denoted as v_{A2O} , v_{B2O} and v_{C2O} respectively.

The pole voltage of any phase for inverter-2 attains a voltage of $V_{dc}/2$, if

- the top switch of that leg in inverter-2 is turned on,
- the bottom switch of the corresponding leg in inverter-1 is turned on.

Similarly the pole voltage of any phase in inverter-2 attains a voltage of V_{dc} , if

- the top switch of that leg in inverter-2 is turned on and
- the top switch of the corresponding leg in inverter-1 is turned on.

Thus, the DC-input points of individual phases of inverter-2 may be connected to a DC-link voltage of either V_{dc} or $V_{dc}/2$ by turning on the top switch or the bottom switch of the corresponding phase leg in inverter-1.

Additionally, the pole voltage of a given phase in inverter-2 attains a voltage of zero, if the bottom switch of the corresponding leg in inverter-2 is turned on. In this case, the DC-input point of that phase for inverter-2 is floating as the top and bottom switches are switched complementarily in any leg in a two-level inverter. Thus, the pole voltage of a given phase for inverter-2 is capable of

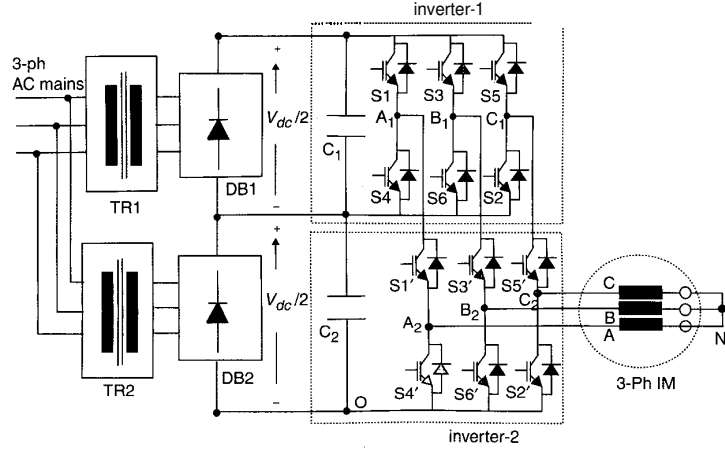


Fig. 1 The power circuit configuration of the proposed three-level inverter

assuming one of the three possible values 0 , $V_{dc}/2$ and V_{dc} , which is the characteristic of a three-level inverter.

Table 1 depicts individual inverter states and the switches turned on to realise those states, for both the inverters.

An example is presented in the following paragraph to determine the resultant space-vector location for a space-vector combination of 5-7' of the two inverters. The combination 5-7 implies that the switching state for inverter-1 is $(-- +)$ and that for inverter-2 is $(+++)$. A '+' indicates that a top switch in an inverter leg is turned on and a '-' indicates that the bottom switch in an inverter leg is turned on. The space-vector V_s constituted by the pole voltages v_{A2O} , v_{B2O} and v_{C2O} is defined as:

$$V_s = v_{A2O} + v_{B2O}e^{j(2\pi/3)} + v_{C2O}e^{j(4\pi/3)} \quad (1)$$

If inverter-1 assumes a state of 5 $(-- +)$ and inverter-2 assumes a state of 7 $(+++)$, from the earlier discussion it follows that:

$$v_{A2O} = V_{dc}/2; v_{B2O} = V_{dc}/2; v_{C2O} = V_{dc} \quad (2)$$

Consequently, the space-vector location for the above set of pole voltages is given by:

$$V_s = (V_{dc}/2) + (V_{dc}/2)e^{j(2\pi/3)} + (V_{dc})e^{j(4\pi/3)} \quad (3)$$

It may be verified that the tip of the space-vector corresponding to the above pole voltages is located at the point E in Fig. 2. The space-vector locations corresponding to the rest of the 63 combinations may similarly be determined. Fig. 2 depicts that these space-vector combina-

tions are distributed over 19 space-vector locations. similar to a conventional three-level inverter. All the space-vector combinations and the space-vector locations are shown in Fig. 2.

From Fig. 2, one may note the redundancy of the space-vector combinations for a given space-vector location. For example, when inverter-2 attains a state of 1' $(+--)$, the points B_2 and C_2 are connected to the point O through the switches $S6'$ and $S2'$. The switches $S3'$ and $S5'$ block the DC-inputs for these two phases as the top and bottom switches in any given leg are switched complementarily in a two-level inverter. It may be noted that the common factor in the states of inverter-1, namely $8(---)$, $3(-+-)$, $4(-++)$ and $5(--+)$, is that in all these states, the point A_1 (DC-input to inverter-2) is connected to the DC-link voltage of $V_{dc}/2$ (Fig. 1, Table 1). Consequently, the combinations 8-1', 3-1', 4-1', 5-1' correspond to the same location A. Additionally, the combination 1-7' also results in the same location.

In this paper, a space-vector modulation scheme is also presented. The switching sequences are devised to ensure a minimum switching frequency. There exist many switching sequences, but to demonstrate the working principle of the proposed topology, only a few combinations have been

Table 1: Inverter states for individual inverters

State of inverter-1	Switches turned on	State of inverter-2	Switches turned on
1 $(+--)$	S6, S'1, S2	1' $(+--)$	S6', S1', S2'
2 $(++-)$	S1, s2, S3	2' $(++-)$	S1', S2', S3'
3 $(-+-)$	s2, s3, s4	3' $(-+-)$	S2', S3', S4'
4 $(-++)$	S3, s4, S5	4' $(-++)$	S3', S4', S5'
5 $(---+)$	S4, S5, S6	5' $(---+)$	S4', S5', S6'
6 $(+-+)$	S5, S6, S1	6' $(+-+)$	S5', S6', S1'
7 $(+++)$	S1, s3, s5	7' $(+++)$	S1', S3', S5'
8 $(---)$	s2, s4, s6	8' $(---)$	S2', S4', S6'

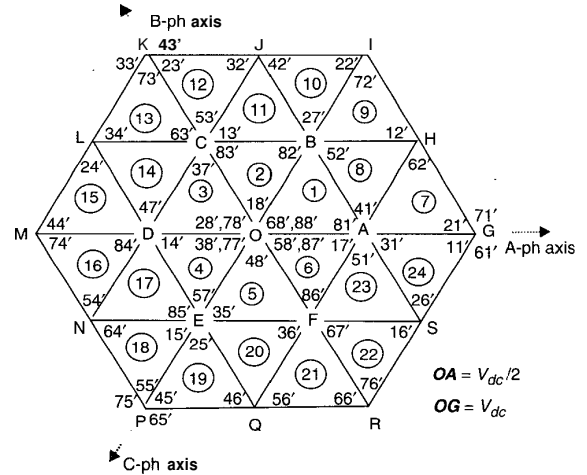


Fig. 2 The space-vector locations and combinations in the proposed circuit topology

employed for a given location. The space-vector combinations used for the implementation of the space-vector modulation in the present work are presented in Fig. 3.

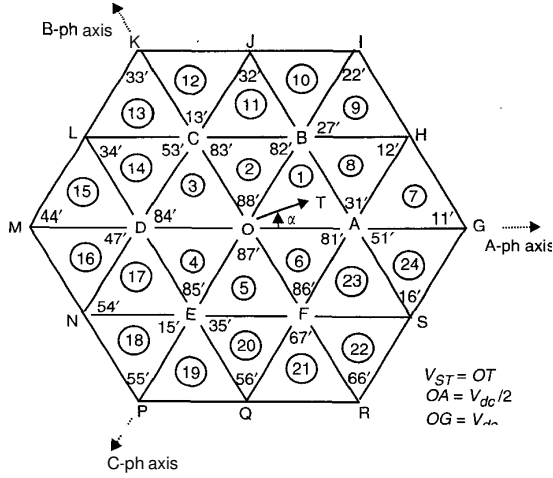


Fig. 3 The space-vector combinations used in the present work

The triplen harmonic currents are absent in this case as the neutral point N of the motor is not connected to the point O. Hence all the triplen harmonic voltages appear across the points O and N (Fig. 1).

One advantage with the proposed topology is that, if the magnitude of the reference voltage space-vector is less than the radius of the maximum circle inscribed in the inner hexagon ($|v_{sr}| < 0.433 V_{dc}$), the tip of the reference voltage space-vector is always situated in the inner hexagon (Fig. 3). In this operating range, inverter-1 is always clamped to the state 8 (---) and inverter-2 alone is switched. Alternatively, inverter-2 can be clamped to the state 7 (+ + +) and inverter-1 could be switched. Consequently, in this operating range the switching losses are due entirely to the switching of one of these inverters and are expected to be lower than in the conventional inverter topology. The proposed power circuit can also be operated with a single DC power supply, with tapped capacitors, as in the case of a conventional neutral clamped inverter. In that case, the inverter cannot be operated as a two-level inverter in the range of lower modulation and a conventional three-level PWM switching scheme is to be employed. This calls for the dynamic balancing of the capacitor voltages by exploiting the redundancy in the space-vector combinations, for a given location, similar to the schemes presented in [7, 8].

It may be noted that the fast recovery clamping diodes are not needed in the proposed circuit when compared to the conventional neutral clamped three-level inverter. However, the bottom bank switches of inverter-2 are to be rated for the full DC-bus voltage of V_{dc} , unlike the case of a conventional neutral clamped three-level inverter, in which all the switches are nominally rated for $V_{dc}/2$ [1, 4]. For example, for the space-vector combination 1-1', the switches S1 and S1' are turned on in the A-phase legs of both the inverters. This makes $v_{A2O} = V_{dc}$. Consequently, the switch S4' must be rated for V_{dc} . The switches in the top bank of inverter-2 need not be rated for the full DC-link voltage of V_{dc} because the top switch of any phase leg of inverter-2 blocks the DC-input voltage to inverter-2,

when the corresponding bottom switch is turned on. Under these conditions, the bottom switches of the corresponding phases of inverter-2 may be turned on so that the top switches of the corresponding phases in inverter-2 need to block only a voltage of $V_{dc}/2$.

Considering the above limitations, it is envisaged that this circuit configuration is suitable for three-level inversion in low-voltage high-power applications (systems such as battery-operated electric vehicle drives) in view of the full DC-link voltage rating for the lower three power devices. One advantage of the proposed system is that the fast recovery neutral point clamping diodes are not needed for the present power circuit. Also, from the engineering point of view, it is easy to assemble such a system, as two existing two-level inverters can be retrofitted to realise this configuration. It should also be noted that the bus-bar design of a two-level inverter is considerably simpler than that of a three-level inverter. The proposed system can work as a conventional two-level inverter in low modulation indices, by clamping the upper inverter. This will reduce the inverter switching losses, when compared to a conventional three-level inverter, and so the overall efficiency of the drive system can be improved.

3 Switching strategy and PWM pattern generation

3.1 Sub-hexagons, sectors and timing definitions

The 64 voltage space-vector locations form the vertices of 24 equilateral triangles, which are referred to as sectors (Fig. 2). The equilateral triangles numbered 1 to 6 are referred to as 'inner sectors'. The equilateral triangles numbered 8, 11, 14, 17, 20 and 23 are referred to as 'middle sectors'. The rest of the sectors (numbered 7, 9, 10, 12, 13, 15, 16, 18, 19, 21, 22 and 24) are referred to as 'outer sectors' (Fig. 3). Six adjacent sectors constitute a sub-hexagon. Six such sub-hexagons can be identified with their centres located at A, B, C, D, E and F respectively (Fig. 3). In addition there is one inner sub-hexagon with its center at O (Fig. 3). The reference voltage space-vector for the space-vector modulation is denoted as v_{sr} and is resolved into two rectangular components v_α and v_β ($v_{sr} = v_\alpha + jv_\beta$), with the a-axis placed along the motor A-phase axis). The angle subtended by v_{sr} with the positive-A axis is denoted as α (Fig. 3). The voltages v_a^* , v_b^* and v_c^* denote the instantaneous reference phase voltages to realise v_{sr} and are obtained by projecting the tip of v_{sr} onto the A, B and C axes respectively (Fig. 4). The relationship between v_α and v_β and v_a^* , v_b^* and v_c^* is given by the transformation:

$$\begin{bmatrix} v_a^* \\ v_b^* \\ v_c^* \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & \sqrt{3}/2 \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} \quad (4)$$

The symbols T_1 and T_2 , respectively, denote the time duration for which the active vectors along the trailing edge and the leading edge of a sector (in which the tip of the reference voltage space-vector is situated) are switched for the realisation of v_{sr} . The symbol T_0 denotes the time duration for which a null vector is switched along with the active vectors to realise v_{sr} . The sampling time period for space-vector modulation is denoted as T_s and is equal to the sum of the time periods T_1 , T_2 and T_0 . The inverter leg switching time periods are those during which the output phases of the inverter are connected to the positive terminal of the DC bus and are denoted as T_{ga} , T_{gb} and T_{gc} respectively for the phases A, B and C. In the conventional

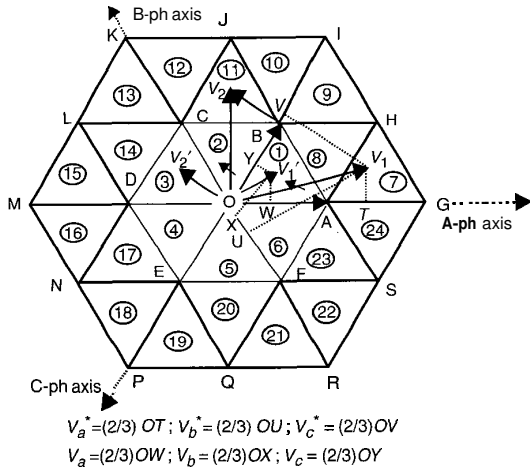


Fig. 4 Mapping of the outer sectors into the inner hexagon

system where a two-level inverter drives an induction motor, there exists an explicit relationship between these timings (T_{ga} , T_{gb} and T_{gc}) and the instantaneous reference phase voltages (v_a^* , v_b^* and v_c^*).

3.2 Sector identification

To implement the PWM pattern, the triangular sector in which the tip of the reference space-vector is situated is first identified and the sub-hexagon to which it belongs is found. The sector identification is based on level comparators along the ja , jb , jc axes perpendicular to the a , b , c axes respectively [6]. The symbols v_{ja}^* , v_{jb}^* and v_{jc}^* denote the projections of v_{sr}^* on to the ja , jb and jc axes respectively. It may be verified that the tip of v_{sr}^* , the reference voltage space-vector, is situated in sector 1 if

$$v_{ja}^* < (\sqrt{3}/4)V_{dc}; v_{jb}^* \geq -(\sqrt{3}/4)V_{dc}; v_{jc}^* < (\sqrt{3}/4)V_{dc} \quad (5)$$

A similar procedure is adopted for the identification of all other sectors [6]. Table 2 summarises the conditions to be satisfied for all the sectors.

The PWM strategy adopted is based on whether the tip of the reference voltage space-vector is situated in the inner sectors (sectors 1 to 6, Fig. 3), in the middle sectors (sectors 8, 11, 14, 17, 20, 23, Fig. 3) or in the outer sectors. In the following sections the PWM strategies adopted for the above three cases are explained. Each cycle of the load phase voltage is divided into 48 equal sub-intervals. Each sub-interval duration corresponds to the sampling interval, T_s . This division is maintained for the entire modulation range with V/f control. The rated frequency of the induction motor corresponds to the maximum value of the magnitude of the reference voltage space-vector on the boundary of modulation. From Fig. 3, this boundary corresponds to the radius of the circle inscribed in the hexagon GTKMPR, and is equal to $0.866V_{dc}$.

3.3 Space-vector based PWM switching strategy for inner sectors

If the tip of the reference voltage space-vector lies in the inner hexagon with centre at O (Fig. 3), a space-vector based scheme as suggested in [9] has been adopted. In this scheme [9], a space-vector based PWM strategy is proposed based on the instantaneous values of the reference voltages of a , b , c phases only. This method does not depend on the magnitude of the reference voltage space-vector and its relative angle with respect to the reference axis (a -axis placed along a phase axis). This space-vector PWM generation scheme is briefly outlined in the Appendix.

This method is extended for the proposed three-level inverter scheme (for PWM pattern generation in inner sectors 1 to 6) by clamping inverter-1 with state 8 (---), while inverter-2 alone is switched. Inverter-2 is switched in such a way that there is only one switching for each sub-interval of that sampling time period. For example, the inverter-2 is switched through the states $8^1-1^1-2^1-7^1$, when $\alpha = 0$. During the next sampling time period, inverter-2 is switched with the reverse sequence, i.e. $7^1-2^1-1^1-8^1$, when $\alpha = 7.5^\circ$. The actual switching time periods for each inverter leg are obtained in the same way as for the single inverter scheme [9]. Table 3 depicts a detailed description of the switching pattern along with the switching sequence. The switching sequence is indicated in brackets, adjacent to the switching pattern. For example the entry $88^1-81^1-82^1-87^1$

Table 2: Sector identification

Sector	v_{ja}^*	v_{jb}^*	v_{jc}^*	Sector	v_{ja}^*	v_{jb}^*	v_{jc}^*
1	$< \frac{\sqrt{3}}{4} V_{dc}$	$\geq -\frac{\sqrt{3}}{4} V_{dc}$	$< \frac{\sqrt{3}}{4} V_{dc}$	2	$< \frac{\sqrt{3}}{4} V_{dc}$	$\geq -\frac{\sqrt{3}}{4} V_{dc}$	$\geq -\frac{\sqrt{3}}{4} V_{dc}$
3	$< \frac{\sqrt{3}}{4} V_{dc}$	$< \frac{\sqrt{3}}{4} V_{dc}$	$\geq -\frac{\sqrt{3}}{4} V_{dc}$	4	$\geq -\frac{\sqrt{3}}{4} V_{dc}$	$< \frac{\sqrt{3}}{4} V_{dc}$	$\geq -\frac{\sqrt{3}}{4} V_{dc}$
5	$\geq -\frac{\sqrt{3}}{4} V_{dc}$	$< \frac{\sqrt{3}}{4} V_{dc}$	$< \frac{\sqrt{3}}{4} V_{dc}$	6	$\geq -\frac{\sqrt{3}}{4} V_{dc}$	$\geq -\frac{\sqrt{3}}{4} V_{dc}$	$< \frac{\sqrt{3}}{4} V_{dc}$
7	$< \frac{\sqrt{3}}{4} V_{dc}$	$< -\frac{\sqrt{3}}{4} V_{dc}$	$\geq \frac{\sqrt{3}}{4} V_{dc}$	8	$< \frac{\sqrt{3}}{4} V_{dc}$	$< -\frac{\sqrt{3}}{4} V_{dc}$	$< -\frac{\sqrt{3}}{4} V_{dc}$
9	$\geq \frac{\sqrt{3}}{4} V_{dc}$	$< -\frac{\sqrt{3}}{4} V_{dc}$	$< \frac{\sqrt{3}}{4} V_{dc}$	10	$\geq \frac{\sqrt{3}}{4} V_{dc}$	$< -\frac{\sqrt{3}}{4} V_{dc}$	$\geq -\frac{\sqrt{3}}{4} V_{dc}$
11	$\geq \frac{\sqrt{3}}{4} V_{dc}$	$\geq -\frac{\sqrt{3}}{4} V_{dc}$	$\geq -\frac{\sqrt{3}}{4} V_{dc}$	12	$\geq \frac{\sqrt{3}}{4} V_{dc}$	$\geq -\frac{\sqrt{3}}{4} V_{dc}$	$< -\frac{\sqrt{3}}{4} V_{dc}$
13	$\geq \frac{\sqrt{3}}{4} V_{dc}$	$< \frac{\sqrt{3}}{4} V_{dc}$	$< -\frac{\sqrt{3}}{4} V_{dc}$	14	$< \frac{\sqrt{3}}{4} V_{dc}$	$< \frac{\sqrt{3}}{4} V_{dc}$	$< -\frac{\sqrt{3}}{4} V_{dc}$
15	$< \frac{\sqrt{3}}{4} V_{dc}$	$\geq \frac{\sqrt{3}}{4} V_{dc}$	$< -\frac{\sqrt{3}}{4} V_{dc}$	16	$\geq -\frac{\sqrt{3}}{4} V_{dc}$	$\geq \frac{\sqrt{3}}{4} V_{dc}$	$< -\frac{\sqrt{3}}{4} V_{dc}$
17	$\geq -\frac{\sqrt{3}}{4} V_{dc}$	$\geq \frac{\sqrt{3}}{4} V_{dc}$	$\geq -\frac{\sqrt{3}}{4} V_{dc}$	18	$< -\frac{\sqrt{3}}{4} V_{dc}$	$\geq \frac{\sqrt{3}}{4} V_{dc}$	$\geq -\frac{\sqrt{3}}{4} V_{dc}$
19	$< -\frac{\sqrt{3}}{4} V_{dc}$	$\geq \frac{\sqrt{3}}{4} V_{dc}$	$< \frac{\sqrt{3}}{4} V_{dc}$	20	$< -\frac{\sqrt{3}}{4} V_{dc}$	$< \frac{\sqrt{3}}{4} V_{dc}$	$< \frac{\sqrt{3}}{4} V_{dc}$
21	$< -\frac{\sqrt{3}}{4} V_{dc}$	$< \frac{\sqrt{3}}{4} V_{dc}$	$\geq \frac{\sqrt{3}}{4} V_{dc}$	22	$< -\frac{\sqrt{3}}{4} V_{dc}$	$\geq -\frac{\sqrt{3}}{4} V_{dc}$	$\geq \frac{\sqrt{3}}{4} V_{dc}$
23	$\geq -\frac{\sqrt{3}}{4} V_{dc}$	$\geq -\frac{\sqrt{3}}{4} V_{dc}$	$\geq \frac{\sqrt{3}}{4} V_{dc}$	24	$\geq -\frac{\sqrt{3}}{4} V_{dc}$	$< -\frac{\sqrt{3}}{4} V_{dc}$	$\geq \frac{\sqrt{3}}{4} V_{dc}$

Table 3: Switching sequences in all sectors

Index	α (deg.)	Possible sectors			Switching sequences		
					Inner sectors	Middle sectors	Outer sectors
					Space-vector combinations (switching sequence) $T_0/2-T_1-T_2-T_0/2$	Space-vector combinations (switching sequence)-sub-hexagonal centre shifted to the origin	Space-vector combinations (switching sequence)-sub-hexagonal centre shifted to the origin
1	0.0	1	-	7	88'-81'-82'-87'	-	81'-11'-12' ($T_0-T_1-T_2$)-A
2	7.5	1	8	7	88'-81'-82'-87'	12'-82'-31' ($T_1-T_2-T_0$)-A	12'-11'-81' ($T_2-T_1-T_0$)-A
3	15.0	1	8	7	88'-81'-82'-87'	31'-82'-12' ($T_0-T_2-T_1$)-A	81'-11'-12' ($T_0-T_1-T_2$)-A
4	22.5	1	8	7	88'-81'-82'-87'	12'-82'-31' ($T_1-T_2-T_0$)-A	12'-11'-81' ($T_2-T_1-T_0$)-A
5	30.0	1	8	7	88'-81'-82'-87'	31'-82'-12' ($T_1-T_0-T_2$)-B	81'-11'-12' ($T_0-T_1-T_2$)-A
6	37.5	1	8	9	88'-81'-82'-87'	12'-82'-31' ($T_2-T_0-T_1$)-B	12'-22'-27' ($T_1-T_2-T_0$)-B
7	45.0	1	8	9	88'-81'-82'-87'	31'-82'-12' ($T_1-T_0-T_2$)-B	27'-22'-12' ($T_0-T_2-T_1$)-B
8	52.5	1	8	9	88'-81'-82'-87'	12'-82'-31' ($T_2-T_0-T_1$)-B	12'-22'-27' ($T_1-T_2-T_0$)-B
9	60.0	2	-	10	88'-83'-82'-87'	-	27'-22'-32' ($T_0-T_1-T_2$)-B
10	67.5	2	11	10	88'-83'-82'-87'	32'-82'-13' ($T_1-T_0-T_2$)-B	32'-22'-27' ($T_2-T_1-T_0$)-B
11	75.0	2	11	10	88'-83'-82'-87'	13'-82'-32' ($T_2-T_0-T_1$)-B	27'-22'-32' ($T_0-T_1-T_2$)-B
12	82.5	2	11	10	88'-83'-82'-87'	32'-82'-13' ($T_1-T_0-T_2$)-B	32'-22'-27' ($T_2-T_1-T_0$)-B
13	90.0	2	11	10	88'-83'-82'-87'	13'-82'-32' ($T_0-T_1-T_2$)-C	27'-22'-32' ($T_0-T_1-T_2$)-B
14	97.5	2	11	12	88'-83'-82'-87'	32'-82'-13' ($T_2-T_1-T_0$)-C	32'-33'-83' ($T_1-T_2-T_0$)-C
15	105.0	2	11	12	88'-83'-82'-87'	13'-82'-32' ($T_0-T_1-T_2$)-C	83'-33'-32' ($T_0-T_2-T_1$)-C
16	112.5	2	11	12	88'-83'-82'-87'	32'-82'-13' ($T_2-T_1-T_0$)-C	32'-33'-83' ($T_1-T_2-T_0$)-C
17	120.0	3	-	13	88'-83'-84'-87'	-	83'-33'-34' ($T_0-T_1-T_2$)-C
18	127.5	3	14	13	88'-83'-84'-87'	34'-84'-53' ($T_1-T_2-T_0$)-C	34'-33'-83' ($T_2-T_1-T_0$)-C
19	135.0	3	14	13	88'-83'-84'-87'	53'-84'-34' ($T_0-T_2-T_1$)-C	83'-33'-34' ($T_0-T_1-T_2$)-C
20	142.5	3	14	13	88'-83'-84'-87'	34'-84'-53' ($T_1-T_2-T_0$)-C	34'-33'-83' ($T_2-T_1-T_0$)-C
21	150.0	3	14	13	88'-83'-84'-87'	53'-84'-34' ($T_1-T_0-T_2$)-D	83'-33'-34' ($T_0-T_1-T_2$)-C
22	157.5	3	14	15	88'-83'-84'-87'	34'-84'-53' ($T_2-T_0-T_1$)-D	34'-44'-47' ($T_1-T_2-T_0$)-D
23	165.0	3	14	15	88'-83'-84'-87'	53'-84'-34' ($T_1-T_0-T_2$)-D	47'-44'-34' ($T_0-T_2-T_1$)-D
24	172.5	3	14	15	88'-83'-84'-87'	34'-84'-53' ($T_2-T_0-T_1$)-D	34'-44'-47' ($T_1-T_2-T_0$)-D
25	180.0	4	-	16	88'-85'-84'-87'	-	47'-44'-54' ($T_0-T_1-T_2$)-D

means that the combination 88' is output for a duration of $T_0/2$, the combinations 81' and 82' are output for durations of T_1 and T_2 respectively, and 87' is output for a duration of $T_0/2$.

3.4 Mapping the middle sectors and the outer sectors into the inner hexagon

In Fig. 4, the reference voltage vectors OV_1 and OV_2 at two different time instants are shown with their tips situated in sector 7 and sector 11, respectively. In sector 7 the vector OV_1 can be conceived to be the vector sum of two components OA and AV_1 . The vector OA can readily be obtained from the appropriate space-vector combinations from the individual inverters (Fig. 3). The vector AV_1 is not directly available from the space-vector combinations (Fig. 3) and hence is to be generated from the adjacent active switching vector locations (A, G and H) using volt-second balance. The periods T_0 , T_1 and T_2 for vector AV_1 in sector 7, in a sampling time period T_s , can be determined by mapping the vector AV_1 to OV_1' by shifting the point A to O. By shifting the point A to O, the outer triangle AGH is mapped to an inner sector OAB (Fig. 4). It may be seen that the original reference vector OV_1 can be realised by using the same timings employed to realise OV_1' . To realise OV_1 , the space-vectors located at A, G and H are switched

instead of the ones located at O, A and B. It is evident that this procedure is conceptually equivalent to producing OV_1' and giving a vectored offset equal to OA to produce OV_1 .

Similarly, sector 11 can be mapped to the inner sector 3 by shifting the point B to O. In this case, the vector BV_2 gets mapped to OV_2' . Adopting this procedure, all outer sectors (7 to 24) may be mapped into the corresponding inner sectors. The generalised equations of transformation for the modified reference phase voltages when the sub-hexagonal centres A to F are shifted to O are given by:

$$\begin{aligned} v_a &= v_a^* - (V_{dc}/3) \cos[(m-1).\pi/3] \\ v_b &= v_b^* + (V_{dc}/3) \cos[m.\pi/3] \\ v_c &= v_c^* + (V_{dc}/3) \cos[(m-2).\pi/3] \end{aligned} \quad (6)$$

In (6), v_a^* , v_b^* and v_c^* are the sampled phase values corresponding to the actual reference voltage space-vector v_{sr} (Fig. 4). The voltages v_a , v_b and v_c correspond to the transformed reference voltage space-vector OV_1' (Fig. 4). In (6), m is an integer variable that takes values 1 to 6 corresponding to points A to F respectively (Fig. 3). The transformed reference phase voltages v_a , v_b and v_c are used to determine the inverter leg switching timings— T_{ga} , T_{gb} and T_{gc} , by using the PWM generation scheme outlined in Section 3.3 and the Appendix. The timing periods T_0 , T_1

and T_2 to switch the space-vector combinations at the nearest vertices are then determined from the inverter leg switching timings T_{ga} , T_{gb} and T_{gc} , as described in the following Sections for the middle sectors and the outer sectors.

3.5 Space-vector based PWM switching strategy for middle sectors

By shifting the centres of the sub-hexagons A to F to the point O using an appropriate coordinate transformation, the middle sectors (sectors numbered 8, 11, 14, 17, 20 and 23) are mapped to a corresponding inner sector (1 to 6). Once the mapped inner sector is identified, the switching periods for individual legs (T_{ga} , T_{gb} and T_{gc}) for both the inverters may be obtained using the procedure outlined in [9]. There exists an explicit relationship between the inverter leg switching timings (T_{ga} , T_{gb} and T_{gc}) and the space-vector switching timings (T_0 , T_1 and T_2) depending upon the sector of the inner hexagon in which the tip of the transformed reference space-vector OV_2' is situated. Using these relationships the space-vector switching timings T_0 , T_1 and T_2 can be determined from the inverter leg switching timings T_{ga} , T_{gb} and T_{gc} . For example, if the tip of OV_2' is situated in sector 8, the sub-hexagonal centre A is shifted to O if $0^\circ < \alpha < 30^\circ$ mapping sector 8 to sector 2 in the inner hexagon. If $30^\circ \leq \alpha < 60^\circ$, to ensure that the nearest sub-hexagonal centre is shifted to O, the sub-hexagonal centre B is shifted to O mapping sector 8 to sector 6 in the inner hexagon.

It may easily be verified that:

$$\begin{aligned} T_0 &= 2T_{gc}; T_1 = T_{ga} - T_{gc}; \\ T_2 &= T_{gb} - T_{ga} \text{ when sector 8 is mapped to sector 2} \end{aligned} \quad (7)$$

and

$$\begin{aligned} T_0 &= 2T_{gb}; T_1 = T_{gc} - T_{gb}; \\ T_2 &= T_{ga} - T_{gc} \text{ when sector 8 is mapped to sector 6} \end{aligned} \quad (8)$$

A similar procedure is adopted when the tip of OV_2' is situated in the sectors 11, 14, 17, 20 and 23. Table 4 summarises the relationships amongst T_1 , T_2 and T_0 and T_{ga} , T_{gb} and T_{gc} for all of the middle sectors. The space-vector combinations, the switching sequence and the sub-hexagonal centres transformed for each sampling time period for the outer sectors are depicted in Table 3. It may be observed that T_0 , the time duration for which a

null vector is output, is not split into equal halves in this case.

3.6 Space-vector based PWM switching strategy for outer sectors

The procedure outlined for the middle sectors may be extended to the outer sectors. It may be noted that the orthogonal axes $-jA$, jB and jC do not pass through the midst of the outer sectors, unlike the middle sectors (Fig. 3). Consequently, the sub-hexagonal centre to be shifted to the point O to map a given outer sector into a corresponding inner sector is always the same, unlike the case for a middle sector (Table 4). The relationships amongst the inverter leg switching timings (T_{ga} , T_{gb} and T_{gc}) and the space-vector switching timings (T_0 , T_1 and T_2) may be obtained from Table 4. The space-vector combinations, the switching sequence and the sub-hexagonal centres transformed for each sampling time period for the outer sectors are depicted in Table 3. In this case also, the time duration T_0 is not split into equal halves.

3.7 Over-modulation

When the reference vector is located outside the hexagon GIKMPR (Fig. 4), a modified reference voltage vector on the periphery of the hexagon having the same angle as the original reference vector is chosen [4]. The modified active vector switching times T_1' and T_2' during over-modulation with the modified reference voltage vector may be calculated simply by the following conditions:

$$T_1' + T_2' = T_s \text{ and } T_1' : T_2' = T_1 : T_2 \quad (9)$$

Therefore

$$\begin{aligned} T_1' &= \frac{T_1}{(T_1 + T_2)} T_s \\ T_2' &= \frac{T_2}{(T_1 + T_2)} T_s \end{aligned} \quad (10)$$

4 Experimental results and discussion

The proposed scheme is implemented for a 1 HP, three-phase induction motor drive in open loop with V/f control for different reference voltages covering the entire speed range. The gating signals for the proposed inverter drive

Table 4: Switching time calculation

Range of α	Sector before transformation	Sub-hexagonal centre shifted to the point O	Sector after transformation	$T_0/2$	T_1	T_2
$0^\circ \leq \alpha < 30^\circ$	7	A	2	T_{gc}	$T_{ga} - T_{gc}$	$T_{gb} - T_{ga}$
$30^\circ \leq \alpha < 60^\circ$	7	B	6	T_{gb}	$T_{gc} - T_{gb}$	$T_{ga} - T_{gc}$
$60^\circ \leq \alpha < 90^\circ$	8	B	3	T_{ga}	$T_{gb} - T_{gc}$	$T_{gc} - T_{ga}$
$90^\circ \leq \alpha < 120^\circ$	8	C	1	T_{gc}	$T_{ga} - T_{gb}$	$T_{gb} - T_{gc}$
$120^\circ \leq \alpha < 150^\circ$	9	C	4	T_{ga}	$T_{gb} - T_{ga}$	$T_{gc} - T_{gb}$
$150^\circ \leq \alpha < 180^\circ$	9	D	2	T_{gc}	$T_{ga} - T_{gc}$	$T_{gb} - T_{ga}$
$180^\circ \leq \alpha < 210^\circ$	10	D	5	T_{gb}	$T_{gc} - T_{ga}$	$T_{ga} - T_{gb}$
$210^\circ \leq \alpha < 240^\circ$	10	E	3	T_{ga}	$T_{gb} - T_{gc}$	$T_{gc} - T_{ga}$
$240^\circ \leq \alpha < 270^\circ$	11	E	6	T_{gb}	$T_{gc} - T_{gb}$	$T_{ga} - T_{gc}$
$270^\circ \leq \alpha < 300^\circ$	11	F	4	T_{ga}	$T_{gb} - T_{ga}$	$T_{gc} - T_{gb}$
$300^\circ \leq \alpha < 330^\circ$	12	F	1	T_{gc}	$T_{ga} - T_{gb}$	$T_{gb} - T_{gc}$
$330^\circ \leq \alpha < 360^\circ$	12	A	5	T_{gb}	$T_{gc} - T_{ga}$	$T_{ga} - T_{gb}$

have been generated using a TMS 320F240 DS processor. A DC-link voltage of 300V is used for experimentation ($V_{dc}=300\text{V}$).

The experimental results for $|v_{sr}|=0.4V_{dc}$ are presented in Fig. 5. In this case, the tip of the reference voltage space-vector v_{sr} is confined to the inner sectors i.e. sectors 1 to 6 (Fig. 3).

The experimentally obtained waveforms of v_{A1O} and the pole voltage v_{A2O} for the -A phase legs are presented in Fig. 5a (top and bottom traces respectively). As mentioned earlier, inverter-2 alone is switched in this case, while inverter-1 is clamped to a state of 8(---). Thus the inverter system behaves in a similar way to a conventional two-level inverter with a DC-link voltage of $V_{dc}/2$. The top trace of Fig. 5a showing that $v_{A1O}=150\text{V}$ ($V_{dc}/2$) confirms this fact. Fig. 5b shows the waveform of v_{A2N} (motor phase voltage) obtained experimentally. As one might expect, it is a familiar six-step waveform of a two-level inverter. The motor phase current in this operating condition is shown in Fig. 5c. Fig. 5d illustrates the normalised harmonic spectra of the voltages v_{A2O} and v_{A2N} (top and bottom traces respectively). It may be noted that the triplen harmonic components are present in

the spectrum of v_{A1O} , and are absent in that of v_{A2O} . All these components are dropped across the points O and N (Fig. 1), as explained in Section 2.

The experimental results obtained when $|v_{sr}|=0.6V_{dc}$ are presented in Fig. 6. In this case, the tip of the reference voltage space-vector is situated either in the middle sectors (8, 11, 14, 17, 20 and 23) or in the outer sectors (Fig. 3). Fig. 6a shows the experimentally obtained waveforms of v_{A1O} and the pole voltage v_{A2O} (top and bottom traces respectively). In this case, both the inverters are switched. Consequently, the DC-input for the phase-A leg of inverter-2 (v_{A1O}) is switched amongst the voltages $V_{dc}/2$ (150 V) and V_{dc} (300 V), as is evident from Fig. 6a (top trace). The bottom trace of Fig. 6a shows the pole voltage v_{A2O} in which all three levels, -0 , $V_{dc}/2$ (150 V) and V_{dc} (300 V), are present, as expected from this topology. Fig. 6b illustrates the experimentally obtained waveform of the voltage $-v_{A2N}$ (motor phase voltage). Fig. 6c shows the motor phase current in this operating condition. Fig. 6d shows the normalised harmonic spectra of voltages v_{A2O} and v_{A2N} (top and bottom traces respectively).

Figs. 7 and 8 show the experimental results when $|v_{sr}|=V_{dc}$ and corresponds to the case of over-modulation

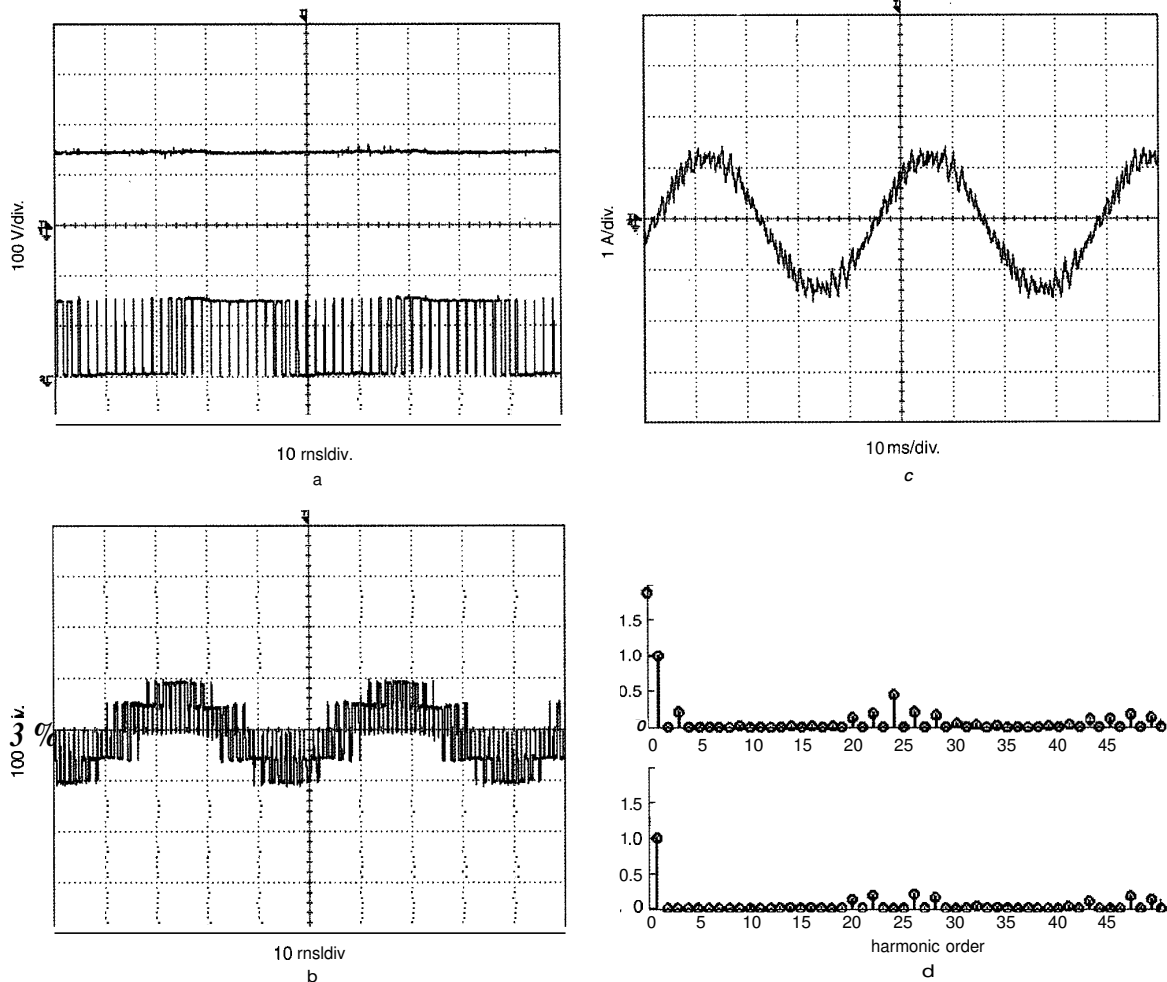


Fig. 5

a The experimental waveforms of pole voltages v_{A1O} (top) and v_{A2O} (bottom) for $|v_{sr}|=0.4V_{dc}$

b The experimental waveform of motor phase-voltage v_{A2N} for $|v_{sr}|=0.4V_{dc}$

c The motor phase current at no-load for $|v_{sr}|=0.4V_{dc}$

d The normalised harmonic spectra of v_{A2O} (top) and v_{A2N} (bottom) for $|v_{sr}|=0.4V_{dc}$

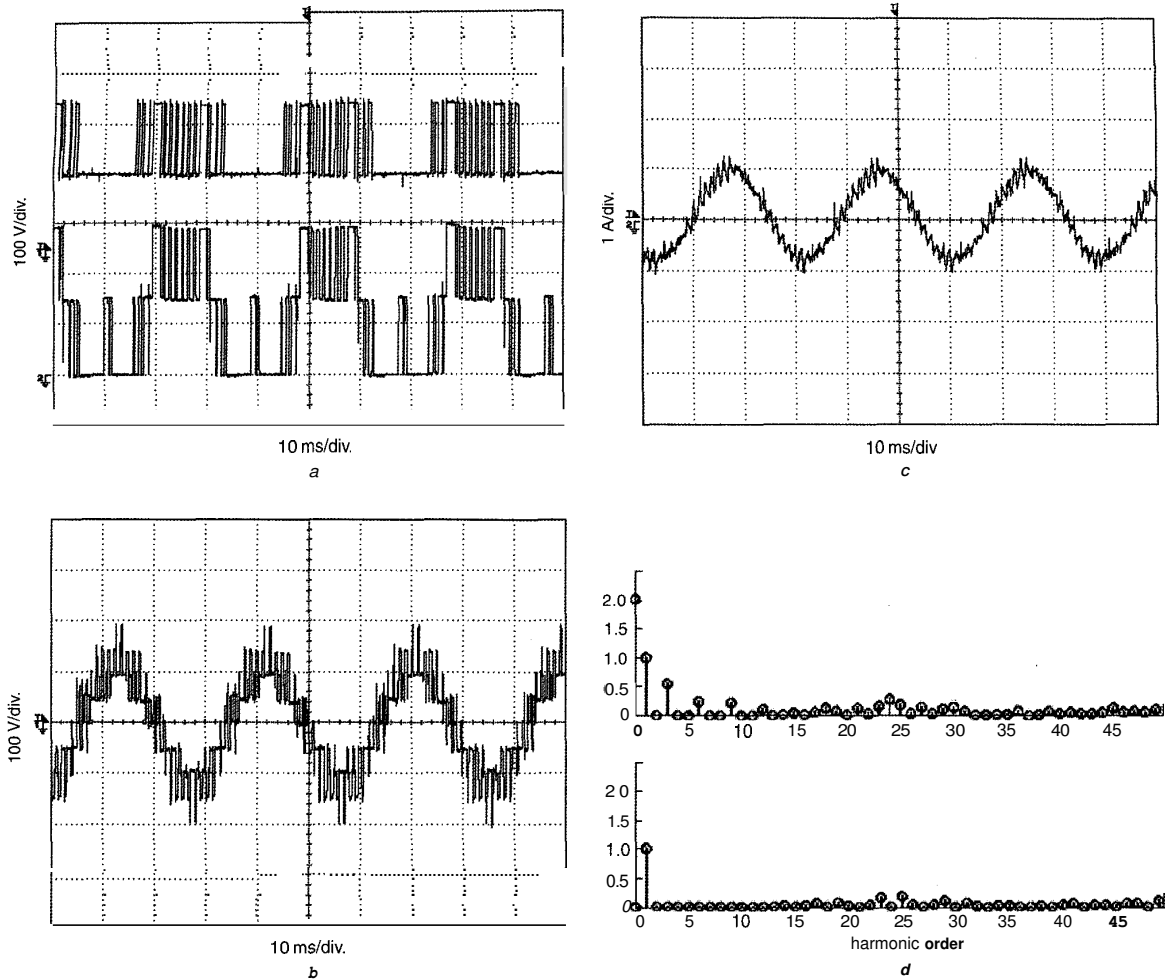


Fig. 6

- a The experimental waveforms of pole voltages v_{A1O} (top) and v_{A2O} (bottom) for $|V_{sr}| = 0.6 V_{dc}$
 b The experimental waveform of motor phase-voltage v_{A2N} for $|V_{sr}| = 0.6 V_{dc}$
 c The motor phase current at no-load for $|V_{sr}| = 0.6 V_{dc}$
 d The normalised harmonic spectra of v_{A2O} (top) and v_{A2N} (bottom) for $|V_{sr}| = 0.6 V_{dc}$

as $|v_{sr}| > 0.866 V_{dc}$ (Fig. 3). In this case, the tip of the reference voltage space-vector is forced to trace the hexagon GIKMPR (Fig. 3) as explained in Section 3.7. The experimental waveforms of the voltage v_{A1O} and the pole voltage v_{A2O} are presented in Fig. 7a (top and bottom traces respectively). The experimental waveform of v_{A2N} (motor phase voltage) is presented in Fig. 7b. Fig. 7c shows the motor phase current in this operating condition. The normalised harmonic spectra of the voltages v_{A2O} and v_{A2N} (the motor phase voltage) are presented in Fig. 8 (top and bottom traces respectively).

Thus the three-level inverter proposed in this paper has been tested for the entire speed range using the V/f control.

5 Conclusions

In the proposed scheme, two two-level inverters connected in cascade achieve three-level inversion. 64 voltage space-vector combinations are possible compared to the 27 combinations obtained in the conventional three-level inverter. As isolated DC power supplies are used to feed

individual inverters, the DC-link capacitors carry only the ripple currents and not the load current. Thus, the voltage fluctuations of the neutral point are avoided. Two existing two-level inverters are retrofitted to realise three-level inversion. The neutral clamping diodes are not needed in this topology, when compared to a conventional NPC three-level inverter.

With two isolated DC link supplies, in the lower range of modulation (when $|v_{sr}| < 0.433 V_{dc}$), one of the inverters can be clamped to a zero inverter vector state and the other inverter can be switched as a two-level inverter reducing the switching losses, when compared to a conventional three-level inverter. The proposed power circuit can also be used with a single DC link with tapped capacitors. In that case, the problem of neutral point balancing is to be addressed as in the case of a conventional three-level inverter, using the redundancy of the space vector combinations for a given location.

This configuration needs two isolated power supplies when compared to an H-bridge topology, which needs three isolated DC links. Three switches in the proposed scheme are to be rated to block the entire DC-bus voltage.

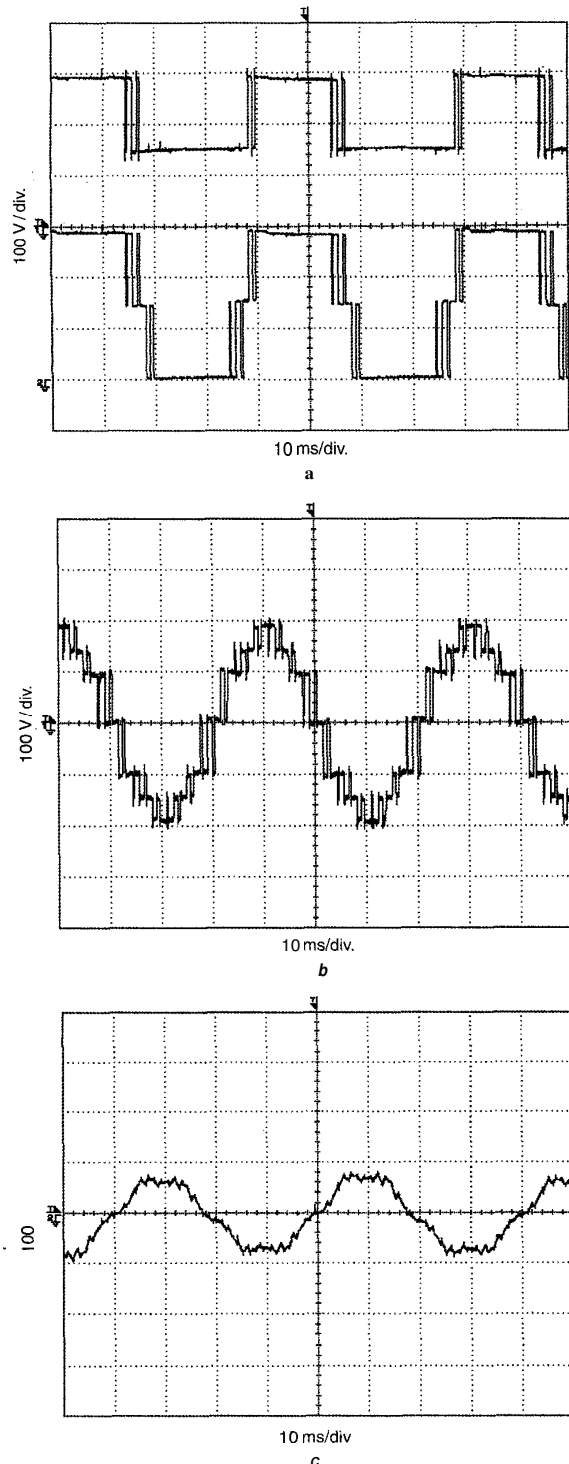


Fig. 7

- a The experimental waveforms of pole voltages v_{A1O} (top) and v_{A2O} (bottom) for $|V_{sr}| = V_{dc}$ (over-modulation)
 b The experimental waveform of motor phase-voltage v_{A2N} for $|V_{sr}| = V_{dc}$ (over-modulation)
 c The motor phase current at no-load for $|V_{sr}| = V_{dc}$ (over-modulation)

The switching patterns are so devised that in each inverter only one leg is switched during a sub-interval of the sampling period T_s .

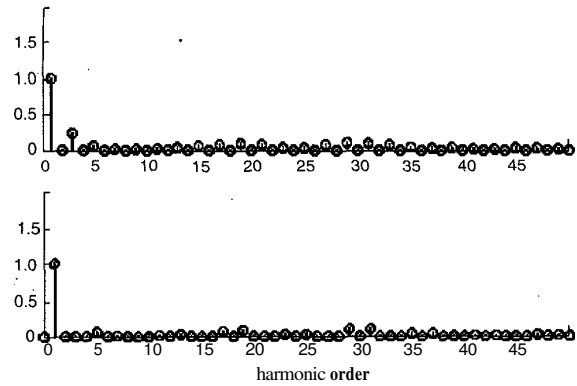


Fig. 8 The normalised harmonic spectra of v_{A2O} (top) and v_{A2N} (bottom) for $|V_{sr}| = V_{dc}$ (over-modulation)

6 References

- 1 NABAE, A., TAKAHASHI, I., and AGAKI, H.: 'A new neutral-point-clamped PWM inverter', *IEEE Trans Ind. Appl.*, 1981, **17**, pp. 518-523
- 2 MANJREKAR, M.D., and LIPO, T.A.: 'A Hybrid Multilevel Inverter Topology for Drive Applications'. Proceedings of 13th Annual Applied electronics Conference (APEC), California, 15-19 February 1998, pp. 523-529
- 3 RUFER, A., VEENSTRA, M., and GOPAKUMAR, K.: 'Asymmetric multilevel converter for high resolution voltage phasor generation'. Proceedings of 8th European Conference on Power electronics and applications (EPE), Lausanne, 13-16 September 1999, pp. P1-P10
- 4 SUH, B.-S., and HYUN, D.-S.: 'A New N-level High Voltage Inversion System', *IEEE Trans. Ind. Electron.*, 1997, **44**, (1), pp. 107-115
- 5 STEMMLER, H., and GUGGENBACH, P.: 'Configurations of high power voltage source inverter drives'. Proceedings of 5th European Conference on Power electronics and applications (EPE), Brighton, UK, 1993, pp. 7-12
- 6 SHIVAKUMAR, E.G., GOPAKUMAR, K., and RANGANATHAN, V.T.: 'Space vector PWM control of dual inverter fed open-end winding induction motor drive'. Proceedings of 16th Annual Applied electronics Conference (APEC), California, 4-8 March 2001, pp. 394-404
- 7 LEE, Y.-H., SUH, B.-S., and HYUN, D.-S.: 'A novel PWM scheme for a three level voltage source inverter with GTO thyristors', *IEEE Trans. Ind. Appl.*, 1996, **32**, (2)
- 8 VON JOUANNE, A., DAI, S., and ZHANG, H.: 'A simple method for balancing the DC link voltage of three level inverters'. Proceedings of 32nd Annual Power electronics Specialists Conference (PESC), Vancouver, Canada, 17-21 June 2001, pp. 1341-1345
- 9 KIM, J.-S., and SUL, S.-K.: 'A Novel Voltage Modulation Technique of the Space Vector PWM'. International Power Engineering Conference, IPEC, Yokohama, 3-7 April 1995, pp. 742-747

7 Appendix

In sector 1, the switching periods for the active vectors T_1 and T_2 may be expressed in terms of the instantaneous values of the reference phase voltages v_a^* , v_b^* and v_c^* as [9]:

$$T_1 = \frac{T_s(v_a^* - v_b^*)}{V_{dc}}; T_2 = \frac{T_s(v_b^* - v_c^*)}{V_{dc}} \quad (11)$$

From (11), the switching time periods proportional to the instantaneous values of the reference phase voltages, termed imaginary switching times, are defined as [9]:

$$T_{as} \equiv \left(\frac{T_s}{V_{dc}}\right)v_a^*; T_{bs} \equiv \left(\frac{T_s}{V_{dc}}\right)v_b^*; T_{cs} \equiv \left(\frac{T_s}{V_{dc}}\right)v_c^* \quad (12)$$

From (11) and (12) the active vector switching times T_1 and T_2 in sector 1 may be expressed as:

$$T_1 = T_{as} - T_{bs}; T_2 = T_{bs} - T_{cs} \quad (13)$$

Extending this procedure for the other sectors, the active vector switching times T_1 and T_2 for the respective sectors

may be expressed in terms of the imaginary switching times T_a , T_{bs} and T_{cs} for a particular sampling interval.

The effective time T_{eff} is the time during which the active vectors are switched in a sector and is given by $(T_1 + T_2)$. This may be determined as the difference between the maximum and minimum values among T_a , T_{bs} and T_{cs} . The time duration T_0 , the time for which a zero vector is applied, may be obtained from T_1 and T_2 as:

$$T_0 = T_s - T_{eff} \quad (14)$$

where

$$\begin{aligned} T_{eff} &= \max\{T_a, T_{bs}, T_{cs}\} - \min\{T_a, T_{bs}, T_{cs}\} \\ &= T_{max} - T_{min} \end{aligned} \quad (15)$$

The offset time T_{offset} required to distribute the zero voltage symmetrically during one sampling period is given by [9]:

$$T_{offset} = \frac{T_0}{2} - T_{min} \quad (16)$$

The actual switching times for each inverter leg T_{ga} , T_{gb} and T_{gc} can be obtained by the time shifting operation as follows:

$$\begin{aligned} T_{ga} &= T_a + T_{offset}; \quad T_{gb} = T_{bs} + T_{offset}; \\ T_{gc} &= T_{cs} + T_{offset} \end{aligned} \quad (17)$$