Three-level inverter configuration with common-mode voltage elimination for induction motor drive

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Abstract: A scheme for a three-level voltage space phasor generation with common-mode voltage elimination is proposed. An open-end-winding induction motor, fed from both ends by two three-level inverters, which are realised by a cascading two two-level inverter, is used in this configuration. The voltage space vectors of individual three-level inverters, which generate the same common-mode voltage in the inverter pole voltage, are variously grouped. When these voltage space vectors are used to switch individual three-level inverters, it results in zero common-mode voltage across the motor windings. In the proposed scheme, voltage space phasors from individual inverters with zero common-mode voltage in the inverter pole voltage are used for PWM control. For the proposed drive configuration, the DC link voltage requirement is only half when compared to the DC link voltage of a conventional neutral-point-clamped (NPC) three-level inverter. The proposed inverter configuration offers reduced circuit and control complexity when compared to similar schemes with NPC or H-bridge inverter configurations.

1 Introduction

Multilevel inverters using pulse-width modulation are being increasingly preferred for high-power applications [1, 2]. The advantages of multilevel inverters are their ability to generate voltage waveforms with lower harmonics, without resorting to high-frequency PWM switching. The switching loss is drastically reduced, as the devices are switched at lower voltages.

The common-mode voltage generates leakage currents, due to the electrostatic couplings, between stator winding and stator iron frame, and between stator winding and rotor iron [3, 4]. The leakage current flowing to the rotor builds up the motor shaft voltage. The shaft voltages then exceed the breakdown strength of the lubrication oil film, leading to flashover between the bearing races. The frequent flashovers may damage the bearing because of the electro-discharge machining (EDM) effect [4].

Special mechanical modifications have been suggested for reducing the bearing currents and the conducted EMI [5]. These include use of insulated bearing at the non-drive end side, reduction of coupling from stator to rotor with electrostatic shields and grounding of the shaft with the grounding brushes. These techniques call for increased maintenance and costs. Finally, attention has been focused on the real source of the problem, i.e. the common-mode voltages generated by the PWM inverter [5]. A number of techniques have been suggested to reduce or eliminate the common-mode voltages, generated by the various configurations of multilevel inverters [5–7]. A modulation scheme, for eliminating the common-mode voltage in the conventional neutral-point-clamped (NPC) three-level inverter, is presented in [6]. The conventional NPC configuration has its own problems, such as neutral-point fluctuations, power-circuit complexity etc. Additional hardware, required to control the neutral-point fluctuations present with the NPC inverter configuration, is described in [7].

An open-end winding induction motor fed from both ends with two-level inverter results in output phase voltage structure, similar to a conventional three-level NPC inverter configuration [2, 8]. Such a configuration is free from neutral-point fluctuations and offers a multiplicity of vector combinations of individual two-level inverters for the same vector locations. Reference [9] presents a common-mode voltage-elimination scheme for this inverter configuration. A three-level inverter configuration formed by cascading two two-level inverters has been presented in [10], where the inverter scheme uses fewer DC sources compared to series-connected H-bridge inverters, and does not suffer from neutral-point fluctuations. A three-level PWM scheme has been proposed using an H-bridge five-level inverter to reduce the common-mode voltages [12]. The five-level H-bridge configuration used in this scheme requires six isolated power supplies, and the implementation of the scheme requires two separate controllers for separate H-bridges [12].

An inverter configuration is presented for induction motor with open-end windings, using two three-level inverters fed from both ends, resulting in output motor phase voltages equivalent to a five-level conventional NPC inverter [11]. Isolated power supplies are used for individual DC links to suppress the common-mode currents in the phase windings [11] resulting from common-mode voltages. The multiplicity of individual three-level inverter switching states, with which the space vector combinations are generated in the above five-level configuration, can be exploited in an efficient manner to eliminate the common-mode voltage problem. In this paper, the switching states of individual three-level inverters are grouped according to the level of common-mode voltage in the pole voltages of the inverter. When only those vector combinations belonging to

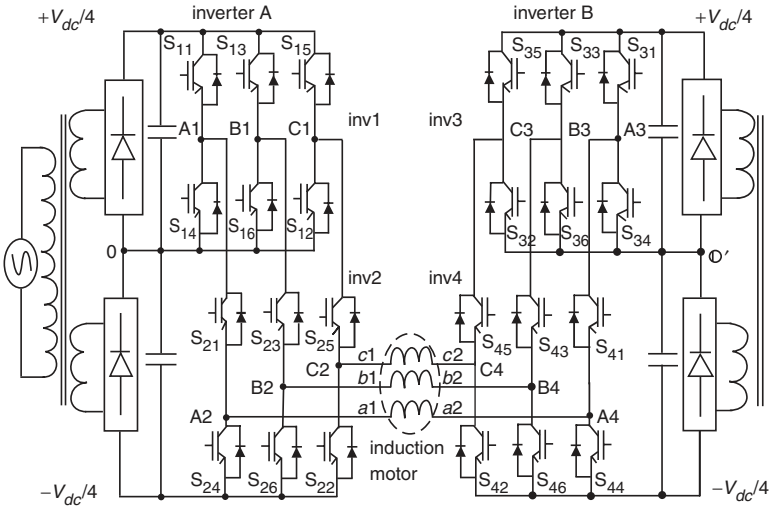


Fig. 1 *Five-level inverter configuration*

one group are used to switch the inverters from both sides, the resultant common-mode voltage across the phase will be zero. In the present work, a common-mode elimination scheme is proposed for the above configuration [11], with appropriate selection of switching states of individual three-level inverters, such that the common-mode voltage is totally eliminated from the inverter pole voltages and the phase windings of the induction motor. As the common-mode voltages are absent in this scheme, the possibility of common-mode currents, electrostatic coupling and associated problems are also eliminated. The problems associated with the conventional NPC inverter configuration, i.e. the neutral-point fluctuations, are also absent in the present work. The proposed three-level voltage space phasor generation with zero common-mode voltage requires only two isolated power supplies as compared to H-bridge topology [12], which requires six isolated power supplies. This demonstrates the superiority of the proposed inverter configuration over the NPC or H-bridge topologies with common-mode elimination. A simple three-level PWM algorithm is presented, which is based only on the instantaneous amplitudes of reference phase voltages. The proposed scheme is experimentally verified on a 1.5 kW open-end winding induction motor drive, in the linear as well as in the over modulation range.

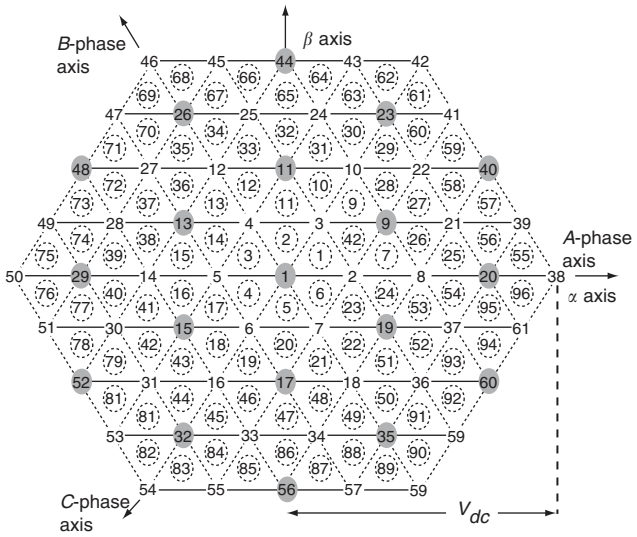


Fig. 2 *Five-level inverter voltage space vector representation (voltage space phasor locations resulting in zero common-mode voltage are shown shaded)*

2 Five-level inverter scheme for open-end winding induction motor drive

Figure 1 shows the schematic of an induction motor drive with open-end winding fed by a multilevel inverter. The inverter of Fig. 1 generates the phase voltages across the induction motor windings, similar to a conventional five-level inverter [11]. The drive configuration of Fig. 1 consists of two three-level inverters (inverter A and inverter B), which feed the induction motor from both ends. Each three-level inverter is formed by cascading two conventional two-level inverters, as shown in Fig. 1 [10]. Inverter A is formed by cascading the inverters Inv1 and Inv2, whereas inverter B is formed by cascading inverters Inv3 and Inv4. Four isolated power supplies consisting of isolation transformers and rectifiers are required for the inverter system of Fig. 1 to avoid the flow of common-mode currents in the motor phase windings. The DC link voltage of each rectifier, feeding top and bottom inverters, is $V_{dc}/4$. The pole voltage of inverter A (V_{A2o}), can be $+V_{dc}/4$ when the top switches (for example S_{11} and S_{21}) are closed, zero when the bottom switch of top inverter and top switch of bottom inverter (for example S_{12} and S_{21}) are closed and $-V_{dc}/4$ when the bottom switch of bottom inverter (for example S_{24}) is closed. The above voltages are specified with respect to middle bus point O.

The voltage space phasor combinations for all the switching states of inverter A and inverter B will result in three-level voltage space vector structures [10]. All possible combinations of switching states of inverter A and inverter B result into 61 voltage space phasor locations, forming 96 triangular sectors, as shown in Fig. 2. There are a total of 729 different combinations possible from the combined inverter fed drive [11]. The switching combinations at certain voltage space phasor locations will result in zero common-mode voltage at the pole of the inverters as well as at the machine phase windings. These voltage space phasor locations are shown shaded in Fig. 2. Using these locations a three-level voltage space phasor structure with common-mode voltage elimination is investigated, in the Section 3.

3 Proposed three-level voltage space phasor generation with common-mode voltage elimination

The common-mode voltage generated in the pole voltage of inverter A is expressed as [3]:

$$V_{CM1} = (V_{A2O} + V_{B2O} + V_{C2O})/3 \quad (1)$$

while the common-mode voltage generated in the pole voltage of inverter B is expressed as:

$$V_{CM2} = (V_{A4O} + V_{B4O} + V_{C4O})/3 \quad (2)$$

V_{CM1} and V_{CM2} are the common-mode voltages generated by inverter A and inverter B and are applied from opposite ends of induction motor phases. The resultant common-mode voltage applied to the motor phase winding can be written as:

$$V_{CM} = V_{CM1} - V_{CM2} \quad (3)$$

Unless, isolation transformers are used to isolate the DC links from both sides, these common-mode voltages may result in large triplen (common-mode) currents in the motor phases [11]. The isolation transformers are bulky, and also add to the cost of the drive. The magnitude of the common-mode voltages V_{CM1} and V_{CM2}, for various switching states of inverter A and inverter B, are shown in Table 1. The switching states, which produce the same common-mode voltage, are grouped in one group. Thus a total of seven groups can be identified as shown in Table 1. The switching states which produce minimum common-mode voltage in the pole voltages (i.e. switching states belonging to groups C, D and E) can be represented on a three-dimensional plane defined as the α–β–0 plane (where 0 corresponds to the common-mode voltage axis), as shown in Fig. 3.

When the switching states from group C (Table 1) are used to switch inverter A and inverter B, the resultant space phasor combinations can be represented by a three-level structure, as shown in Fig. 4. For example, when inverter A is switched with state '+ + −' and inverter B with state '− + +', the resultant voltage vector is shown in Fig. 4 as '+ + − − + +'. For all voltage space phasor locations (along with the multiple switching state combinations of inverter A and inverter B) in Fig. 4, the first switching state in each pair corresponds to inverter A, while the second one corresponds to switching state of inverter B (Fig. 4). (In Fig. 4, '+', '0' and '−' indicates the inverter pole voltage level of $+V_{dc}/4$, zero and $-V_{dc}/4$ V, respectively.) Here, the inverter A and inverter B pole voltages have common mode voltage (V_{CM1}, V_{CM2}) equal to $V_{dc}/12$), whereas the common-mode voltage (V_{CM}) in the motor phases is zero. Similarly, when the switching states from group E are used to switch inverter A and inverter B, the resultant space phasor combinations can be represented by a similar three-level structure, as shown in Fig. 5. In this case, the individual inverter pole voltage has common-mode voltage (V_{CM1}, V_{CM2}) equal to $-V_{dc}/12$ (Table 1), and the common-mode voltage (V_{CM}) in the motor phases is zero.

When the switching states belonging to group D (Table 1) are used to switch inverter A and inverter B, the resultant space phasor combinations can be represented by a similar three-level structure, as shown in Fig. 6. Here, the inverter A and inverter B pole voltage have zero common-mode voltage (V_{cm1}, V_{cm2}) (Table 1), and the motor phase voltages also have zero common-mode voltage (V_{CM}). The

Table 1: Common-mode voltage generated by inverter A and inverter B

Group	Switching states of three-level inverters	Common mode voltage V_{CM1}, V_{CM2}
A	+++	$+V_{dd}/4$
B	++0, +0+, 0++	$+V_{dd}/6$
C	+−+, ++−, −++, 00+, 0+0, +00	$+V_{dd}/12$
D	000, +0−, +−0, 0+−, 0−+, −+0, −0+	*0*
E	−+−,−−+, +−−, 0−0, 00−, −00	$-V_{dd}/12$
F	0−−, −0−, −−0	$-V_{dd}/6$
G	−−−	$-V_{dd}/4$

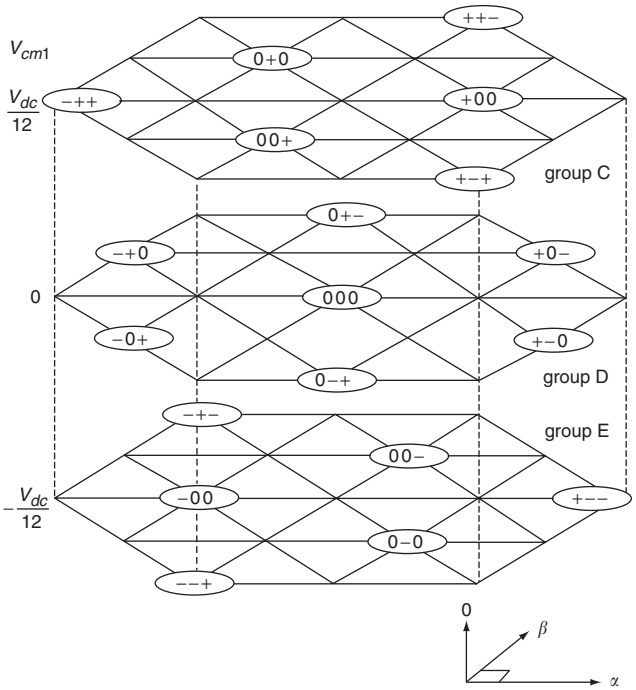


Fig. 3 *Representation of voltage space vectors of inverter A (belonging to groups C, D and E) in a three-dimensional plane: α–β–0 plane*

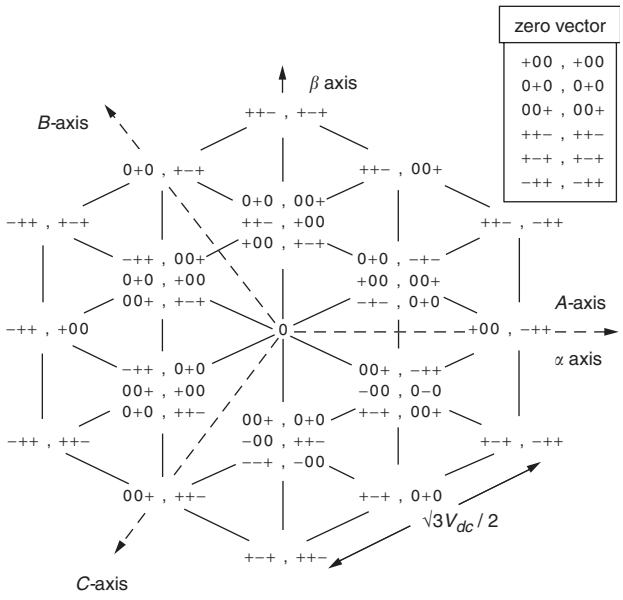


Fig. 4 *Resultant three-level space vector configuration when group C switching states are used to switch inverter A and inverter B*

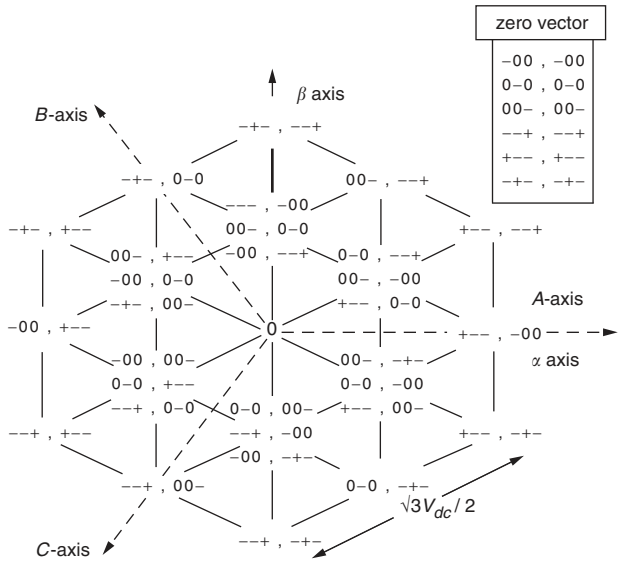


Fig. 5 *Resultant three-level space vector configuration when group E switching states are used to switch inverter A and inverter B*

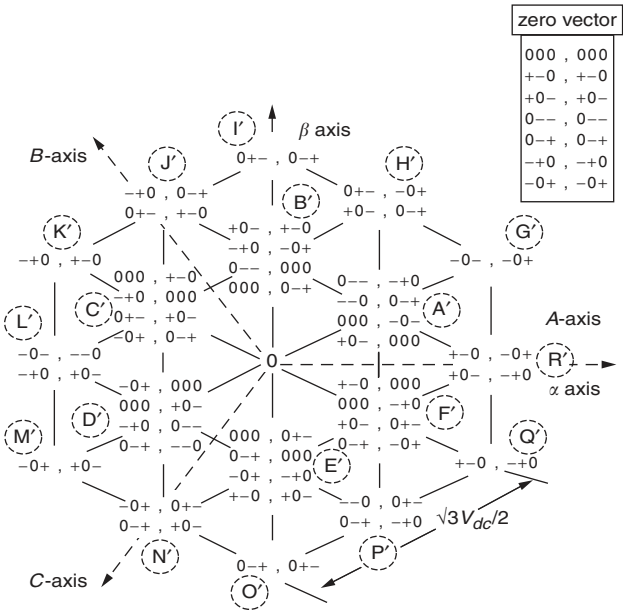


Fig. 6 *Resultant three-level space vector configuration when group D switching states are used to switch inverter A and inverter B*

seven voltage space vectors belonging to group D result in a total of 49 voltage space vector combinations, and their locations are as shown in Fig. 6. The common-mode voltages are completely eliminated in the phase windings as well as in the inverter system (pole voltages). The problems associated with the common-mode voltages inducing currents in the leakage capacitances are completely eliminated (as the electrostatic coupling between stator winding to stator iron and between stator winding and rotor iron is ineffective) in the present work. The need for isolated DC links from both sides is also eliminated in the proposed structure. The modified power schematic of the proposed three-level inverter drive configuration is as shown in Fig. 7.

The multiplicity of vector combinations for vectors of combined three-level inverters plays an important role, when deciding on the modulation scheme, to obtain

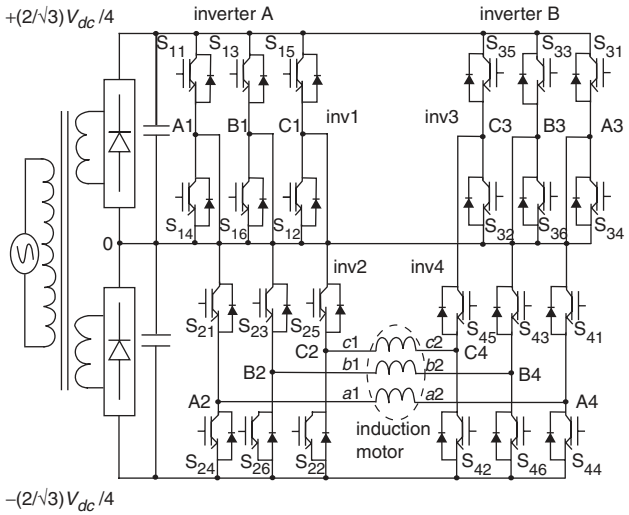


Fig. 7 *Schematic of modified three-level inverter drive scheme with common-mode voltage elimination*

minimum switching per inverter vector change, as described in the next Section. This is not possible with reduced common-mode three-level inverter structure, obtained with a five-level cascaded H-bridge configuration, as the space vectors locations do not exhibit multiplicity [12]. Moreover, the proposed configuration requires only two power supplies, whereas the scheme with the five-level H-bridge configuration requires six isolated power supplies [12].

4 PWM switching scheme for proposed three-level inverter drive with common-mode elimination

As described in the previous Section, for common-mode voltage elimination from phase voltage and from the inverter pole voltage, the switching states from group D gives best performance compared to group C or group E (Table 1). Therefore, switching combinations of only group D are considered for further analysis. It is to be noted that the maximum reference space vector possible in the linear range of modulation with this configuration is $3V_{dc}/4$ (with a total DC link voltage of $V_{dc}/2$) (Fig. 6). The corresponding amplitude of fundamental component in the phase voltage is $2/3 \times 3V_{dc}/4 = V_{dc}/2$, which is the same as the maximum peak amplitude of phase voltage generated by a conventional two-level inverter with sine PWM (i.e. 15% less than can be obtained with space vector PWM) [9]. This can be compensated for with an additional voltage boost of 15% to the individual DC links [9]. Therefore, in the present work, the DC link voltage of an individual two-level inverter (of cascaded three-level inverters) is $(2\sqrt{3}) \times V_{dc}/4$ (where V_{dc} is the DC link voltage required for the conventional two-level inverter, to produce the same peak phase voltage) (Fig. 7). With the additional boost by a factor of $2/\sqrt{3}$ in the DC link voltage, the magnitudes of the various space vectors are as shown in Fig. 8*b*. When inverter vector switches from G′ to H′, pole A2 of inverter A changes state from + to 0 and pole B2 of inverter A changes state from 0 to + (Fig. 6). The same change can be effected when pole A4 of inverter B changes states from − to 0 and pole B4 of inverter B changes state from 0 to −. Thus, for each vector change, simultaneous switching is required in two phases, from either inverter A or inverter B. This is from the fact that only seven (Group D) out of 27

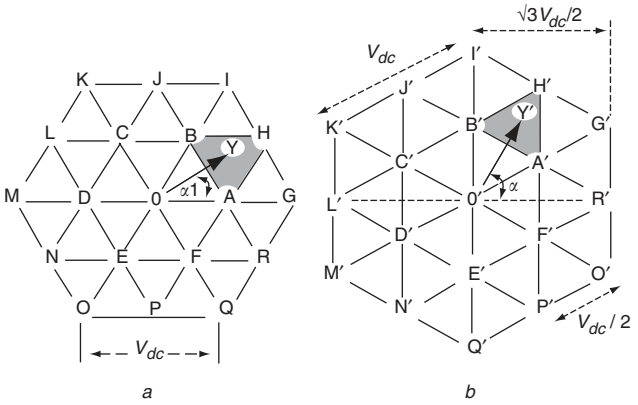


Fig. 8 *Transformation of actual reference vector OY′ to conventional three-level inverter space vector OY*
a Space vector locations of conventional three-level inverter
b Space vectors of proposed three-level inverter derive with common-mode voltage elimination

switching combinations are used for switching of three-level inverters A and B for the present work (Fig. 3).

A reference space vector of magnitude equal to 'V_{SR}' and rotating in the space at fundamental frequency is sampled at regular intervals 'T_S'. The sampled value of the reference space vector is then used to determine the inverter switching vectors and the time for which these vectors are required to be switched in a sampling interval. For example, consider the sampling interval when the tip of the reference vector is in a sector formed by A′G′H′ (Fig. 6). Here space vector OG′ can be uniquely obtained by switching inverter A with switching state '−+0' and inverter B with switching state '0+−'. The space vector OH′ can be obtained by switching inverter A and inverter B with switching states '0+−' and '−0+', respectively (Fig. 6). Alternatively, OH′ can also be obtained by switching inverter A and inverter B with switching states '+0−' and '0+−', respectively. This is possible because of the multiplicity of switching states of inverter A and inverter B at point H′ in Fig. 6. Similarly, OA′ can be obtained by four distinct switching state combinations of inverter A and inverter B. The switching states for vector locations OH′, OG′ and OA′ are selected such that only one inverter (our of inverter A and inverter B) switches for each switching subinterval in a sampling period, and thus minimum switching of inverter legs is ensured.

4.1 Mapping of reference space vector of proposed inverter to reference space vector of conventional three-level inverter

The voltage space phasor locations of the proposed three-level inverter with common-mode elimination (Fig. 6) are compared with the space vector locations of a conventional three-level inverter with DC link voltage of V_{dc}, as shown in the Fig. 8. Consider a reference space vector OY′ at a sampling instant at an angle α with respect to A phase axis. The reference space vector can be realised by switching appropriate vectors from inverter A and inverter B. From Fig. 8, it can be noted that the triangular sectors for the proposed three-level inverter structure are leading by an angle 30°, with respect to the respective triangular sectors of the conventional three-level inverter structure (Fig. 8*a*). The length of side of the triangular sector of the proposed three-level structure (with a 15% voltage boost in the DC link) is equal to that of the triangular sector of a conventional three-level inverter. Therefore, the corresponding space vectors (forming a triangular sector) of the proposed

Table 2: Three-level inverter space vector locations and corresponding switching states of inverter A and inverter B and gate signals

Inverter space vector locations generated by three-level PWM controller	Switching state of inverter A	Switching state of inverter B	Gate signals for inverter A						Gate signals for inverter B					
			S_{11}	S_{21}	S_{13}	S_{23}	S_{15}	S_{25}	S_{31}	S_{41}	S_{33}	S_{43}	S_{35}	S_{45}
0	000	000	0	1	0	1	0	1	0	1	0	1	0	1
A	+0−	000	1	1	0	1	0	0	0	1	0	1	0	1
B	000	0−+	0	1	0	1	0	1	0	1	0	0	1	1
C	−+0	000	0	0	1	1	0	1	0	1	0	1	0	1
D	000	+0−	0	1	0	1	0	1	1	1	0	1	0	0
E	0−+	000	0	1	0	0	1	1	0	1	0	1	0	1
F	000	−+0	0	1	0	1	0	1	0	0	1	1	0	1
G	+0−	−0+	1	1	0	1	0	0	0	0	0	1	1	1
H	0+−	−0+	0	1	1	1	0	0	0	0	0	1	1	1
I	0+−	0−+	0	1	1	1	0	0	0	1	0	0	1	1
J	0+−	+−0	0	1	1	1	0	0	1	1	0	0	0	1
K	−+0	+−0	0	0	1	1	0	1	1	1	0	0	0	1
L	−0+	+−0	0	0	0	1	1	1	1	1	0	0	0	1
M	−0+	+0−	0	0	0	1	1	1	1	1	0	1	0	0
N	−0+	0+−	0	0	0	1	1	1	0	1	1	1	0	0
O	0−+	0+−	0	1	0	0	1	1	0	1	1	1	0	0
P	+−0	0+−	1	1	0	0	0	1	0	1	1	1	0	0
Q	+−0	−+0	1	1	0	0	0	1	0	0	1	1	0	1
R	+−0	−0+	1	1	0	0	0	1	0	0	0	1	1	1

inverter, are leading with respect to those of the conventional system by an angle 30° (Fig. 8). For example OA′ is leading OA by 30°. Therefore we can obtain the reference space vector of the conventional system from the reference space vector of the proposed inverter system as follows:

$$V_{SR1} = V_{SR} \times e^{-30^\circ} \tag{4}$$

The reference space vector V_{SR} is used to generate the PWM signals for a conventional three-level inverter. The vectors generated by the controller are then mapped to the vectors of the proposed three-level inverter with common-mode elimination, as described in the following.

4.2 Generation of voltage space vectors of proposed three-level inverter from voltage space vectors of conventional three-level inverter

A space phasor based PWM algorithm is used to generate the switching times for the vectors of a conventional three-level inverter [9, 13]. The inverter switching vectors and the time duration for which the inverter space vectors to be switched, during a switching interval T_S, are determined directly from the instantaneous amplitude of the reference voltage [9, 13]. Thus it avoids the use of a look-up table for sector identification and increases the speed of computation, making it useful for real-time implementation. The algo-

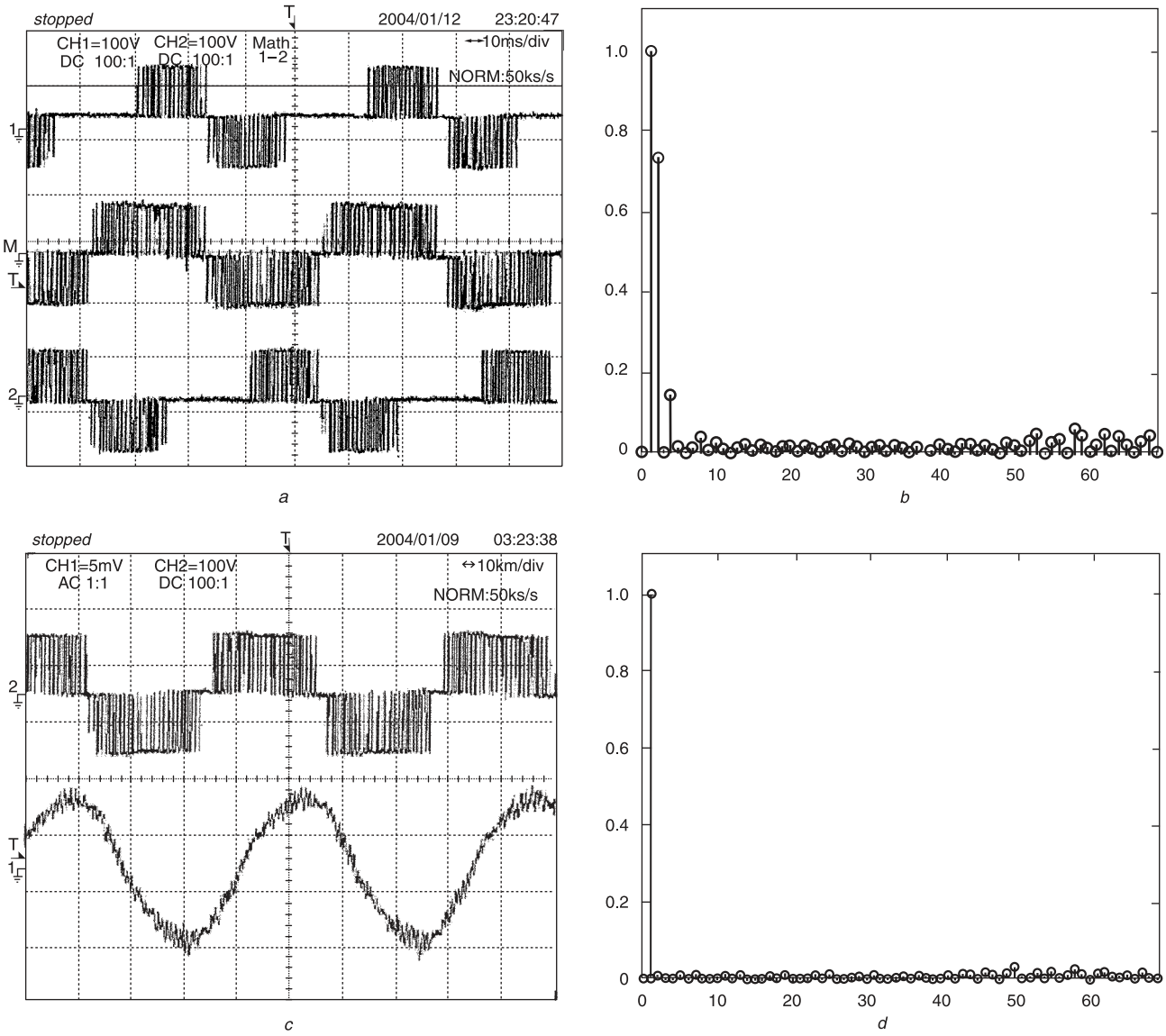
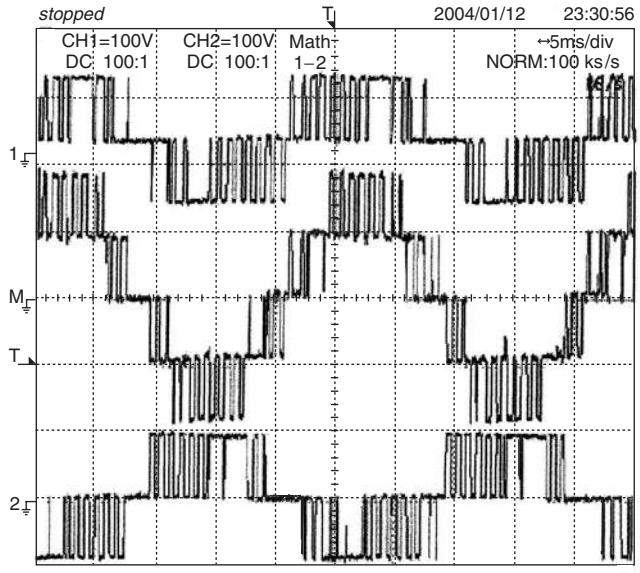


Fig. 9

a Pole voltage waveforms (V_{A2O} and V_{A4O}) for modulation index 0.4 (middle trace is *A*-phase voltage waveform)
x-axis: 1 div. = 10 ms, *y*-axis: 1 div. = 100 V
b Normalised harmonic spectrum for pole voltage of Fig. 9*a*
c A-phase current and phase voltage for modulation index 0.4 (reference space vector is in inner layer)
x-axis: 1 div. = 10 ms, upper trace; *y*-axis: 1 div. = 100 V, lower trace; *y*-axis: 1 div. = 2A (no load)
d Normalised harmonic spectrum for phase voltage of Fig. 9*c*
e Pole voltage waveforms (V_{A2O} and V_{A4O}) for modulation index 0.7 (i.e. when reference space vector is in outer layer). Middle trace is the *A*-phase voltage; *y*-axis = 100 V/div. and *x*-axis is 5 ms/div.
f Normalised harmonic spectrum for pole voltage of Fig. 9*e*
g A-phase current and phase voltage for modulation index 0.7 (i.e. when reference space vector is in outer layer)
x-axis: 1 div. = 5 ms, upper trace; *y*-axis: 1 div. = 100 V lower trace; *y*-axis: 1 div. = 2A (no load)
h Normalised harmonic spectrum for phase voltage of Fig. 9*g*



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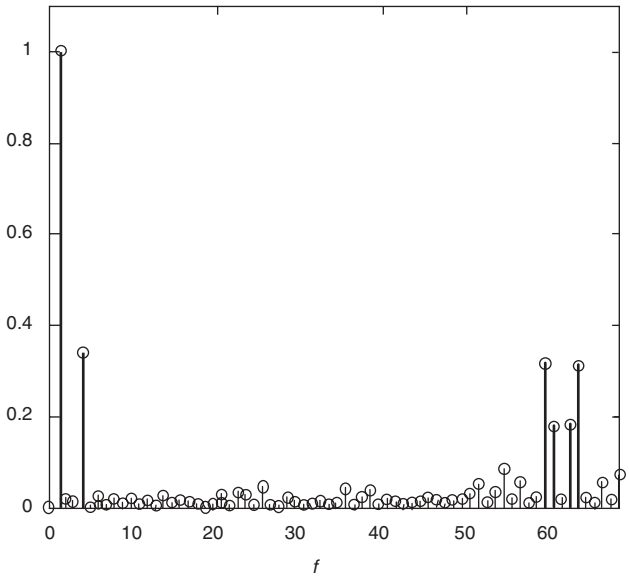

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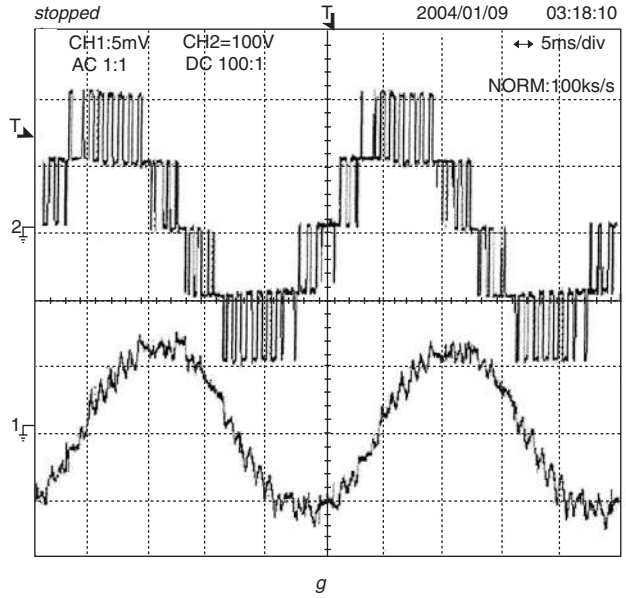

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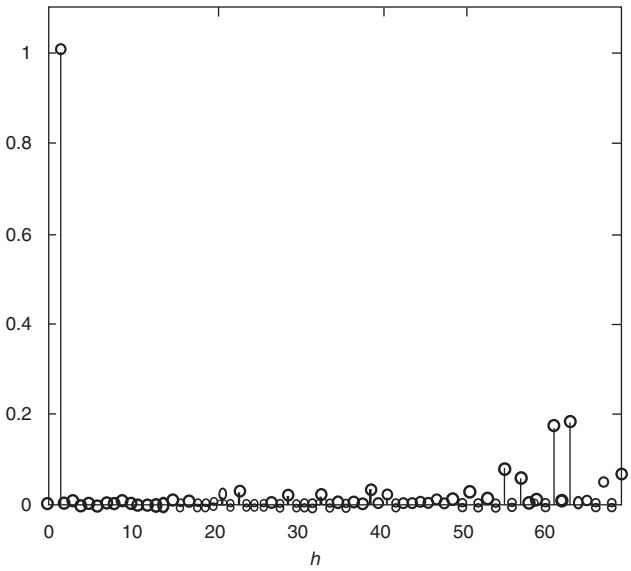

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Fig. 9 *(Continued)*

rithm is explained in Appendix 1. Digital logic is used to translate the vectors generated by the PWM algorithm for the conventional three-level structure to the vectors of the proposed three-level inverter drive. As shown in Fig. 8, a unique mapping is defined between the vector locations of a conventional three-level inverter and those of the proposed three-level inverter system with common-mode elimination. For the reference space vector OY, the conventional three-level PWM algorithm generates the timings for switching the vectors OA, OB and OH in the given sampling interval. These vectors can be uniquely transferred to the voltage space vectors of the proposed three-level inverter, which are shown as OA′, OB′ and OH′ for generating the reference space vector OY′. Vectors OA′, OB′ and OH′ are realised by switching appropriate switching states from inverter A and inverter B (Fig. 6). Thus the modulation scheme involves the following steps:

(*a*) Sample the reference space vector V_{SR} with a sampling interval T_S.

(*b*) Compute the modified reference vector V_{SR1} using (4).

(*c*) Determine the switching times from the modified reference space phasors (refer to Appendix 1).

(*d*) Translate the conventional three-level inverter vectors forming the mapped triangular sector to actual vectors of the proposed three-level inverter with common-mode elimination.

As explained in the previous subsection, the multiplicity of switching states of inverter A and inverter B with which the vector combinations are generated gives many options to select the switching pattern for inverter A and inverter B. The combinations of switching states of individual three-level inverters selected to realise the resultant space vector locations of the proposed three-level inverter are as shown in Table 2.

4.3 Generation of gate signal for inverter A and inverter B

The PWM signals for three phases are generated using full compare units of digital signal process (DSP) TMS320F240. The PWM signals and the level signals *A_Level, B_Level* and *C_Level* are taken out from DSP I/O ports through A2, B2 and C2 (refer to Appendix 1). The decoding of *A_Level*, *B_Level* and *C_Level* signals along with *PWM_A*, *PWM_B* and *PWM_C* signals is done using

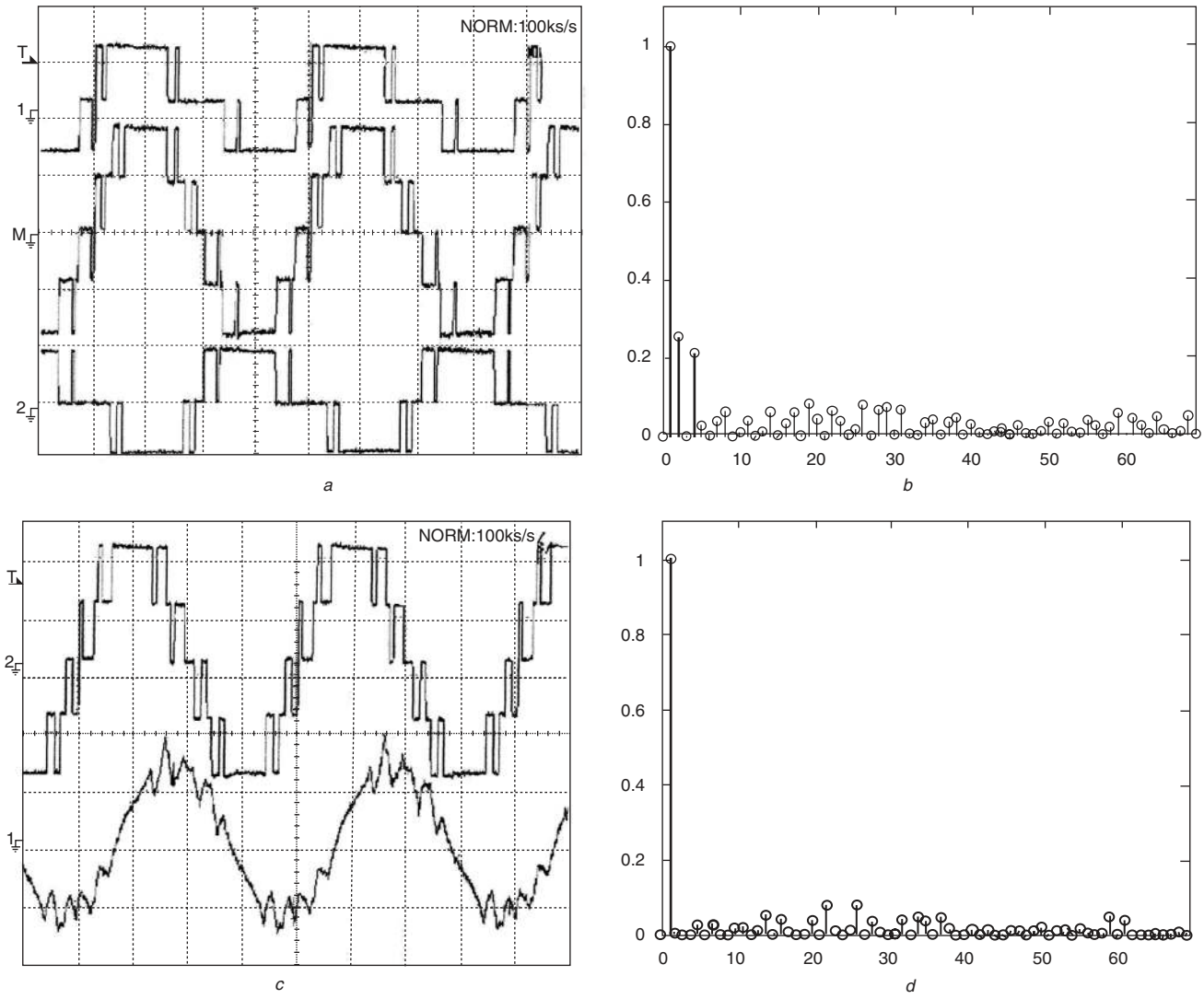

Fig. 10
a Pole voltage waveforms (V_{A2O} and V_{A4O}) for modulation index of 0.95 (over-modulation) (middle trace is *A*-phase voltage) *x*-axis: 1 div. = 5 ms, *y*-axiz: 1 div. = 100 V
b Normalised harmonic spectrum for pole voltage of Fig. 10*a*
c A-phase current and resultant phase voltage for modulation index 0.95 (over modulation)
x-axis: 1 div. = 5 ms, upper trace; *y*-axis: 1 div. = 100 V lower trace; *y*-axis: 1 div. = 2A (no load)
d Normalised harmonic spectrum for phase voltage of Fig. 10*c*

PALCE22V10 (a CMOS flash erasable second-generation programmable logic array device), which generates the switching signals for both of the three-level inverters (Table 2). The resultant vector (Fig. 6) is decided by the combination of inverter A and inverter B switching vectors.

5 Experimental results and discussion

The proposed scheme has been tested on a 1.5 kW three-phase induction motor (see Appendix 2 for motor data) drive with V/f control for different modulation indices covering different speed ranges (two-level, three-level and over-modulation region). The DC link voltage of around 100 V is used for each two-level inverter. In the proposed PWM scheme, the deadbands of the inverter legs are properly tuned, such that any common-mode voltage generated due to dead-band mismatch are avoided. The modulation index is varied from low modulation index to the over-modulation region. The results are presented in Figs. 9–11. The carrier frequency used for PWM generation is limited to around 1.25 kHz.

The pole voltage waveforms of inverter A (V_{A2o}) and inverter B (V_{A4o}) for modulation index 0.4 (i.e. when the reference space vector is in the inner layer) are shown in Fig. 9*a*. Figure 9*b* shows the normalised harmonic spectrum of the pole voltage. The phase-A current and the resultant phase voltage across the phase-A winding of the induction motor are shown in Fig. 9*c*, and the normalised harmonic spectrum of the phase voltage is shown in Fig. 9*d*. Both the pole voltage and the phase voltage show the absence of triplen voltage content. The waveforms do not have half-wave symmetry, as only some selected vectors of both inverters are switched. The pole voltage shows significant even harmonics, which are absent in the phase voltage waveforms. The even harmonics cancel each other in phase voltage and the fundamental component gets added up. Similarly, the pole voltage waveforms, when the reference space vector is in the outer layer (modulation index = 0.7), are shown in Fig. 9*e*. Figure 9*f* shows the normalised harmonic spectrum of the pole voltage. The resultant phase voltage and phase current are shown in Figs. 9*g*, and *h* shows the normalised harmonic spectrum of the phase voltage. Here also the pole voltages and phase voltages do

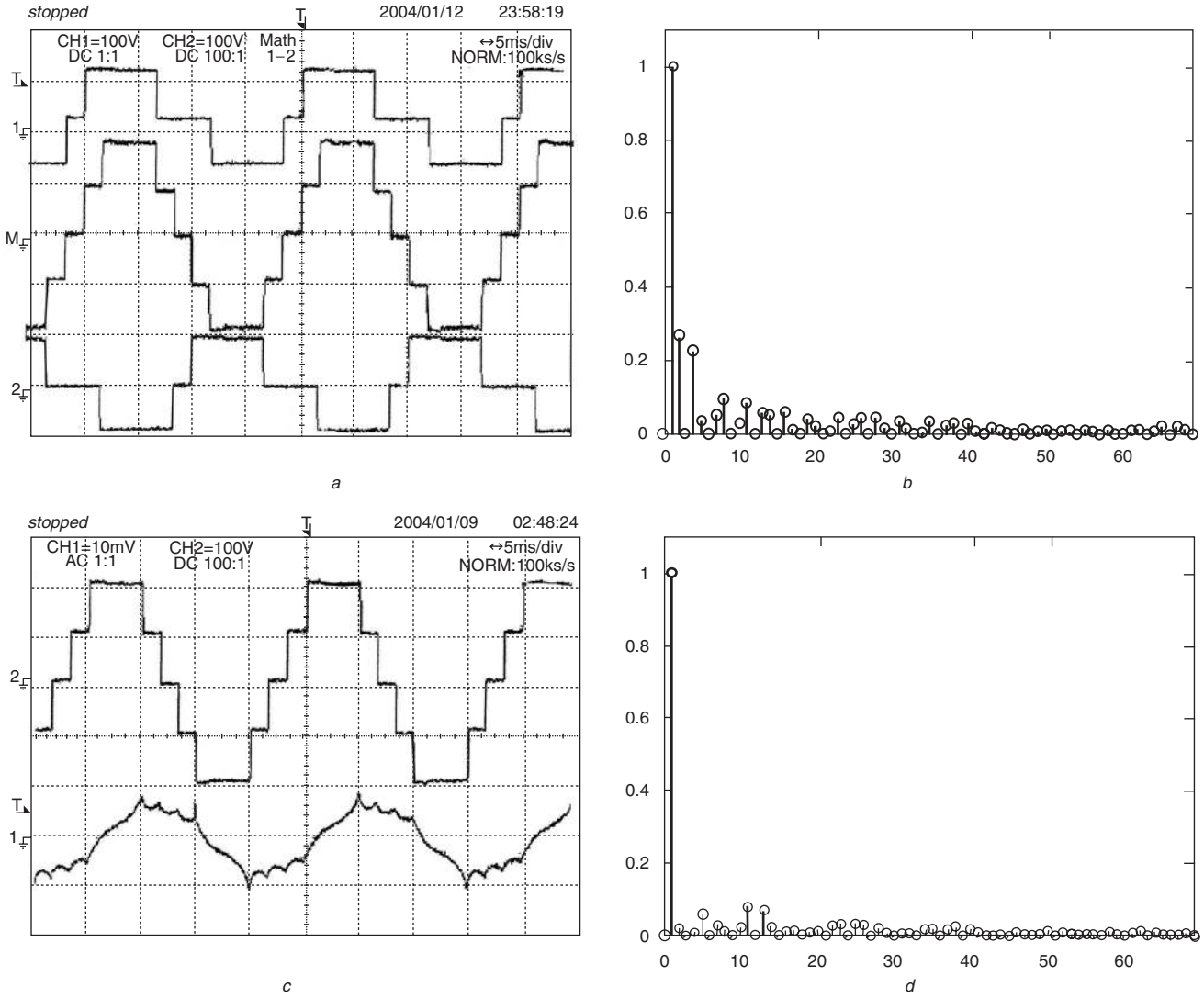

Fig. 11
a Pole voltage waveforms (V_{A2O} and V_{A4O}) for 12 step mode. Middle trace is *A*-phase voltage waveform
x-axis: 1div. = 5 ms, *y*-axiz: 1 div. = 100 V
b Normalised harmonic spectrum for pole voltage of Fig. 11*a*
c A-phase current and resultant phase voltage for 12-step mode
x-axis: 1div. = 5 ms, upper trace; *y*-axis: 1 div. = 100 V lower trace; *y*-axis: 1 div. = 2A (no load)
d Normalised harmonic spectrum for phase voltage of Fig. 11*c*

not contain any triplen harmonic order. The motor is speeded up to the over-modulation range and similar observations are taken. Figure 10*a* shows the pole voltages in the over-modulation region. The phase voltage and phase current during over-modulation are shown in Fig. 10*c*. Figure 10*b* and *d* show the normalised harmonic spectra of the pole voltages and the phase voltage of Figs. 10*a* and *c*, respectively. Here, also, it can be noted that the triplen components are absent. The phase voltages as well as line voltages show 5th and 7th harmonic components, which are apparent in the over-modulation range. The inverter system is operated in 12-step mode and the corresponding pole voltages are shown in Fig. 11*a*. The respective phase voltage and phase current, during 12-step mode, are shown in Fig. 11*c*. Figures 11*b* and *d* show the normalised harmonic spectra of pole voltage and phase voltage, in which the common-mode components are absent. In the 12-step mode, also, it can be seen that the 5th and 7th harmonic components are present in the pole voltage and in the phase voltage.

6 Conclusions

A three-level inverter configuration with common-mode elimination is proposed for an induction motor drive with open-end windings. The individual switching states of the inverters, feeding from each side, are grouped according to the common-mode voltage they generate in the inverter pole voltage, and are represented in a three-dimensional space. It has been shown that, when the inverters on both sides of motor phase are switched with switching states from only one group, the common-mode voltage generated across the motor phases is zero. This suppresses the common-mode currents, which otherwise will flow in the machine windings. With the proposed scheme, the switching states of individual three-level inverters are chosen such that the common-mode voltage is absent in the pole voltages. Thus the common-mode voltages are completely eliminated from the inverter pole voltages as well as from the motor phases. The proposed topology with a SVPWM scheme has been implemented for a 1.5 kW induction motor drive with open-

end windings. For the proposed inverter configuration, the DC link voltage requirement is only half that of the conventional three-level inverter configuration with common-mode elimination. Only two power supplies are required in the proposed scheme, whereas the equivalent three-level inverter configuration with common-mode elimination based on H-bridge topology requires six isolated power supplies.

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9 Appendix 1

PWM algorithm for inverter leg switching time calculation for three-level inverter [13]

1 Read V_A, V_B and V_C values and find the reference space vector V_{SR} using the relation

$$V_{SR} = V_A + V_B \times e^{j120^\circ} + V_C \times e^{j240^\circ}$$

2 Calculate the reference space vector V_{SR1} using transformation $V_{SR1} = V_{SR} \times e^{-j30^\circ}$.

3 Calculate the instantaneous modified amplitudes of phase voltages V_{as}, V_{bs} and V_{cs} for the three-level PWM algorithm from V_{SR1}.

4 Determine switching vectors for the three-level inverter using these instantaneous amplitudes of the reference phase described as below:

(*a*) Convert the phase voltages into equivalent time T_{as},T_{bs} and T_{cs} where

$$T_{as} = V_{as} \times \frac{T_s}{V_{dc}/2}, T_{bs} = V_{bs} \times \frac{T_s}{V_{dc}/2}, T_{cs} = V_{cs} \times \frac{T_s}{V_{dc}/2}$$

(*b*) $T_{offset1} = -(max(T_{as}, T_{bs}, T_{cs}) + min(T_{as}, T_{bs}, T_{cs}))/2$

(*c*) Determine $T^*_{as}, T^*_{bs} T^*_{cs}$ as $T^*_{as} = T_{as} + T_{offset1}$, $T^*_{bs} = T_{bs}$ $T_{offset1}$ $T^*_{cs} = T_{cs} + T_{offset1}$

(*d*) if ($T^*_{a,b,cs}$ is negative).{$T_{A,B,C\_Cross} = T_s + T^*_{a,b,cs}$ A,B,C_Level $= 0$}

elseif (($T^*_{a,b,cs}$ is positive){$T_{A,B,C\_Cross} = +T^*_{a,b,cs}$ and A,B,C_Level $= 1$}

*(A, B, C_level $= 0$ implies that the sampled A,B,C values lie in the lower triangle for sinusoidal PWM and the inverter leg ahs to switch between '0' and '−' levels. $A, B, C_{\text{Level}} = 1$ implies that the sampled values lie in the upper triangle and the inverter leg has to switch between '+' and '0'.)

(*e*) Sort $T_{\_A\_Cross}, T_{\_B_Cross}, T_{\_C\_Cross}$ The maximum of $T_{\_A\_Cross}, T_{\_B\_Cross}, T_{\_C\_Cross}$, is $T_{\_third\_cross}$. The minimum of $T_{\_A\_Cross}, T_{\_B\_Cross}, T_{\_C\_Cross}$, is $T_{\_first\_cross}$ and the rest is $T_{\_second\_cross}$.

Assign first_cross_phase, second_cross_phase and third_cross_phase according to which phase determined $T_{\_first\_cross}$, $T_{\_second\_cross}$ and $T_{\_third\_cross}$ [13].

(*f*) if $T_{\_third\_cross} - T_{\_first\_cross} > T_S$ go to step *j*

(*g*) Calculate $T_{offset2}$ as follows:

$T_{middle} = T_{\_third\_cross} - T_{\_first\_cross}$, $T_o = T_s - T_{middle}$ and therefore,

$T_{offset2} = (T_o/2) - T_{\_first\_cross}$

(*h*) Determine T_{ga},T_{gb},T_{gc} as

$T_{ga} = T_{\_A\_Cross} + T_{-offset2}$, $T_{gb} = T_{\_B\_Cross} + T_{-offset2}$, $T_{gc} = T_{\_C\_Cross} + T_{-offset2}$

(*i*) Go to step 5.

(*j*) Over-modulation case:

If $(T_{\_third\_cross} - T_{\_second\_cross}) < (T_{\_second\_cross} - T_{\_first\_cross})$

$T_{offset2} = -T_{\_first\_cross}$

else

$T_{offset2} = T_s - T_{\_third\_cross}$

(*k*) $T_{g\_first\_cross} = 0, T_{g\_second\_cross} = T_s + T_{-offset2}$, $T_{g\_third\_cross} = T_s$.

(*l*) If $T_{g\_second\_cross} < 0, T_{g\_second\_cross} = 0$.

(*m*) If $T_{g\_second\_cross} > T_s, T_{g\_second\_cross} = T_s$.

(*n*) Determine T_{ga}, T_{gb}, T_{gc} by equating $T_{g\_first\_cross}$, $T_{g\_second\_cross}$ and $T_{g\_third\_cross}$ to T_{ga}, T_{gb}, T_{gc} depending on the phase, which determines first cross, second cross and third cross during the switching interval [13].

5 Using the pwm_*a*, pwm_*b* and pwm_*c* signals and level signals A_Level, B_Level and C_Level, generate the switching signals for inverter A and inverter B using the digital logic presented in Table 2.

6 Go to step 1.

10 Appendix 2

Motor data

1.5 kW, 400 V, 50 Hz, four-pole, $R_s = 2.08\,\Omega$, $R_r = 1.9\,\Omega$, $L_r = 0.28$ H, $L_s = 0.28$ H, $M = 0.272$ H.