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A Three-Phase Four-Leg Flying-Capacitor Multi-Level Inverter-based Active Power Filter for Unbalanced Current Operation

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Abstract—The paper describes a new application of flying capacitor multi-level inverters whereby a three-phase, four-leg three-level inverter is used for harmonic current cancellation and unbalanced current compensation in a 4-wire system. A direct 3D-PWM scheme is developed to deal with the increased state redundancy in the four-leg flying capacitor multilevel inverter. Test results show much superior performance in the four-leg case, which may allow the use of smaller DC supply capacitors. A new modified dead–beat current control algorithm is proposed and combined successfully with the 3D-PWM modulation technique in a hardware demonstrator of a complete active filter.

Index Terms—STATCOM, Active power filtering, Multi-level converters, 3D-Pulse width modulation, Unbalanced power systems

I INTRODUCTION

The growing use of power electronic controlled-equipment is now posing a challenging problem through the presence of harmonics within 3-phase 4-wire power distribution networks. Such systems may supply large variable speed drives and high-power phase-controlled rectifiers installed in large office buildings, they now also supply large numbers of relatively low-power single-phase, harmonic generating appliances, such as PCs, microwave ovens, and fluorescent lighting incorporating electronic ballasts. With many operating simultaneously, the harmonic components may accumulate to significant levels at the Point of Common Coupling (PCC). Consequently they cause disturbances to the PCC voltage, and give rise to undesirable effects in distribution equipment such as increased losses, resonance and even damage. Load imbalance is a distinct effect causing fundamental and harmonic zero-sequence currents in the neutral line which are added to triplen harmonics generated by single-phase non-linear loads. A recent investigation conducted by the authors on a university building power network [1] revealed the severity of load current unbalance and harmonic contaminations.

Power electronic-based compensators are effective in eliminating harmonics and compensating reactive power, yet most reported work considers their use in balanced three-phase systems; applications for unbalanced three-phase four-wire systems such as those at distribution level have received less attention. The limited reported research concentrates mainly on two-level [2 – 5] or diode-clamped multi-level inverters (DCMI) [6 – 8].

This paper presents a new three-phase four-leg flying capacitor inverter for active power filtering in three-phase four-wire unbalanced distribution systems. Although the characteristics of the flying-capacitor multi-level inverter (FCMI) are well known and reported [9, 10], the three-phase four-leg configuration has received little or no consideration. Its main advantage is in having the fourth leg specifically for managing the neutral-line current, which improves stability and utilisation of the DC-bus voltage, as well as increasing zero-sequence output capability.

Control of a multi-level three-phase four-leg FCMI is challenging since it has many more switching states for the same output voltage vectors than other topologies with the same number of levels. 3D-Space Vector Modulation (SVM) techniques have been proposed over recent years [7, 8, 11, 12] and in particular R. Zhang *et al.* developed a 3D-SVM algorithm for two-level four-leg inverters [11], where the proposed method employed the α-β-0 coordinate system. Dai *et al.* have subsequently reported their development of 3D-SVM and Direct 3D-PWM schemes for both four-leg diode-neutral-point clamped multilevel Inverters (DCMI) and their three-leg counterpart with a centre-split capacitor [7, 8]. Developments in multi-level 3D-SVM include algorithm simplification through elimination of the Clarke transform, giving rise to the so-called natural or a-b-c coordinate system [12, 13]. However, all these methods were still exclusively applied to DCMI circuits. For the control of FCMIs with four phase legs, the sequence of switching vectors should be arranged taking into account the current direction, the capacitor voltages at different levels and the desired reference voltage vector. The design is particularly challenging during transient states when the current direction is uncertain and voltage values may depart significantly from their balanced levels.

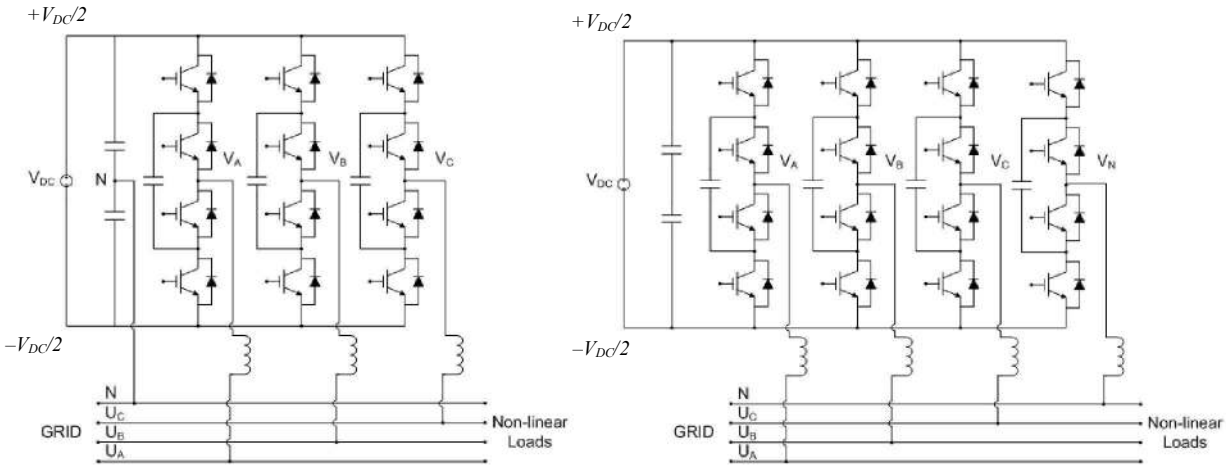
This paper presents a new 3D-PWM scheme dedicated to FCMIs of four-leg. The method embeds a closed-loop voltage balancing scheme into the Direct 3D-PWM algorithm. The proposed methods can select the most suitable switching sequence to generate desired output voltage waveforms for compensating imbalance in a three-phase four-wire system, and simultaneously minimise the fluctuation of inverter capacitor voltages at each level. This scheme has been applied to a practical 10 kVA, 450 V three-level four-leg Flying Capacitor Multilevel Inverter (FCMI)-based active power filter. A new control scheme which combines deadbeat operation with the derivative of the reference current is developed for eliminating both harmonics and unbalanced load current. The active power

filter (APF) architecture and the principle of its control scheme are described. Comparison of this proposed scheme with previous published work has been made. Practical evaluations show its steady state and transient operations for a typical unbalanced nonlinear load which validates fully this new APF device and the control algorithm.

II. FCMIs for Three-Phase Four-Wire Systems

Three-phase inverters, regardless of their topology and number of levels, can be used in a 3-Phase 4-Wire System either as a three-phase three-leg circuit with split dc capacitor for neutral point connection, or a three-phase four-leg with the last leg as the neutral leg [2]. For flying capacitor multi-level inverters these configurations are shown in Fig. 1. Both can be used as power conditioners though the four-leg one requires more switching devices, gate drivers and protection circuits. The phase inductors between the grid lines and inverter limit the harmonic currents due to fast switching. A three-level FCMI is used here as an example, although the principles are general.

With the circuit in Fig. 1(a) under unbalanced load conditions, neutral current flows through the DC-bus capacitors, leading to neutral-point potential variations and DC-bus voltage ripples. This, in turn, increases fluctuations of the phase capacitor voltages and degrades the output voltage waveforms. Rather than increasing the DC-bus capacitance to reduce voltage fluctuation, a better approach is to use a fourth leg, as shown in Fig. 1(b), specifically to manage the neutral-line current. This improves stability and utilisation of the DC-bus voltage, as well as increasing zero-sequence output capability.



(a) (b)

Fig. 1. Circuit diagrams of (a) 3-level 3-leg and (b) 3-level 4-leg FCMIs.

The key feature for a 3-level, 4-leg converter is that the neutral point (point V_N in Fig. 1(b)) is no longer at a nominally fixed potential relative to the DC bus line (N in Fig. 1(a)) and can switch between the three available voltage levels, $-\frac{V_{DC}}{2}$, 0, $\frac{V_{DC}}{2}$ (denoted as 0, 1, 2), in the same way as the three phase legs. Consequently there is no longer a unique *switching state/vector* which realises the desired load voltage. The switching states of the 3-level 4-leg FCMI achieving a desired output voltage vector, say $[V_{AN}\ V_{BN}\ V_{CN}]=\left[\frac{V_{DC}}{2}\ 0\ \frac{V_{DC}}{2}\right]$, are much more numerous than for any other topologies with the same numbers of legs and levels. They are listed in Table I, alongside the equivalent states for the DCMI topology. It can be seen that the 4-leg FCMI has a total of eight different switching states realising the required output voltage vector, while the DCMI which has only two. Likewise the multiplicity of available switching states of a 4-leg FCMI escalates faster with the number of levels than it does for a DCMI, as shown in Table II. This diversity of states of the FCMI introduces a large degree of freedom in converter control, but complicates the modulation procedure as compared with the DCMI circuit.

TABLE I
4-LEG, 3-LEVEL SWITCHING VECTORS

	Swicthing State				Load Voltage		
	V_A	V_B	V_C	V_N	V_{AN}	V_{BN}	V_{CN}
DCMI	1	0	1	0	$V_{DC}/2$	0	$V_{DC}/2$
	2	1	2	1	$V_{DC}/2$	0	$V_{DC}/2$
FCMI	1(a)	0	1(a)	0	$V_{DC}/2$	0	$V_{DC}/2$
	1(a)	0	1(b)	0	$V_{DC}/2$	0	$V_{DC}/2$
	1(b)	0	1(a)	0	$V_{DC}/2$	0	$V_{DC}/2$
	1(b)	0	1(b)	0	$V_{DC}/2$	0	$V_{DC}/2$
	2	1(a)	2	1(a)	$V_{DC}/2$	0	$V_{DC}/2$
	2	1(a)	2	1(b)	$V_{DC}/2$	0	$V_{DC}/2$
	2	1(b)	2	1(a)	$V_{DC}/2$	0	$V_{DC}/2$
	2	1(b)	2	1(b)	$V_{DC}/2$	0	$V_{DC}/2$

TABLE II
4-LEG, N-LEVEL SWITCHING VECTORS

Levels, *n*	Total Switching Vectors for DCMI, N_{SV}	Unique Output Voltage Vectors, N_{VV}	Redundant Switching Vectors, N_R	Total Switching Vectors for FCMI
3	81	65	16	256
4	256	175	81	4096
5	625	369	256	65536
6	1296	671	625	1048576
7	2401	1105	1296	16777216

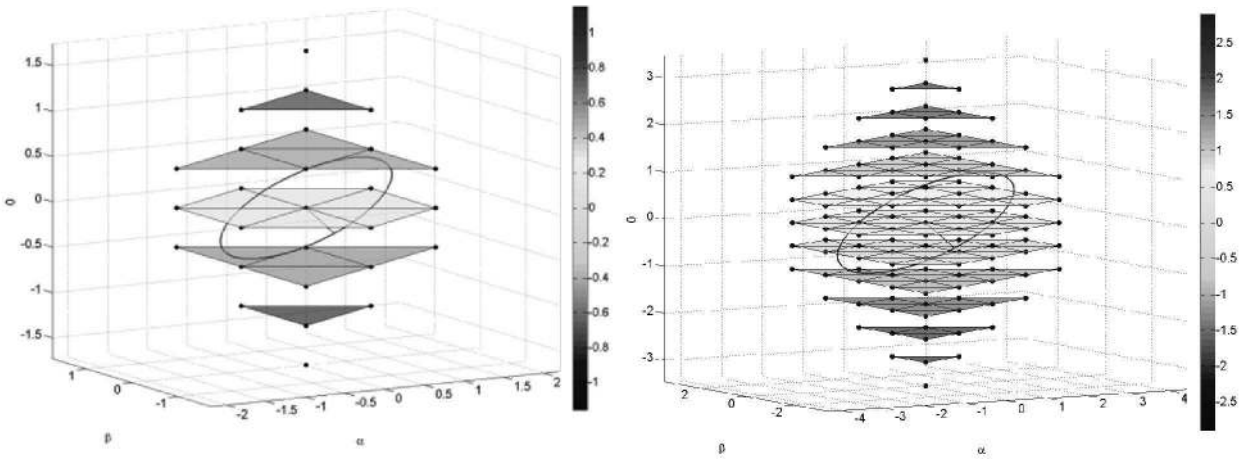
III. DIRECT 3D-PWM SCHEME FOR THREE-PHASE FOUR-LEG FCMI

Control of a 3-phase 4-leg FCMI for unbalanced operation is more intricate due to a large number of switching states overlapping as shown in the previous section. Changes of FCMI terminal voltage due to load variations and unbalance would cause cell and dc-bus capacitor voltages to fluctuate which, in turn, would worsen the terminal voltage performance. 3D-SVM algorithms combined with capacitor voltage balancing are developed and described below.

A. Direct 3D-SVM Scheme

In 3D-SVM the zero component of the output voltage vectors is considered and the switching vectors are in three-dimensional (α-β-0) space, hence a structure is formed encompassing a number of triangular and hexagonal planes. Fig. 2(a) shows the arrangement of the 27 vectors for a 3-level inverter, and Fig. 2(b) illustrates how this structure expands for a 5-level converter. It can be seen that the vectors which 'overlapped' on the α-β plane (viewed along the 0-axis) actually occupy separate levels on the 0-axis; for the 3-level inverter there are 7 discrete levels, whereas for the 5-level converter this increases to 13.

Direct 3D-SVM technique, proposed by Dai *et al.* [7] is claimed to be the most computationally efficient. Using this technique for FCMI the input 3-phase reference voltages V_{AN}*, V_{BN}* and V_{CN}* are combined to form a 3D reference vector, and then normalized according to the number of converter levels, *n*, and the magnitude of the DC-bus voltage, V_{DC}, as



(a) (b)

Fig. 2. 3D vector plots for (a) a 3-level and (b) 5-level converters respectively, with unbalanced reference trajectories.

$$\overline{V}_{REF} = \begin{pmatrix} \mathrm{V_{AN}}^* \\ \mathrm{V_{BN}}^* \\ \mathrm{V_{CN}}^* \end{pmatrix} \text{ and } \overline{v}_{REF} = \overline{V}_{REF}\left(\frac{n-1}{V_{DC}}\right) + \frac{V_{DC}}{2} \tag{1}$$

The resulting normalised vector is then decomposed into two components: an offset vector, v_{OFF}, and a two-level vector, $v_{2\mathrm{L}}$; the former is found by taking the integer part of the normalised reference vector and hence we have

$$\overline{v}_{OFF} = \begin{bmatrix} \mathrm{int}(v_{REFA}) \\ \mathrm{int}(v_{REFB}) \\ \mathrm{int}(v_{REFC}) \end{bmatrix} \text{ and } \overline{v}_{2L} = \overline{v}_{REF} - \overline{v}_{OFF} = \begin{bmatrix} v_{2LA} \\ v_{2LB} \\ v_{2LC} \end{bmatrix} \tag{2}$$

The two-level vector values correspond directly to the PWM duty cycles of the corresponding phase legs, and the offset vector values indicate the normalised levels to switch between.

B. 3D-SVM for 4-Leg FCMI with Closed-Loop Capacitor Voltage Balance

With the fourth leg added, the number of available switching vectors increases greatly for FCMI topology; for example, a 3-level 4-limb FCMI has 256. However, the number of unique output voltage vectors generated by the new configuration only increases to 65, as shown in Table II. Thus, when an output voltage vector is commanded, a wide choice of switching vectors is presented, each with a differing neutral-leg output. Selection is made firstly by

appropriate modulation of the fourth neutral leg output and then the capacitor voltage balance. We define a 'shift' voltage, $v_{SHIFT} = -\frac{v_{MAX} + v_{MIN}}{2}$, as the neutral reference. Note v_{MAX} and v_{MIN} are the maximum and minimum values among the leg reference voltages respectively. v_{SHIFT} is recalculated sample-by-sample and varies with the input reference signals. It is subsequently applied to each of the three phase leg references as well. Consequently, there is no effect on the resultant phase-neutral output voltages as it is cancelled at the neutral point. The technique stems from carrier based implementations of traditional SVM, using a common offset voltage for active vector centralisation and giving improved THD performance [14].

For the criteria of cell capacitor balancing two vector selection schemes may be applied. The first enables natural capacitor voltage balancing [15, 16]. However this scheme is slow and cannot cope with large load variations. The alternative closed loop scheme should be employed which uses the measured intermediate flying capacitor voltages as well as the phase leg currents to select the most suitable switching state to either charge or discharge each capacitor whilst maintaining the required output voltage. The flowchart for the 3D-SVM with closed-loop capacitor voltage control for the FCMI of either the 3-leg or 4-leg configuration is given in Fig. 3. Firstly, the input 3-phase-neutral reference voltages are normalized and decomposed into two-level and offset vectors, before being passed to the vector selection process. For a 3-level FCMI each phase module contains four switching devices; the centre two switches constitute Cell 1, and the outer ones form Cell 2. As the devices within a cell are switched complementarily, two pairs of PWM signals, PWM1x and PWM2x (where x denotes the phase leg), are generated by the control algorithm. The corresponding duty cycles of the PWM signals, D_{1X} and D_{2X} respectively, are determined by considering the value of the offset vector, v_{OFF}. For capacitor voltage balancing in each phase leg of the 3-leg FCMI, the algorithm compares the corresponding flying-capacitor voltage with the nominal $V_{DC}/2$ value to determine whether it requires charging or discharging. The phase load current direction is also observed. If it is positive, i.e. current is flowing out of the leg while the voltage is low, the switching state sequence providing the corrective action is chosen, and conversely, the sequence containing the opposing intermediate state is selected.

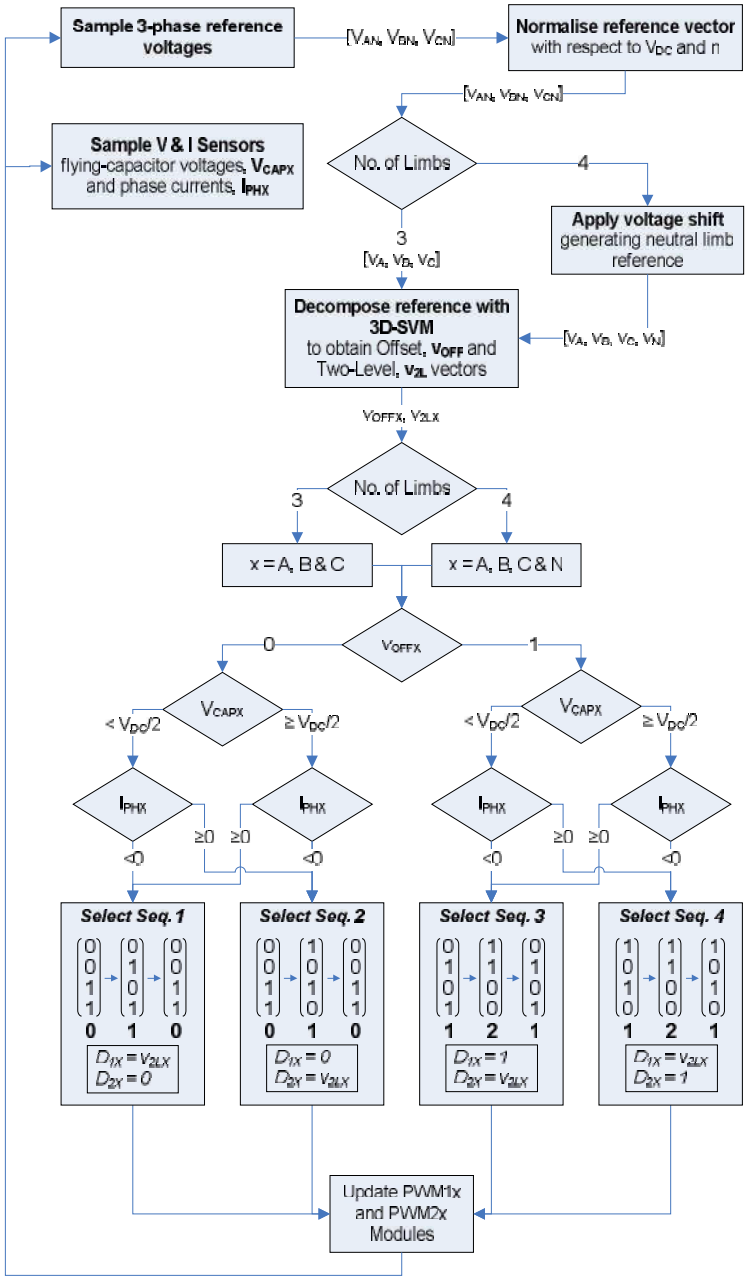


Fig. 3. Flowchart of 3D-SVM for 3-level 4-leg FCMI with closed-loop balancing technique.

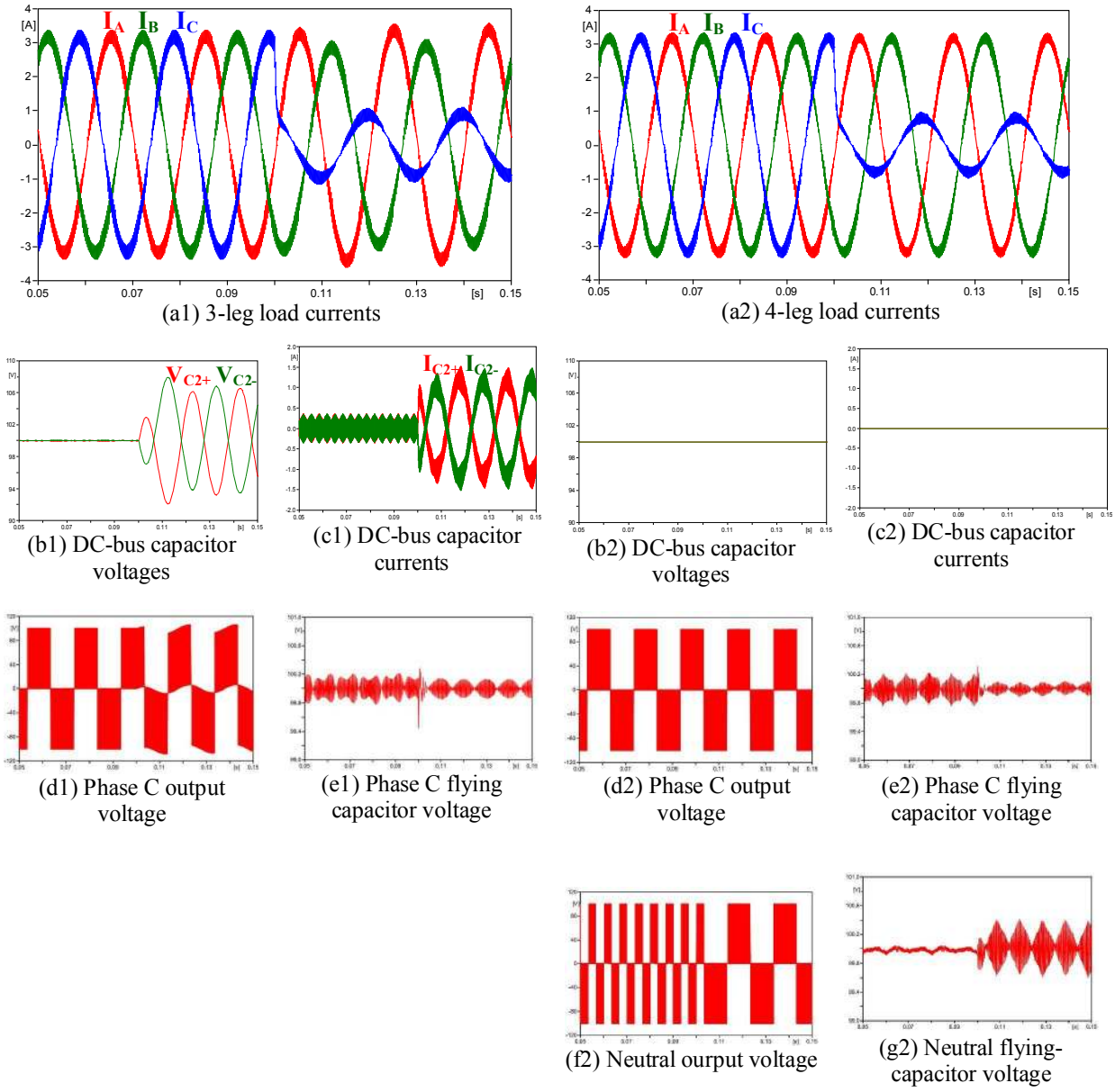
C. Comparison of 3-leg and 4-leg FCMIs

Dynamic performances of 3-leg and 4-leg FCMIs are now compared via computer simulation when controlled by the same 3-D PWM algorithm combined with closed-loop balancing schemes. The DC-bus consists of two series-linked 560 μF capacitors, and is supplied with a constant DC voltage of 200 V; each flying-capacitor has a

capacitance of 560 μF per leg, and a nominal voltage of 100 V. The converter operates at a switching frequency of 5 kHz, and supplies a balanced resistive-inductive load of 25 Ω-8.2 mH per phase.

Initially the reference magnitudes of phases A, B and C are set equally to 80 V_{pk}; after 0.1s, the reference voltage of Phase C is suddenly decreased to 20 V_{pk}. The modulation index change is reflected in the load current waveforms for both topologies (Figs. 4 (a1) and (a2)). As expected, the reduction in Phase C reference causes the current in this phase to reduce accordingly; this action creates a subsequent imbalance between the three phases and the neutral line current increases as a result. Observing the load current magnitude in the 4-leg case (Fig. 4 (a2)) after the imposed imbalance at 0.1s, Phases A and B remain unchanged, and Phase C reduces proportionally with the commanded reference. However, in the 3-leg case (Fig. 4 (a1)) all three phase currents undergo a change in magnitude, inconsistent with the reference. This can be attributed to fluctuation of the converter neutral point owing to the flow of current through the DC-bus capacitors under the unbalanced condition.

The voltages across the two series-linked DC-bus capacitors are shown for both topologies, in Figs. 4(b1) and (b2). As expected, there is no visible voltage fluctuation with the 4-leg topology, but for the 3-leg case the neutral current is forced to flow into the DC-bus mid-point. Consequently, the DC-bus voltage exhibits fluctuation (up to 8%) at the fundamental frequency. The adverse effect of this on the phase output voltages are shown in Figs. 4(d1) and (d2), and this explains the irregularities previously observed in the current waveforms in the 3-leg case. Using the closed-voltage balancing scheme, flying capacitor voltages are well balanced in both topologies as shown in Figs. 4(e1) and (e2), and ripple amplitude in the 4-leg case is much smaller than its 3-leg counterpart. These results have shown the superior performance of the four-leg topology in keeping the DC voltage stable; hence much smaller capacitors can be used in this circuit.



(a1) 3-leg load currents

(a2) 4-leg load currents

(b1) DC-bus capacitor voltages

(c1) DC-bus capacitor currents

(b2) DC-bus capacitor voltages

(c2) DC-bus capacitor currents

(d1) Phase C output voltage

(e1) Phase C flying capacitor voltage

(d2) Phase C output voltage

(e2) Phase C flying capacitor voltage

(f2) Neutral ourput voltage

(g2) Neutral flying-capacitor voltage

Fig. 4: Simulated voltage and current waveforms for unbalanced 3-phase reference voltage under closed-loop capacitor balancing (a1)-(e1) waveforms for 3-leg FCMI. (a2)-(g2) waveforms for 4-leg FCMI

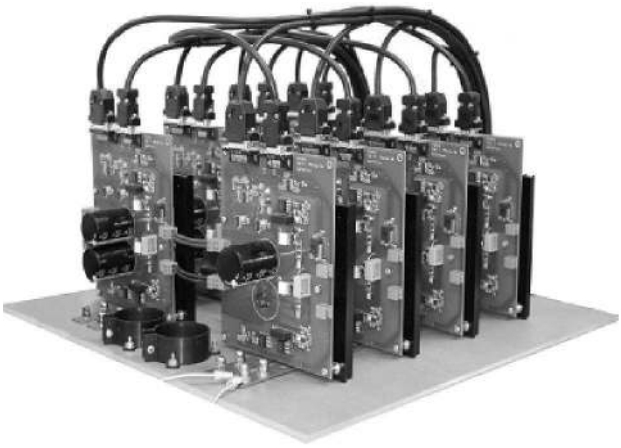
IV. A PRACTICAL FOUR-LEG FCMI-based ACTIVE POWER FILTER

A practical active power filter using the above 3-level-4-leg FCMI and Direct-3D PWM scheme was constructed to test for effective harmonic elimination under unbalanced load conditions.

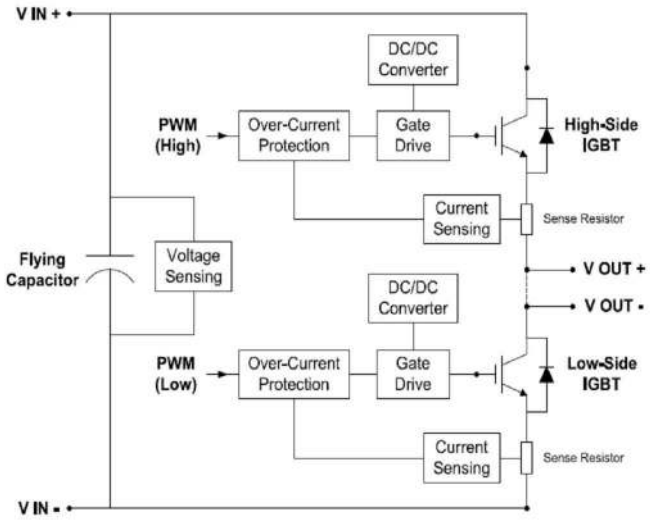
A. The 3-phase 4-leg 10 kVA FCMI

The 4-leg FCMI circuit diagram is as shown in Fig. 1(b), the experimental test rig is shown in Fig. 5(a) and specifications are listed in Tables III – V in the Appendix. This is a compact modular construction, consisting of eight identical cell modules with circuit schematics as shown in Fig. 5(b), each containing: two complementary Infineon 600 V / 30 A IGBT switches with anti-parallel fast recovery diode in a TO-247 package, optically-isolated gate drivers, a 400 V, 560 μF flying capacitor, and on-board measurement and device fault protection circuitry. Two such cell modules are connected together to form a 3-level phase leg, and then to a common DC-bus, across which is a total capacitance of 1.5 mF. All capacitance values are selected from simulation studies to give ripple voltage levels below 5% at steady state [17]. The DC-bus contains two identical capacitors connected in series to form a central neutral-point for 3-leg operation, and is supplied by a variable DC Switch-Mode Power Supply. PWM signals are generated using a Texas Instruments TMS320F2812 DSP switching at 5 kHz. Testing uses a Y-connected balanced resistive load of 25 Ω/phase is connected through 8.2mH filter inductors for current smoothing. The 'star' point of the load is connected back to the neutral-leg of the converter.

Waveforms from the experimental 3-phase-4-leg FCMIs are shown in Fig. 6. The converter was modulated using the closed-loop-balanced 3D-PWM algorithm, with predefined imbalanced reference voltage set as 50 Hz sinusoid, having amplitudes of 90, 80 and 70 V across phases A, B and C respectively; they are displaced by 120^{o} from each other as shown in Fig. 6(a). Figs. 6(b) and (c) show the unbalanced load current waveforms and line-line output voltage.

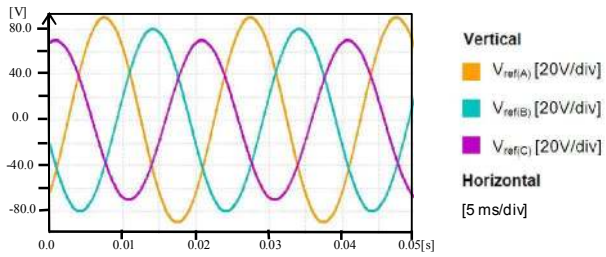


a) Photograph of the FCMI experimental setup

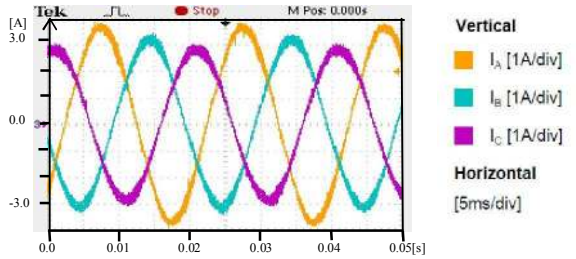


b) Schematic of FCMI module circuit

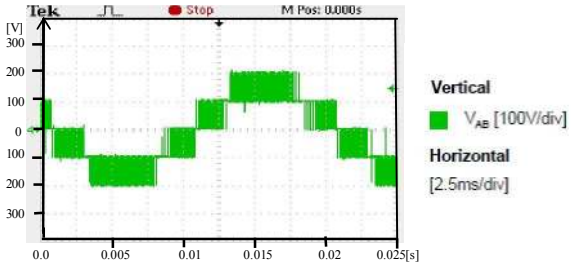
Fig. 5. 3-phase 4-leg FCMI experimental set



(a) Imbalanced three phase reference voltage (V_{ref})



(b) Load currents



(c) Line-line output voltage (V_{AB})

Fig. 6. Experimental 3-phase 4-leg FCMI waveforms

B. Harmonic Elimination Control Scheme

This 4-leg FCMI can also be used as a shunt-connected APF for eliminating harmonic components and unbalanced load current on a distribution network. The system block diagram is shown in Fig. 7(a). The most important elements are software for harmonic and unbalanced current extraction and current control algorithms, which are implemented using the DSP device for 3D-PWM and are described below.

The algorithm must ensure harmonic, zero and negative sequence current components are extracted from the load current. The distinct characteristics exhibited by fundamental and harmonic frequencies in the rotating frame

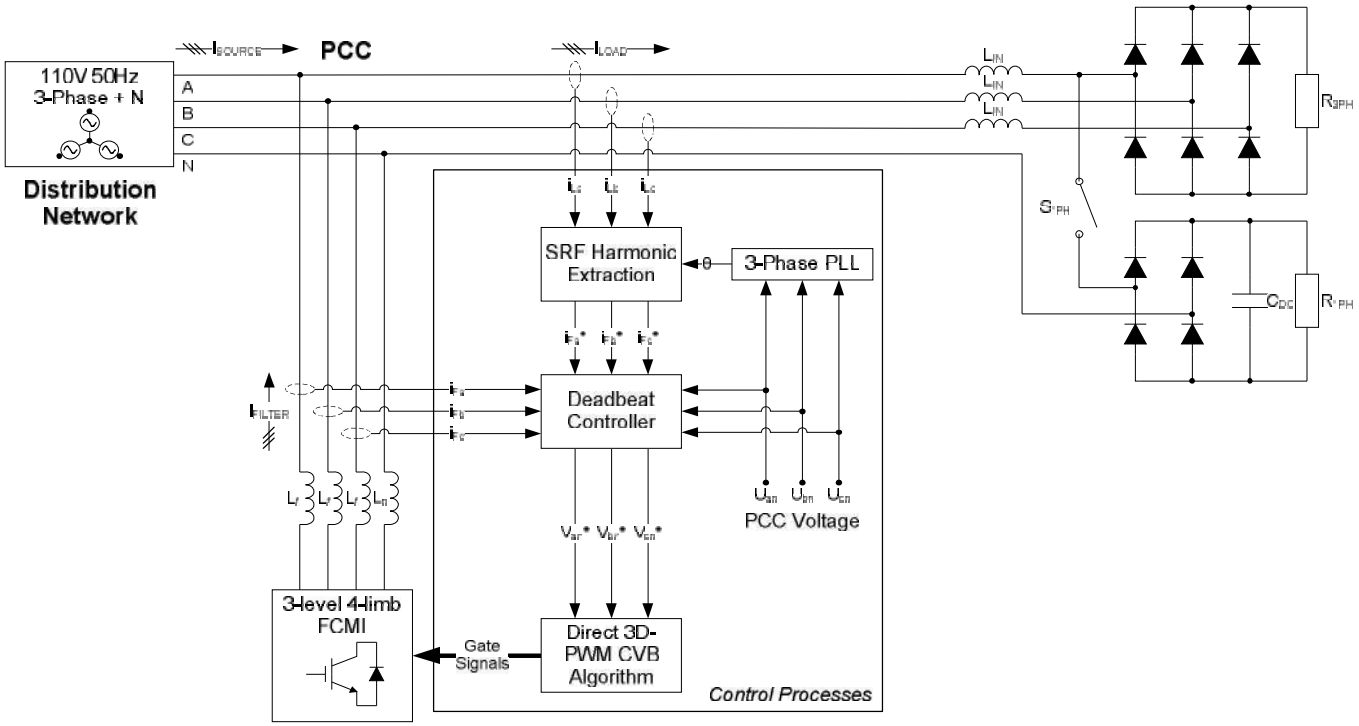


Fig. 7. Block diagrams for: (a) APF controlled system and harmonic and unbalanced current elimination Scheme. (b) Scheme for extraction of harmonic, negative and zero sequence current components

are exploited by the well-known Synchronous Reference Frame (SRF) harmonic extraction technique [18, 19]. This method is extended to unbalanced 4-wire systems where zero-sequence harmonics exist. The phase locking scheme based on the in-quadrature signal generation principle [20] is still applicable for tracking the grid voltage vector, but both Clarke and Park transforms must now consider the zero-component corresponding to the neutral-line current in an unbalanced 4-wire system. It contains a fundamental part arising from general load imbalance, together with zero-sequence harmonics drawn by non-linear loads; since the zero-axis forms the point about which the synchronous frame rotates, frequencies present in the zero-component are unaffected by the transformation. Consequently if the zero-component is forced to 0, compensation of fundamental imbalance may be achieved in addition to compensation of harmonics. The block diagram of such a harmonic extraction scheme is presented in Fig. 7(b). Detailed explanations are given elsewhere [17]. The extracted harmonic currents form the reference vector for APF.

For current control, previous published work on APF uses mainly conventional PID control schemes [21]. Here the well-known deadbeat control scheme is used as it has benefits of fast dynamic response and high computational efficiency. In this application the algorithm samples the filter output current and calculates the required voltage control value using the extracted harmonic current as the reference and the model of the system which is a three-phase low-pass filter between the PCC and the AC terminals of FCMI. Assuming the PCC voltage of constant magnitude and frequency, the FCMI AC-side voltage vector at the next sample can be calculated as

$$\vec{v}_f(k+1) = \vec{e}(k) + \vec{i}_f^{\,*}(k)\frac{L_f}{T_s} + \vec{i}_f(k)\left[R_f - \frac{L_f}{T_S}\right] \tag{3}$$

where $\vec{e}(k)$ denotes the PCC voltage vector, $\vec{i}_f^{\,*}(k)$ denotes the reference current vector at the current sample time extracted by the scheme in Fig. 7(b), R_f and L_f are filter parameters. This algorithm works well for tracking constant or slowly varying reference variables. However in this application, the extracted harmonic reference current varies continuously and often rapidly from one sample to the next due to load variations. Thus, the reference current applied for control voltage calculation at the current sample interval may differ significantly from its actual value at the next sample. This mismatching causes errors in harmonic current cancellation and was discussed in some previous publications [21, 22]. This problem can only be tackled by taking into account the rate of change of the

reference current. In ref [21], a conventional PID controller is used for a current source-based APF; the addition of the derivative term overcomes the delay in reference current calculation. In [22], two additional terms are added to the voltage signal calculation, i.e. reference current error at the present sample and that at the last sample. This makes the algorithm complicated and it is difficult to select the two scaling factors for these terms. In this work only the rate-of-change of the reference current at the current sample instant is calculated and the result added to the original reference value, thus the new reference current vector for the deadbeat controller is given as

$$\vec{i}_f^{\,*\prime}(k) = \vec{i}_f^{\,*}(k) + \tau_c \frac{\vec{i}_f^{\,*}(k) - \vec{i}_f^{\,*}(k-1)}{T_S} \tag{4}$$

where τ_c denotes the scaling factor which must be carefully tuned. Thus the modified formula for calculating FCMI voltage vector at the next sample instant is changed to

$$\vec{v}_f(k+1) = \vec{e}(k) + \vec{i}_f^{\,*}(k)\left[\frac{L_f}{T_s} + \frac{L_f\tau_c}{T_s^2}\right] - \vec{i}_f^{\,*}(k-1)\left[\frac{L_f\tau_c}{T_s^2}\right] + \vec{i}_f(k)[R_f - \frac{L_f}{T_s}] \tag{5}$$

The voltage vector obtained at every sample is used as the modulating signal for the 3D-PWM scheme described in Section III. The flowchart of the software for the harmonic extraction and control schemes, together with the direct 3D PWM algorithm and capacitor voltage balancing, is as shown in Fig. 8 and the total execution time per sample is recorded as 43μs.

C. Experimental Test

The experimental test of FCMI active power filter (APF) was performed using a hardware load which emulates features of an unbalanced network with harmonics. It consists of a three-phase full-bridge rectifier and a switchable single–phase one, with DC-side resistance loads of 10 Ω and 25 Ω respectively. The experimental setup is illustrated in Fig. 7, where the APF output terminals are connected to the three-phase network common coupling point (PCC) via a set of filter inductors. The three-phase unbalanced and distorted load currents measured at the PCC are shown in Fig. 9(a). The injected APF injected compensating current and the resultant current seen from the source-side of the PCC for all three phases are shown in Figs. 9(b) and 9(c). The source currents are clearly shown

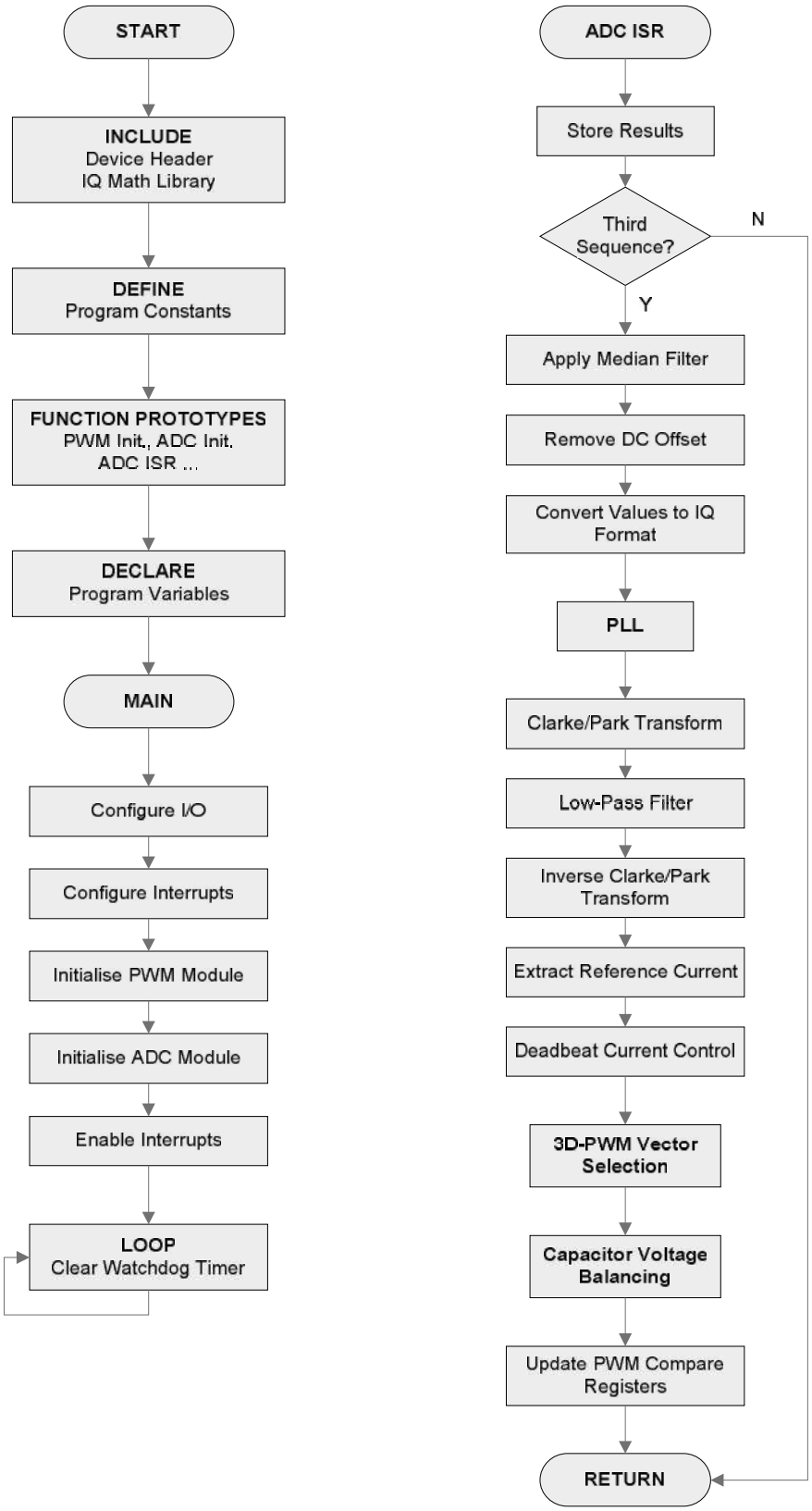


Fig. 8 Flow chart for implementing the harmonic extraction and control schemes with the proposed direct 3D PWM algorithm

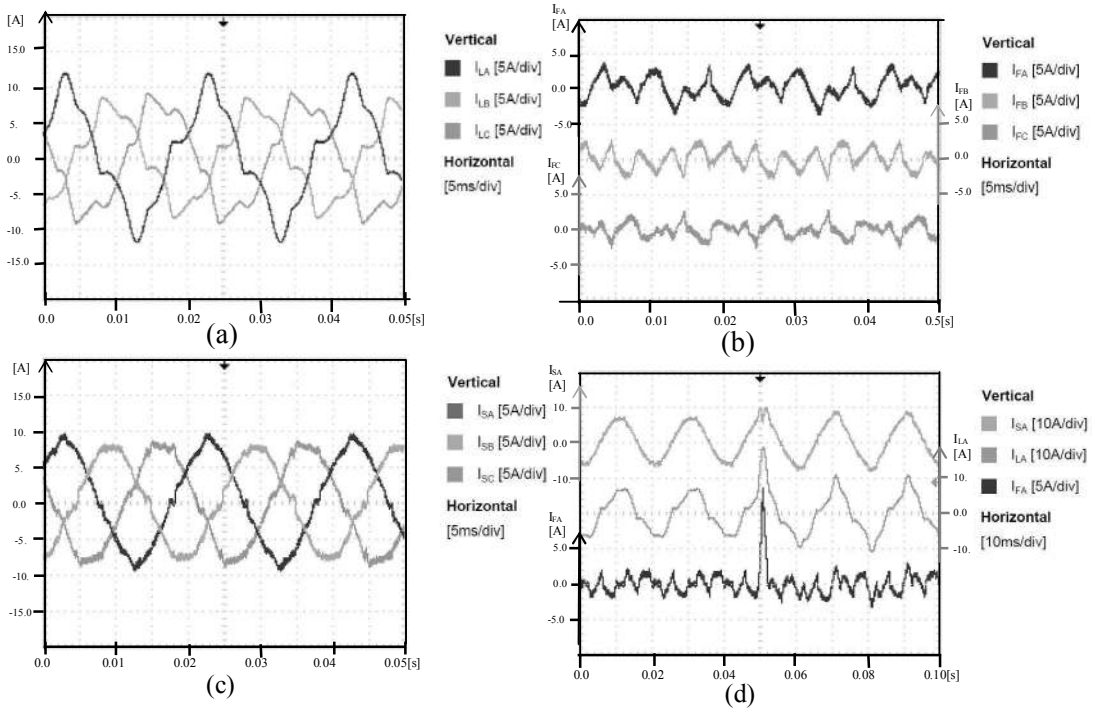
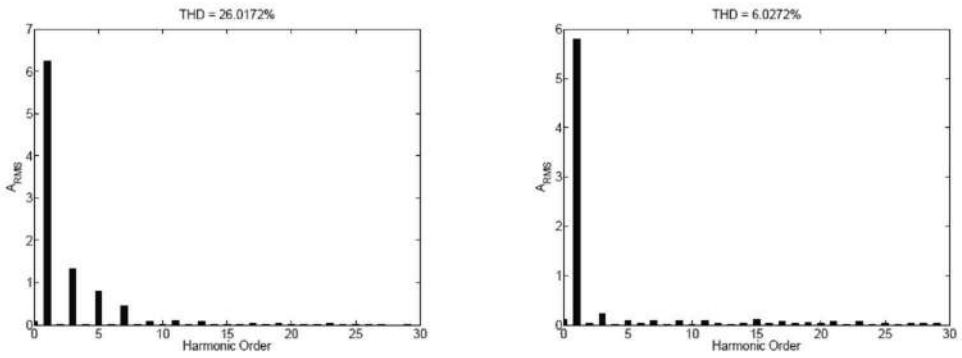


Fig. 9. Experimental results: (a) uncompensated unbalanced 3-phase load current waveforms, (b) APF generated compensating currents (c) compensated 3-phase source currents, (d) APF control of phase A current after a transient load current change.

being adequately compensated by the APF, both in terms of harmonic distortion and unbalance, when compared with the original measured harmonic load current (Fig. 9(a)); after compensation they are near-sinusoidal. Fig. 9(d) shows the excellent transient response due to the modified deadbeat control scheme when the single phase nonlinear load is suddenly switched in representing an abrupt change of the harmonic conditions. A large transient increase in load current is observed, attributable to the initial charging of the output capacitor C_{DC} (across load R_{1PH} in Fig. 7). The APF responds promptly by injecting a large compensating current pulse into the PCC; consequently, the disturbance imposed on the source current is minimal, demonstrating a good dynamic performance of the proposed APF control scheme. Fig. 10 compares the frequency spectra of the phase A uncompensated load current with the compensated source current showing clear suppression across all harmonic frequencies. The Total Harmonic Distortion (THD) factor is reduced from 26% without compensation to about 6% after the compensation. This result is comparable with that reported in ref [21] which achieved a THD of around 5% using a 2-level 3-leg current source-based active power filter, but the latter is only for harmonic elimination under balanced load condition.



(a) (b)

Fig. 10. Frequency spectra for (a) Unbalanced phase A load current and (b) Compensated balance Phase A grid current

V. CONCLUSIONS

As a new application of the flying capacitor multi-level inverter, a three-phase, four-leg FCMI was proposed as an active power filter in four-wire unbalanced power distribution systems. It was found that a four-leg FCMI gives increased switching state redundancies but for unbalanced load operation it can maintain DC-bus voltage balance significantly better than its 3-leg counterpart. This leads to superior performance in three-phase voltage control. A new 3-D PWM switch state selection algorithm specific to the FCMI topology has been developed and two different flying capacitor voltage balancing schemes were compared. Capacitor values can be much reduced in this new form of active power filter.

A new deadbeat current control scheme was also demonstrated, where the notable feature is inclusion of the derivative of the reference current to compensate reference current delay. The complete control strategy provides compensation of positive, negative and zero-sequence harmonic currents as well as the fundamental phase load imbalance. The combination of this control algorithm with the 3D-PWM modulation technique was demonstrated successfully using a fully-rated hardware prototype of the active power filter, and gave excellent results in both steady and transient operations.

APPENDIX

Active Power Filter Hardware Data

TABLE III
SPECIFICATIONS OF IGBTS

Parameter	Value
Maximum collector-emitter voltage, V_{CE}	200 V
Maximum DC collector current, I_C	30 A
Short-circuit collector current, $I_{C(SC)}$	275 A
Short-circuit withstand time, t_{SC}	5 µs
Collector-emitter saturation voltage, $V_{CE(Sat.)}$	1.5-1.9 V
Gate-emitter threshold voltage, $V_{GE(Th.)}$	4.1-5.7 V
Total turn-on time, t_{on}	44-50 ns
Total turn-off time, t_{off}	300-382 ns

TABLE IV
SPECIFICATIONS OF FCMI CAPACITORS

Parameter	Value
Capacitance	560 µF ± 20 %
Maximum working voltage	400 VDC
Maximum surge voltage	450 VDC
Maximum RMS ripple current (120Hz)	5.52A
Maximum RMS ripple current (10kHz)	7.90A
Lifetime	3000h

TABLE V
TEST SETUP PARAMETERS

Parameter	Value
V_{DC}	200 V
C_1	560µF
C_1	3000µF
L_F	1mH
V_{DC}	0.1mH

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