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Three-Phase PLL for Grid-Connected Power Converters under Both Amplitude and Phase Unbalanced Conditions

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Abstract: **This paper proposes a technique for accurate phase estimation of distorted three-phase grid voltages including unbalanced amplitudes and/or phase angles. An adaptive cascaded delayed signal cancellation (CDSC) strategy is used for the generation of the amplitude balanced three-phase voltages. The CDSC strategy also eliminates both odd and even harmonics from the input voltage. An algorithm is also reported for removing the phase angle deviations from the three-phase voltages including unbalanced phase angles. Finally, a phase-locked loop (PLL) is applied to estimate the phase angle of the reference phase voltage. It requires only one PLL to estimate three phase angles of the thee-phase voltages, respectively, suffering from the unbalanced amplitudes and phase angles. It is also immune to harmonic distortions at changeable frequency environment. When compared to the CDSC-PLL and *dq*CDSC-PLL techniques reported in the technical literature, it can provide improved phase estimation under amplitude and phase unbalanced condition. Simulated and experimental results of the technique are acquired from the MATLAB/Simulink and dSPACE1104 control board platform, respectively, for a number of case studies observed in the grid voltage.**

Keywords: **Harmonics, phase angle estimation, phase-locked loop (PLL), synchronization, and three-phase voltage.**

I. Introduction

Distributed generation system requires power converter for the operation of the grid-connected mode [1]. For the pulse-width modulation process of the power converter, the controller uses instantaneous phase angle of the grid voltage to produce synchronized reference signal. The phase angle estimation technique used for this purpose should be immune to harmonics, DC offset, frequency variations and voltage unbalances like amplitude and/or phase angle deviations [2].

Phase-locked loop (PLL) is extensively used phase estimation technique for synchronization of the grid connected power converters [2-11]. In order to achieve better performances in adverse conditions, the PLL either incorporate in-loop filter or use pre-filter, or combine both [3-5]. Among various types of three-phase PLLs [6], synchronous reference frame (SRF)-PLL [7] is mostly used to calculate the phase angle of a three-phase voltage system for their simplicity and robustness. However, the SRF-PLL can only calculate the phase angle of the three-phase system accurately at high speed if the system is balanced and purely sinusoidal [8]. Otherwise, it suffers from severe distortion caused by the presence of harmonics or any type of amplitude or phase angle imbalances [9]. Several researches have been carried out for improving the performance of the SRF-PLL under unbalanced amplitudes and harmonics [10-12].

A second-order generalized integrator based PLL has been reported in [13]. But the technique is suitable only for single phase systems. Enhanced three phase PLLs based on adaptive filtering are presented in [14]. In [15], an improved version of moving average filter based PLL is introduced. This technique is well suited when the voltages have amplitude imbalances along with equal phase jump of all the phases. The adaptive-lattice SRF-PLL technique, as reported in [16], can greatly compensate for harmonic distortion. Another pre-filter based algorithm, standard complex-coefficient filter based PLL, has also been found useful in harmonic condition [4].

A signal reforming algorithm based SRF-PLL has been presented in [9]. However, it is only appropriate for amplitude imbalance condition. A double synchronous reference frame PLL (DSRF-PLL) and a decoupled-DSRF-PLL have been presented in [17]. The delayed signal cancellation (DSC) strategy based PLLs can efficiently eliminate the negative sequence components and the harmonic components without any significant phase error [18-22]. These advanced methods have filtering stages within or before the control loop of the PLL [23-26]. Although, they exhibit excellent performances, these algorithms may not be able to provide accurate phase estimation when the phase angles are not balanced.

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Adaptive low-pass notch filter based PLLs have been introduced in [27]. However, these techniques do not consider the case of phase angle imbalances of the three-phase voltages. Also, these have been developed assuming that the frequency of the system is known and constant. Hence, the filter parameters are to be changed according to the altered frequency for accurate estimation.

The three-phase PLL algorithms reported in the technical literature are designed for improving the performance or reducing the complexity of the technique under unbalanced amplitude condition and distortions including harmonics and DC offset. It can be seen from the power system analysis [28] that not only the amplitude but also the phase angle imbalances occur in the grid voltages under the unbalanced loading and/or fault conditions. In these conditions, the response of the existing three-phase PLL algorithms will be affected; consequently, the performance of the grid-connected power converter will be degraded. Therefore, a suitable three-phase PLL algorithm is required so that it can provide accurate phase estimation under both the amplitude and phase unbalanced condition including harmonic distortion and DC offset.

The objective of this paper is to report a technique based on three-phase PLL for accurate phase estimation of the three-phase voltages under simultaneous amplitude and phase angle imbalances along with harmonic distortion and DC offset. The proposed algorithm contains the followings: i) cascaded DSC (CDSC) approach for balancing the amplitudes and rejecting the harmonics and DC offset, ii) an algorithm for removing the imbalanced phase angles, and iii) a three-phase SRF-PLL for estimating the phase angle. It requires only one PLL to generate accurate phase angles of the three phase voltages under amplitude and/or phase unbalanced conditions. It is also able to remove the error created by the DC offset, odd and even harmonics. When compared to the CDSC-PLL [18] and *dq*CDSC-PLL [22], it can provide improved phase estimation under amplitude and phase unbalanced condition. Both simulation and experimental results are documented for verifying the usefulness of the technique.

The remaining paper is organized as follows – Section II introduces developing procedures of the proposed technique. Section III documents the simulation results carried out in MATLAB/Simulink for several case studies. Experimental results in dSPACE control board platform are reported in Section IV. Section V concludes the paper.

II. Proposed Phase Estimation Technique

The proposed phase estimation technique relying on a SRF-PLL for three-phase voltage system is shown in Fig. 1. The symbols used in Fig. 1 are defined as follows: v_a, v_b and v_c are the three-phase voltages of phases 'a', 'b' and 'c', respectively, $v_{a'}$, $v_{b'}$ and $v_{c'}$ are the amplitude normalized fundamental voltages of phases 'a', 'b' and 'c', respectively, $v_{a''}$, $v_{b''}$ and $v_{c''}$ are both the amplitude and phase angle balanced fundamental voltages of phases 'a', 'b' and 'c', respectively, $\Delta\theta_b$ and $\Delta\theta_c$ are the phase angle deviations of the voltages v_b and v_c, respectively, from 120° with respect to the reference voltage v_a, f is the estimated fundamental frequency, f' is the low-pass filtered estimated fundamental frequency, and ϕ_a, ϕ_b and ϕ_c are the estimated fundamental instantaneous phase angles of the voltages v_a, v_b and v_c , respectively.

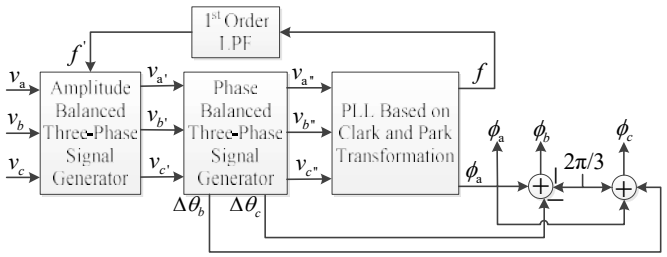

Fig. 1: Proposed phase estimation technique from the distorted three-phase voltages including amplitude and/or phase angle imbalances.

In the proposed technique, a frequency adaptive amplitude balanced three-phase signal generator (ABSG) is used. The main function of the ABSG is to normalize the voltages of each phase by using their respective fundamental amplitude. This normalization process helps to remove the amplitude unbalanced condition. The ABSG also eliminates the voltage distortions caused by the DC offset and harmonics. The amplitude normalized three-phase voltages are then forwarded to a phase balanced three-phase signal generator (PBSG). The PBSG has also two functions. The first function is to track the amount of phase imbalance exists among the three phase voltages. The second one is to generate the phase balanced three-phase voltages by removing the imbalanced phase angles. The output voltages of the PBSG have unity amplitude and 120° angular displacement between the adjacent two phases. The generated balanced voltages are fed to a PLL relying on the Clarke and Park transformation for tracking the instantaneous phase angle (ϕ_a) of the reference phase voltage, v_a. The estimated phase angle of the reference phase voltage and the deviation of the phase angles of other two phase voltages are then processed to get the actual phase angles (ϕ_b and ϕ_c) of other two phase voltages. The fundamental frequency generated by the PLL is also fed back to the ABSG for adaptive elimination of the harmonics and adaptive amplitude normalization of the phase voltages. A first-order low-pass filter (LPF) is used in the feedback path of the frequency in-order to provide sufficient delay for stability purposes [18]. In this case, the time constant of the LPF should be equal or greater than the time constant of the forward path. The following subsections describe the detail functions of each block shown in Fig. 1.

A. Amplitude Balanced Three-Phase Signal Generator (ABSG)

The sampled three-phase grid voltages with a sampling index and time interval of n and T_s, respectively, can be expressed as follows:

$$\left.\begin{aligned} v_a(n) &= A_a \sin(\omega n T_s) + \text{DC Offset} + \text{Harmonics} \\ v_b(n) &= A_b \sin(\omega n T_s - 2\pi/3 - \Delta\theta_b) + \text{DC Offset} + \text{Harmonics} \\ v_c(n) &= A_c \sin(\omega n T_s + 2\pi/3 + \Delta\theta_c) + \text{DC Offset} + \text{Harmonics} \end{aligned}\right\} \quad (1)$$

where A_a, A_b and A_c are the fundamental voltage amplitudes of the phases 'a', 'b' and 'c', respectively, and $\omega=2\pi f$ is the fundamental angular frequency. The instantaneous phase angles of the voltages v_a, v_b and v_c are $\phi_a=\omega n T_s$, $\phi_b=\omega n T_s-2\pi/3-\Delta\theta_b$ and $\phi_c=\omega n T_s+2\pi/3+\Delta\theta_c$, respectively. Both odd and even harmonics can be present due to the nonlinear loads connected to the grid. On the other hand, saturation in current transformer, grid faults or analog-to-digital conversion process can inject DC offset.

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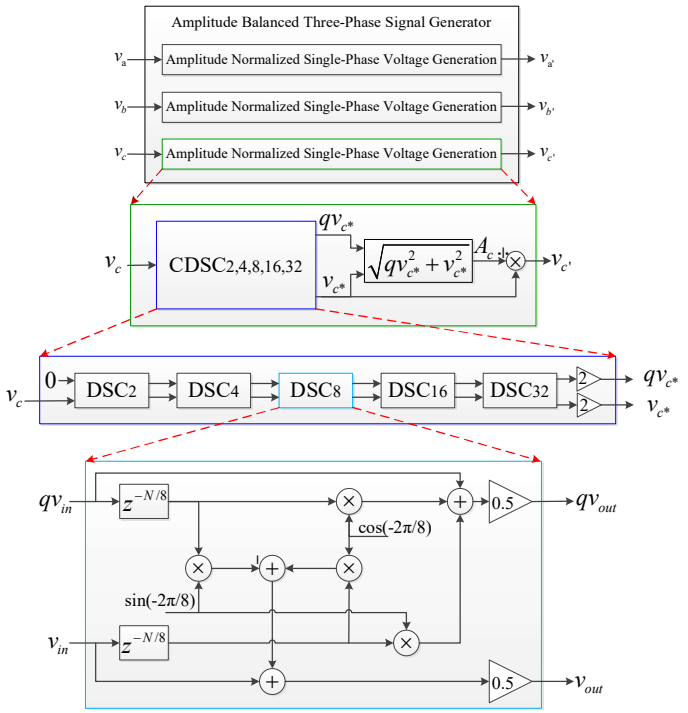

Fig. 2: Block diagram representation of the ABSG for generating the amplitude balanced three-phase voltages.

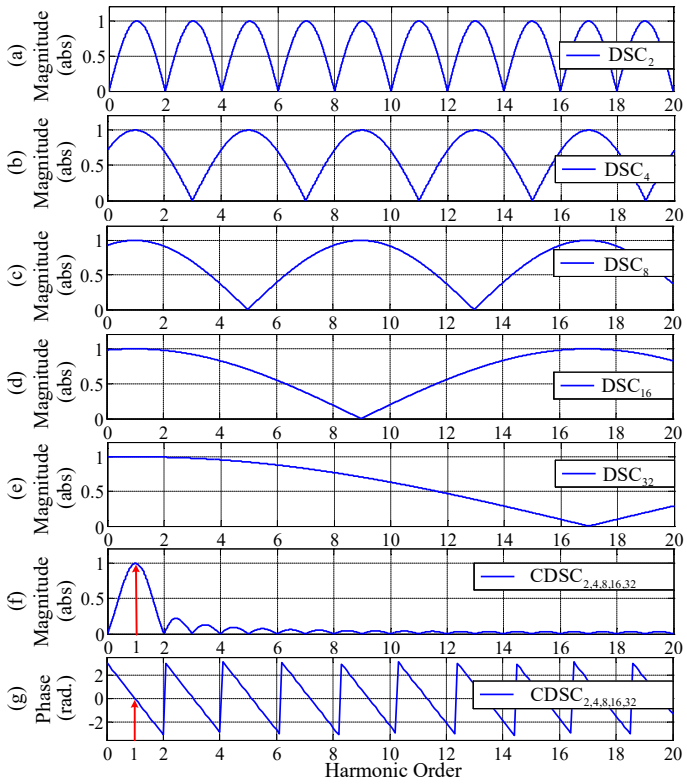

Fig. 3: Frequency response of the DSC_2, DSC_4, DSC_8, DSC_{16}, DSC_{32} and $CDSC_{2,4,8,16,32}$ operators.

The block diagram representation of the ABSG for generating the amplitude balanced three-phase voltages is shown in Fig. 2. As it can be observed, the amplitude normalization of each phase voltage is obtained separately. So, three same operations are performed for the three phase voltages separately. The generation of the orthogonal voltages including the rejection of DC offset and harmonics from each phase voltage is the first step of the ABSG. The fundamental voltage amplitude, which is used to normalize the in-phase voltage component, is then obtained from the generated orthogonal voltages. The DSC strategy is used to achieve the above objectives. Several DSC operators are cascaded in series to remove the DC offset and all the harmonics from the input voltages. The CDSC operator has two orthogonal inputs and two orthogonal outputs. However, according to the anti-conjugate decomposition process, the CDSC operator can still produce orthogonal voltages at its output for single-phase voltage system when zero and single-phase voltage are used as the inputs [29]. The block diagram representation of the CDSC operator is shown in Fig. 2, where $CDSC_{2,4,8,16,32}$ is formed by cascading DSC_2, DSC_4, DSC_8, DSC_{16} and DSC_{32}. The subscripts 2, 4, 8, 16 and 32 of DSC_2, DSC_4, DSC_8, DSC_{16} and DSC_{32} indicate that the input voltages are delayed by $N/2$, $N/4$, $N/8$, $N/16$ and $N/32$ samples, respectively, where N is the number of voltage samples in one fundamental period. Fig. 3 illustrates the magnitude responses of DSC_2, DSC_4, DSC_8, DSC_{16}, DSC_{32} and $CDSC_{2,4,8,16,32}$. Harmonic order up to 20 is shown in Fig. 3. As it can be seen, DSC_2 can eliminate all even harmonics (2, 4, 6, …, 20) including DC offset. It can also be noticed that DSC_4 and DSC_8 can remove the following harmonics order (3, 7, 11, 15 and 19) and (5 and 13) respectively. On the other hand, DSC_{16} and DSC_{32} can reject 9th and 17th harmonics, respectively. Therefore, by cascading DSC_2, DSC_4, DSC_8, DSC_{16} and DSC_{32}, all the lower order odd and even harmonics up to 20 including the DC offset can be eliminated from the input voltage, as can also be noticed from the magnitude response of $CDSC_{2,4,8,16,32}$ shown in Fig. 3(f). Both positive and negative sequence harmonics can be eliminated from the input voltages by using the $CDSC_{2,4,8,16,32}$ operator, as documented in [29]. From the harmonic specifications in the IEC standard 61000-4-13 [30], it is observed that the lower order harmonics are dominant. For this reason, DSC_2, DSC_4, DSC_8, DSC_{16} and DSC_{32} blocks are used in the proposed technique for rejecting lower order harmonics including the DC offset. On the other hand, it can be seen from the phase response shown in Fig. 3(g) that the $CDSC_{2,4,8,16,32}$ operator does not introduce any phase error at the tuned fundamental frequency.

The implementation of the DSC_8 operator is also shown in Fig. 2. Similarly, other operators (DSC_2, DSC_4, DSC_{16} and DSC_{32}) can be implemented by using their respective subscript in the place of 8 in the terms $z^{-N/8}$, $\sin(-2\pi/8)$ and $\cos(-2\pi/8)$ used in DSC_8. The value of $N/8$ in DSC_8 can be integer or non-integer. For the non-integer value of $N/8$, an interpolation operation can be used between the adjacent voltage samples to get the value of the voltage at the delay of $z^{-N/8}$. Same procedure can be followed for other DSC operators if their respective numbers of delayed samples are non-integer. This process helps to reduce the error caused by the rounding or ceiling function of the non-integer value of the number of delayed samples. A relatively simple linear interpolation operation is used in the proposed technique. The outputs of three separate $CDSC_{2,4,8,16,32}$ operators used for three-phase voltages can be expressed by (2), (3), and (4), respectively.

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$$\left.\begin{aligned} v_{a*}(n) &= A_a \sin(\omega n T_s) \\ q v_{a*}(n) &= A_a \cos(\omega n T_s) \end{aligned}\right\} \quad (2)$$

$$\left.\begin{aligned} v_{b*}(n) &= A_b \sin(\omega n T_s - 2\pi/3 - \Delta\theta_b) \\ q v_{b*}(n) &= A_b \cos(\omega n T_s - 2\pi/3 - \Delta\theta_b) \end{aligned}\right\} \quad (3)$$

$$\left.\begin{aligned} v_{c*}(n) &= A_c \sin(\omega n T_s + 2\pi/3 + \Delta\theta_c) \\ q v_{c*}(n) &= A_c \cos(\omega n T_s + 2\pi/3 + \Delta\theta_c) \end{aligned}\right\} \quad (4)$$

Therefore, the fundamental voltage amplitudes of the three-phase voltages can be acquired by

$$\left.\begin{aligned} A_a &= \sqrt{v_{a*}^2(n) + q v_{a*}^2(n)} \\ A_b &= \sqrt{v_{b*}^2(n) + q v_{b*}^2(n)} \\ A_c &= \sqrt{v_{c*}^2(n) + q v_{c*}^2(n)} \end{aligned}\right\} \quad (5)$$

The above estimated amplitudes can now be used to normalize the estimated in-phase voltage component so that the amplitude balanced three-phase voltages are attained. The amplitude balanced three-phase voltages can be achieved by

$$\left.\begin{aligned} v_{a'}(n) &= v_{a*}(n)/A_a = \sin(\omega n T_s) \\ v_{b'}(n) &= v_{b*}(n)/A_b = \sin(\omega n T_s - 2\pi/3 - \Delta\theta_b) \\ v_{c'}(n) &= v_{c*}(n)/A_c = \sin(\omega n T_s + 2\pi/3 + \Delta\theta_c) \end{aligned}\right\} \quad (6)$$

B. Phase Balanced Three-Phase Signal Generator (PBSG)

The phase balanced three-phase voltages are produced in two steps. The first step is to extract the amount of phase imbalance exists between two adjacent phases. In the second step, the extracted imbalanced phase angle is removed from the voltages to make them balanced. In our proposed technique, the phase voltage v_a is chosen as the reference phase. So, $\Delta\theta_b$ is the phase angle deviation from 120° between the voltages v_a and v_b. Similarly, $\Delta\theta_c$ is the phase angle deviation from 120° between the voltages v_a and v_c.

B-1. Estimation of Phase Angle Deviations ($\Delta\theta_b$ and $\Delta\theta_c$)

The amplitude normalized three-phase voltages, as obtained by (6), is balanced only when the values of both phase angle deviations ($\Delta\theta_b$ and $\Delta\theta_c$) are zero. However, one or both phase angle deviations can be nonzero under unbalanced fault or loading conditions and hence the voltages will become unbalanced. In order to eliminate the phase angle error sourced by $\Delta\theta_b$ and $\Delta\theta_c$ in the performance of the PLL, their values have to be known. To calculate the value of $\Delta\theta_b$, $v_{a'}$ is considered as the reference signal and $v_{b'}$, as given in (6), can be expanded as follows:

$$\sin(\omega n T_s)\cos(2\pi/3 + \Delta\theta_b) - \cos(\omega n T_s)\sin(2\pi/3 + \Delta\theta_b) = v_{b'}(n) \quad (7)$$

At the beginning, which is the first zero-crossing point, of each cycle of $v_{a'}$, the values of $\sin(\omega n T_s)$ and $\cos(\omega n T_s)$ are equal to 0 and 1, respectively. Therefore, after putting the values of $\sin(\omega n T_s)$=0 and $\cos(\omega n T_s)$=1, equation (7) can be written as follows:

$$-\sin(2\pi/3 + \Delta\theta_b) = v_{b'}(n)$$

$$\Rightarrow \Delta\theta_b = -2\pi/3 + \sin^{-1}\{-v_{b'}(n)\} \quad (8)$$

It can be seen from (8) that the value of the voltage $v_{b'}$ at the first zero crossing of a cycle of $v_{a'}$ is required for calculating the value of $\Delta\theta_b$. On the other hand, in order to calculate the value of $\Delta\theta_c$, $v_{a'}$ is chosen as the reference signal and $v_{c'}$, as given in (6), can be expanded as follows:

$$\sin(\omega n T_s)\cos(2\pi/3 + \Delta\theta_c) + \cos(\omega n T_s)\sin(2\pi/3 + \Delta\theta_c) = v_{c'}(n) \quad (9)$$

It is known that $\sin(\omega n T_s)$=0 and $\cos(\omega n T_s)$=1 at the first zero crossing point of a cycle of $v_{a'}$. In this circumstance, equation (9) can be expressed as follows:

$$\sin(2\pi/3 + \Delta\theta_c) = v_{c'}(n)$$

$$\Rightarrow \Delta\theta_c = -2\pi/3 + \sin^{-1}\{v_{c'}(n)\} \quad (10)$$

The voltage $v_{c'}$ at the first zero crossing of each cycle of the voltage $v_{a'}$ is used for updating the value of $\Delta\theta_c$. So, equations (8) and (10) can be used to acquire the phase angle deviations of the phase voltages $v_{b'}$ and $v_{c'}$, respectively, where the voltage of phase 'a' is assumed as the reference. Equations (8) and (10) can give exact value of the phase angle deviations when the value of $v_{a'}$ is zero. However, for a fixed sampling frequency, discretization process can introduce errors in the estimated values of $\Delta\theta_b$ and $\Delta\theta_c$ when the voltage $v_{a'}$ is not sampled at exactly zero value. In this case, the amount of phase angle error introduced is $\Delta\theta_{er}=\sin^{-1}\{v_{a'}(n)\}$, where the value of $v_{a'}$ is positive. For a large sampling frequency, this error can be small and can be neglected. However, it can be significant for a small sampling frequency and hence need to be considered. This error can be subtracted from (8) and (10) to get the actual the values of $\Delta\theta_b$ and $\Delta\theta_c$. Fig. 4 shows a flowchart which demonstrates the algorithm used for calculating the values of $\Delta\theta_b$ and $\Delta\theta_c$.

In this paper, the voltage of phase 'a' is chosen as the reference. However, any phase voltage can be considered as the reference. In the three-phase system, the adjacent two phase voltages of the reference one (any one) are displaced by ±120° under balanced condition (or, ±120°±angle deviation under unbalanced phase angle condition). Zero crossing point (negative to positive) of the reference (can be any one) phase voltage is used for the estimation of the phase angle deviations

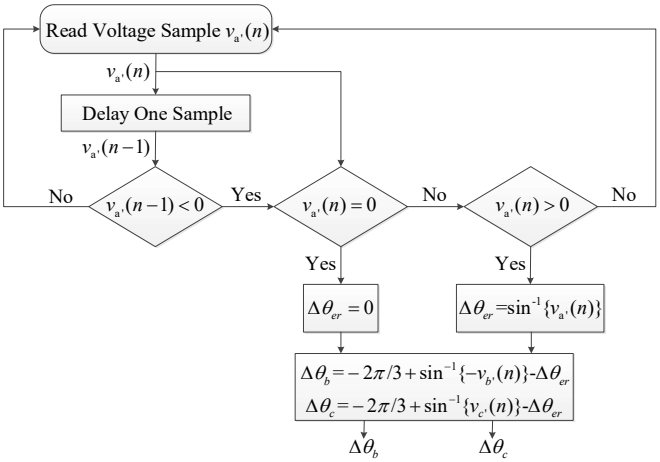

Fig. 4: Flowchart for calculating the phase angle deviations of the voltages at phases 'b' and 'c', where the voltage at phase 'a' is considered as the reference.

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of other two phase voltages. These deviations are calculated as relative angle deviations. Changing the reference phase will not cause any error.

B-2. Elimination of Phase Angle Deviations ($\Delta\theta_b$ and $\Delta\theta_c$)

The phase angle differences between two adjacent phases can be made equal to 120° by eliminating $\Delta\theta_b$ and $\Delta\theta_c$ from the voltages $v_{b'}$ and $v_{c'}$, respectively. For this purpose, $v_{b'}(n)$, as shown in (6), can be expanded as follows:

$$v_{b'}(n) = \sin(\omega nT_s - 2\pi/3)\cos(\Delta\theta_b) - \cos(\omega nT_s - 2\pi/3)\sin(\Delta\theta_b) \quad (11)$$

Equation (11) can be solved for obtaining an expression for $\sin(\omega nT_s\text{-}2\pi/3)$, thus (11) can be re-written as follows:

$$\sin(\omega nT_s - 2\pi/3)\cos(\Delta\theta_b) - v_{b'}(n) = \sqrt{1-\sin^2(\omega nT_s - 2\pi/3)}\sin(\Delta\theta_b) \quad (12)$$

After squaring both sides of (12), the following simplified relation is acquired.

$$\sin^2(\omega nT_s - 2\pi/3) - 2\cos(\Delta\theta_b)v_{b'}(n)\sin(\omega nT_s - 2\pi/3) + v_{b'}^2(n) - \sin^2(\Delta\theta_b) = 0 \quad (13)$$

The above relation is a quadratic equation and the solution for $\sin(\omega nT_s\text{-}2\pi/3)$ can be written as

$$\sin(\omega nT_s - 2\pi/3) = \cos(\Delta\theta_b)v_{b'}(n) \pm \sin(\Delta\theta_b)\sqrt{1-v_{b'}^2(n)} \quad (14)$$

The expression of $v_{c'}$, as given in (6), can be expanded as

$$v_{c'}(n) = \sin(\omega nT_s + 2\pi/3)\cos(\Delta\theta_c) + \cos(\omega nT_s + 2\pi/3)\sin(\Delta\theta_c) \quad (15)$$

Similar procedures, as presented from (11) to (14), can be followed for acquiring an expression for $\sin(\omega nT_s\text{+}2\pi/3)$ from (15). After derivation, the expression for $\sin(\omega nT_s\text{+}2\pi/3)$ can be expressed as

$$\sin(\omega nT_s + 2\pi/3) = v_{c'}(n)\cos(\Delta\theta_c) \pm \sin(\Delta\theta_c)\sqrt{1-v_{c'}^2(n)} \quad (16)$$

Both (14) and (16) have two solutions. Since the sum of the balanced three-phase voltages is zero, the actual solutions of (14) and (16) will satisfy the following condition:

$$v_{a'}(n) + \sin(\omega nT_s - 2\pi/3) + \sin(\omega nT_s + 2\pi/3) = 0 \quad (17)$$

where $v_{a'}(n)=\sin(\omega nT_s)$, as given in (6). After meeting the above condition, the phase balanced three-phase voltages can be obtained and expressed by new symbols as follows:

$$\left.\begin{aligned} v_{a''}(n) &= v_{a'}(n) = \sin(\omega nT_s) \\ v_{b''}(n) &= \sin(\omega nT_s - 2\pi/3) \\ v_{c''}(n) &= \sin(\omega nT_s + 2\pi/3) \end{aligned}\right\} \quad (18)$$

C. Instantaneous Phase Angles Estimation

The extracted three-phase balanced voltages, as given by (18), are used as the inputs of the Clarke and Park transformations based PLL to track the instantaneous phase angle ($\phi_a=\omega nT_s$) of the reference phase voltage v_a. The value of ϕ_a is also used with the estimated values of $\Delta\theta_b$ and $\Delta\theta_c$ to track the phase angles of other two phase voltages (v_b and v_c) and they are achieved by:

$$\phi_b = \phi_a - 2\pi/3 - \Delta\theta_b \quad (19)$$

$$\phi_c = \phi_a + 2\pi/3 + \Delta\theta_c \quad (20)$$

III.Simulation Results

MATLAB/Simulink is used for numerical result analysis of the proposed technique in a personal computer environment. The tuning parameters of the proposed phase angle estimation technique are selected as follows: sampling frequency=4 kHz, time constant of the LPF=20ms, k_p=50 and k_i=98696, where k_p and k_i are the gains of the proportional and integral controller, respectively, of the PLL. Reference [7] is followed to tune the parameters k_p and k_i. The odd and even harmonics contents, as shown in Table I, are reported in the IEC standard 61000-4-13 [30]. These harmonics are injected in the fundamental voltage component to create 14.58% total harmonic distortion (THD).

Case-1: Performance under balanced condition at nominal and off-nominal frequencies including harmonics

The steady-state response of the proposed ABSG and PBSG based three-phase PLL under harmonically polluted but balanced conditions is observed in Fig. 5. To create the condition, the amplitudes of the three phase voltages are set unity and the percentage of harmonic contents are set as in Table I. In addition, the fundamental frequency is varied from 45 to 55 Hz. Fig. 5 shows that the technique proposed here can produce the instantaneous phase angles of all the phases with error less than 0.2° under the created adverse condition.

Case-2: Performance under amplitude unbalanced condition at nominal and off-nominal frequencies including harmonics

The amplitudes of all the phases of the voltages are made unequal keeping the phase angles balanced. The amplitudes are A_a=0.9 p.u., A_b=1.2 p.u., and A_c=0.8 p.u.. The percentage of harmonic contents of each phase is presented in Table I. As shown is Fig. 6, the phase errors are less than 0.2°, which is similar to the balanced condition of case-1, for instantaneous phase angle estimation of all the phases under amplitude unbalanced condition including the variation of fundamental frequency in the range of 45 to 55 Hz and harmonics.

Fig. 7(a) shows three-phase voltage signals with the fundamental frequency of 50 Hz and unbalanced amplitudes including harmonics pollution. In this case, the fundamental voltage amplitudes of the three-phase voltages are changed by a

Table I: Harmonics based on IEC standard 61000-4-13 [30]

Harmonic					THD
2nd	3rd	4th	5th	7th	14.58%
3.0%	8.0%	1.5%	9.0%	7.5%	

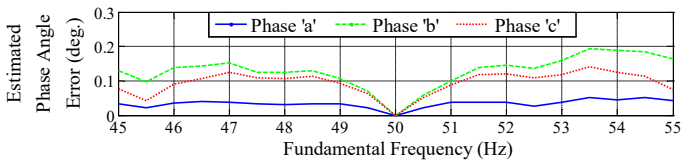

Fig. 5: Steady-state performance of the proposed technique at nominal and off-nominal frequencies, where the input voltages are balanced with unity amplitude but distorted by harmonics given in Table I.

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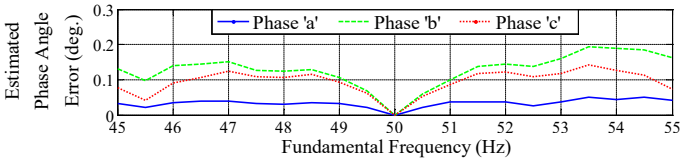

Fig. 6: Steady-state performance of the proposed technique at nominal and off-nominal frequencies, where only the amplitudes (A_a =0.9 p.u., A_b=1.2 p.u., and A_c=0.8 p.u.) are unbalanced and distorted by harmonics given in Table I.

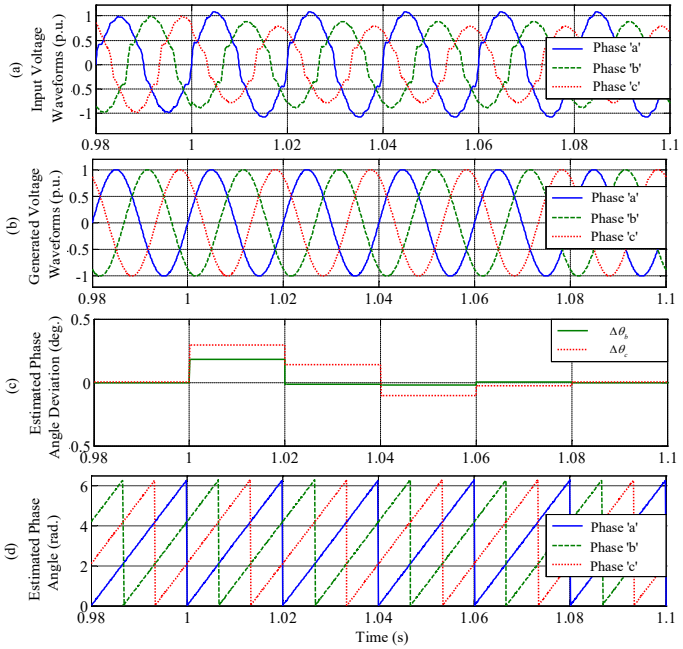

Fig. 7: Performance of the proposed technique when the unbalanced amplitudes are created by a step from 1.0 p.u. to A_a=1.1 p.u., A_b=0.90 p.u., and A_c=0.80 p.u. at time 1s and distorted by harmonics given in Table I.

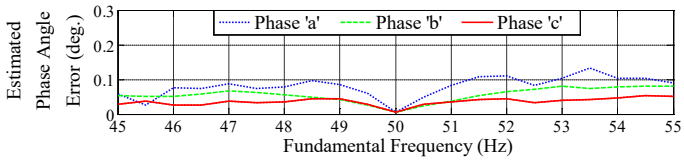

Fig. 8: Steady-state performance of the proposed algorithm at nominal and off-nominal frequencies, where only the phase angles ($\Delta\theta_b$=10° and $\Delta\theta_c$=5°) of the input voltages are unbalanced and distorted by harmonics given in Table I.

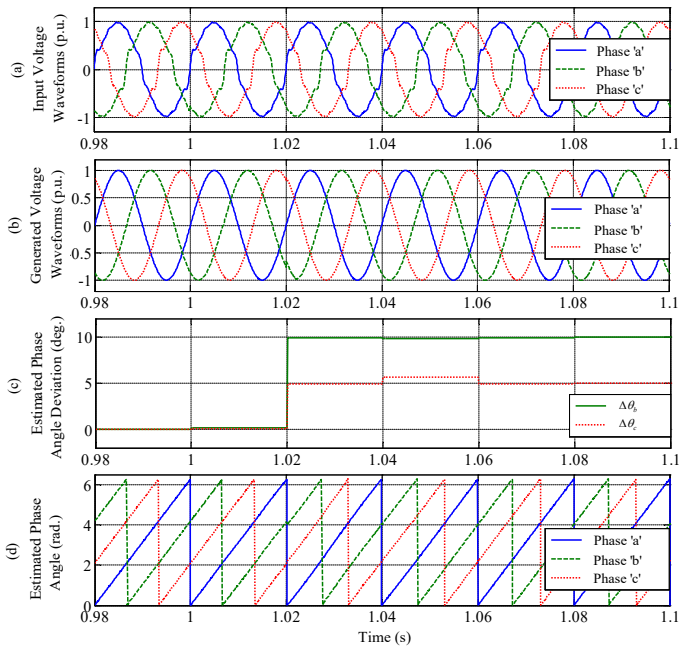

Fig. 9: Performance of the proposed technique when the unbalanced phase angles are created by a step from 0° to $\Delta\theta_b$=10° and $\Delta\theta_c$=5° at time 1s and distorted by harmonics given in Table I.

step from 1.0 p.u. to A_a=1.1 p.u., A_b=0.90 p.u., and A_c=0.80 p.u. at time 1s and the percentage of harmonics are shown in Table I. The response of the technique is also shown in Figs. 7(b)-(d) and it is seen that the technique can track the phase angles under amplitude unbalanced and harmonic distortions.

Case-3: Performance under phase unbalanced condition at nominal and off-nominal frequencies including harmonics

In this case, the phase angles of the system are made unbalanced - i.e. the angle difference between adjacent phase voltages is not 120°. Here, the fundamental voltage amplitudes of all phases are kept unity. The phase angle deviations are chosen as $\Delta\theta_b$=10° and $\Delta\theta_c$=5°. Harmonic pollutions are introduced also. The fundamental frequency is varied -5 to +5 Hz from the nominal value. Fig. 8 displays the steady-state response of the proposed phase estimation technique under the aforementioned condition. In this case, the estimated phase errors are less than 0.15°.

Fig. 9 shows the response of the technique when the imbalanced phase angles is created by a step from 0° to $\Delta\theta_b$=10° and $\Delta\theta_c$=5° with the amplitudes of the three phases being unity. It can be noticed from Fig. 9(c) that the technique needs 60 ms (3 fundamental periods) as settling time for tracking the phase steps where a ±2% error criteria is considered for calculating the settling time. However, after some transient time, the proposed technique can track the unbalanced phase angles accurately.

Case-4: Performance under both amplitude and phase unbalanced condition at nominal and off-nominal frequencies including harmonics

Fig. 10 depicts the errors of the estimated instantaneous phase angle by using the proposed technique under both the amplitude and phase unbalanced conditions with the presence of harmonic distortions. For this case, the fundamental voltage amplitudes are selected as A_a=1.0 p.u., A_b=1.1 p.u., and A_c=0.9 p.u. and the phase angle deviations are $\Delta\theta_b$=15° and $\Delta\theta_c$=10°. Similar to the case-3, the proposed technique generates less than 0.15° phase errors in the estimated instantaneous phase angles of the three-phase voltages.

In Fig. 11, the errors of the estimated instantaneous phase angle under both the amplitude and phase angle unbalanced condition at nominal fundamental frequency and with the presence of harmonics, as presented in Table I, is revealed. The phase angle deviation $\Delta\theta_b$ is varied from -20° to 20° in a step of 5° keeping the value of $\Delta\theta_c$=2°. In this case, the errors generated by the proposed technique are found to be less than 0.03°. The estimated errors are less than 0.02° when the phase angle deviation $\Delta\theta_c$ is varied from -20° to 20° in a step of 5° with the value of $\Delta\theta_b$=2°. Fig. 12 shows the simulation results. For Figs. 11 and 12, the fundamental amplitudes are set as A_a=1.0 p.u., A_b=1.1 p.u., and A_c=0.9 p.u..

Unequal fundamental amplitudes (A_a=1.2 p.u., A_b=0.8 p.u., and A_c=0.6 p.u.) and unequal phase angle displacement ($\Delta\theta_b$=

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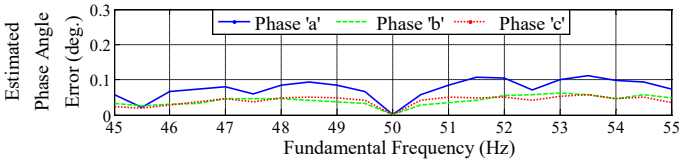

Fig. 10: Steady-state performance of the proposed algorithm at nominal and off-nominal frequencies, where both the amplitudes (A_a=1.0 p.u., A_b=1.1 p.u., and A_c=0.9 p.u.) and the phase angles ($\Delta\theta_b$=15° and $\Delta\theta_c$=10°) of the input voltages are unbalanced and also distorted by harmonics given in Table I.

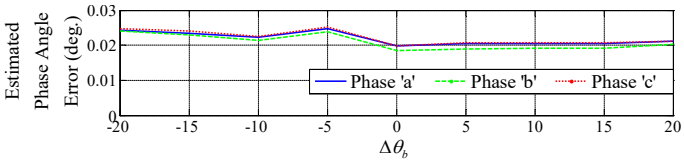

Fig. 11: Steady-state performance of the proposed algorithm at nominal frequency and various phase deviations ($\Delta\theta_b$), where both the amplitudes (A_a=1.0 p.u., A_b=1.1 p.u., and A_c=0.9 p.u.) and the phase angle ($\Delta\theta_c$=2°) of the input voltages are unbalanced and distorted by harmonics given in Table I.

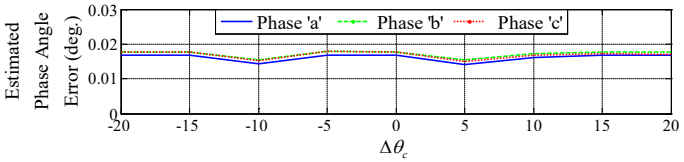

Fig. 12: Steady-state performance of the proposed algorithm at nominal frequency and various phase deviations ($\Delta\theta_c$), where both the amplitudes (A_a=1.0 p.u., A_b=1.1 p.u., and A_c=0.9 p.u.) and the phase angle ($\Delta\theta_b$=2°) of the input voltages are unbalanced and distorted by harmonics given in Table I.

-10° and $\Delta\theta_c$=10°) between adjacent phase voltages are created by a step from 1 p.u. and 0°, respectively, at time 1s. The generated three-phase voltage signals and the response of the technique are shown in Fig. 13. As it can be observed, after some transient time, the phase angles are tracked accurately by using the proposed technique under both amplitude and phase unbalanced conditions.

Performance comparison

The performance of the proposed technique is compared with the CDSC-PLL [18] and *dq*CDSC-PLL [22]. Same tuning parameters are used for the proposed and CDSC-PLL techniques. On the other hand, $CDSC_{2,4,8,16,32}$ and the loop filter based on proportional, integral and derivative (PID) controller with the gains reported in [22] is used for the *dq*CDSC-PLL technique. Fig. 14 demonstrates the performance comparison of these three techniques for different cases under harmonics at nominal frequencies. The presented techniques can generate accurate phase estimation, as shown in Fig. 14(a), when the voltages are balanced and also contain 10% DC offset. They take around 3 fundamental cycles as response time, as shown in Fig. 14(b), when unbalanced amplitudes are created by a step from 1.0 p.u. to A_a=1.1 p.u., A_b =0.90 p.u., and A_c=0.80 p.u. at time 1s. On the other hand, it can be seen from Fig. 14(c) that the proposed technique can track the phase angle accurately after the dynamic delay when unbalanced phase angles are created by a step from 0° to $\Delta\theta_b$=10° and $\Delta\theta_c$=5° at time 1s. In this case, both the CDSC-PLL and *dq*CDSC-PLL generate -1.66° offset error in the estimated phase angle after the transient. The CDSC-PLL and *dq*CDSC-PLL techniques also produce 5.39° offset error in the estimated phase angle after the transient, as shown in Fig. 14(d), when unbalanced

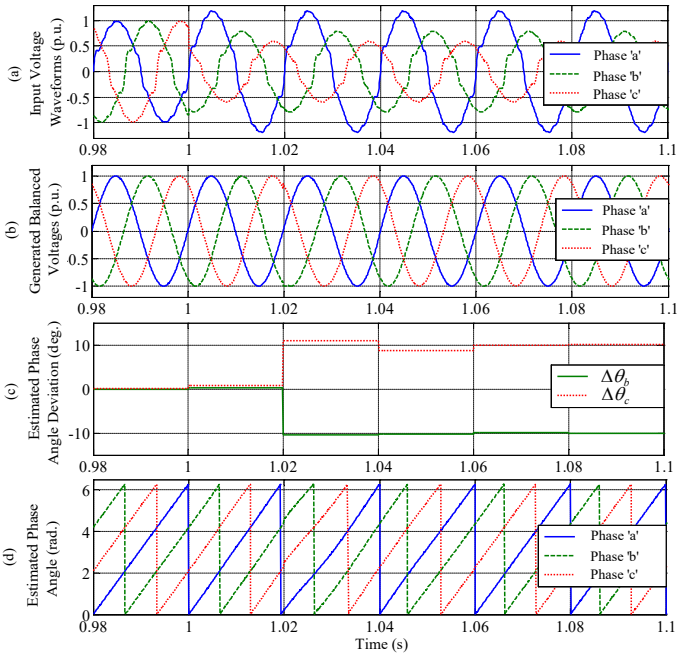

Fig. 13: Performance of the proposed technique when unbalanced fundamental amplitudes (A_a=1.2 p.u., A_b=0.8 p.u., and A_c=0.6 p.u.) and unbalanced phase angle displacement ($\Delta\theta_b$=-10° and $\Delta\theta_c$=10°) are created by a step from 1 p.u. and 0°, respectively, at time 1s and distorted by harmonics given in Table I.

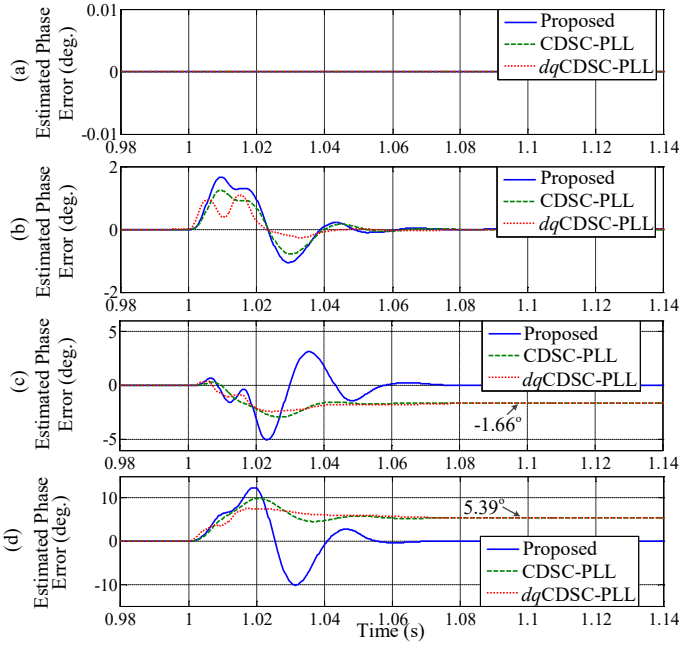

Fig. 14: Estimated phase error comparison among the proposed, CDSC [18] and *dq*CDSC [22] based PLLs under harmonics and (a) balanced voltages include 10% DC offset. (b) unbalanced amplitudes are created by a step from 1.0 p.u. to A_a=1.1 p.u., A_b =0.90 p.u., and A_c=0.80 p.u. at time 1s (c) unbalanced phase angles are created by a step from 0° to $\Delta\theta_b$=10° and $\Delta\theta_c$=5° at time 1s. (d) unbalanced amplitudes (A_a=1.2 p.u., A_b =0.80 p.u., and A_c =0.60 p.u.) and unbalanced phase angle displacement ($\Delta\theta_b$=-10° and $\Delta\theta_c$=10°) are created by a step from 1 p.u. and 0°, respectively, at time 1s.

amplitudes (A_a=1.2 p.u., A_b =0.80 p.u., and A_c =0.60 p.u.) and unbalanced phase angle displacement ($\Delta\theta_b$=-10° and $\Delta\theta_c$=10°) are created by a step from 1 p.u. and 0°, respectively, at time 1s.

It can be observed from the presented results that the proposed three-phase PLL algorithm can provide accurate phase estimation under amplitude and/or phase unbalanced

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condition. Moreover, it can provide phase estimation of all three-phase voltages. These advantages of using the proposed algorithm come at the cost of being more computationally demanding compared to the existing CDSC-PLL and *dq*CDSC-PLL. Therefore, a compromise is made between the phase estimation accuracy and digital resources consumption.

IV. Experimental Results

In this section, the real-time experimental performance of the proposed technique in dSPACE DS1104 platform is presented. The real-time three-phase voltage signals are generated by using the digital-to-analog converter (DAC) of the DS1104. The inputs of the analog-to-digital converter (ADC) can be regarded as the measured three-phase analog grid voltages, which are generated by the DAC of the DS1104. The experimental results are captured from the screen of an 8 Channels Tektronix MSO58 oscilloscope.

Fig. 15 reveals the real-time three-phase voltage signals and steady-state response of the proposed technique when both the amplitudes (A_a=1.2 p.u., A_b=0.8 p.u., and A_c=0.6 p.u.) and phase angles ($\Delta\theta_b$=15° and $\Delta\theta_c$=10°) are unbalanced. The technique can accurately generate three-phase balanced voltages and estimate the phase angle deviations, as can be seen in Fig. 15(a). It can also track the instantaneous phase angles of the unbalanced three-phase voltages accurately, which can also be noticed in Fig. 15(b).

The dynamic response of the proposed technique under both amplitudes and phase angles unbalanced condition is shown in Fig. 16. In this case, the unbalanced amplitudes of the three-phase voltages are created by a step as follows: A_a=1 to 1.2 p.u., A_b=1 to 0.80 p.u., and A_c=1 to 0.60 p.u.. The phase angle deviations are also changed by a step as follows: $\Delta\theta_b$=0° to 15° and $\Delta\theta_c$=0° to 10°. It can be seen from Fig. 16 that the technique requires 3 fundamental cycles as settling time for tracking the phase angle deviations and can also detect the phase angle accurately after the transient time.

The real-time transient response under unbalanced phase step condition is displayed in Fig. 17. In this case, the following phase steps are used: $\Delta\theta_b$=0° to 15° and $\Delta\theta_c$=0° to 10°. Similar to both the amplitudes and phase angles unbalanced condition, the technique spends 3 fundamental cycles as settling time for tracking the phase step deviations.

The experimental performance of the proposed technique under 10% DC offset and balanced three-phase voltages including harmonics is depicted in Fig. 18. As it can be noticed, the technique is also able to reject the negative effects caused by the DC offset.

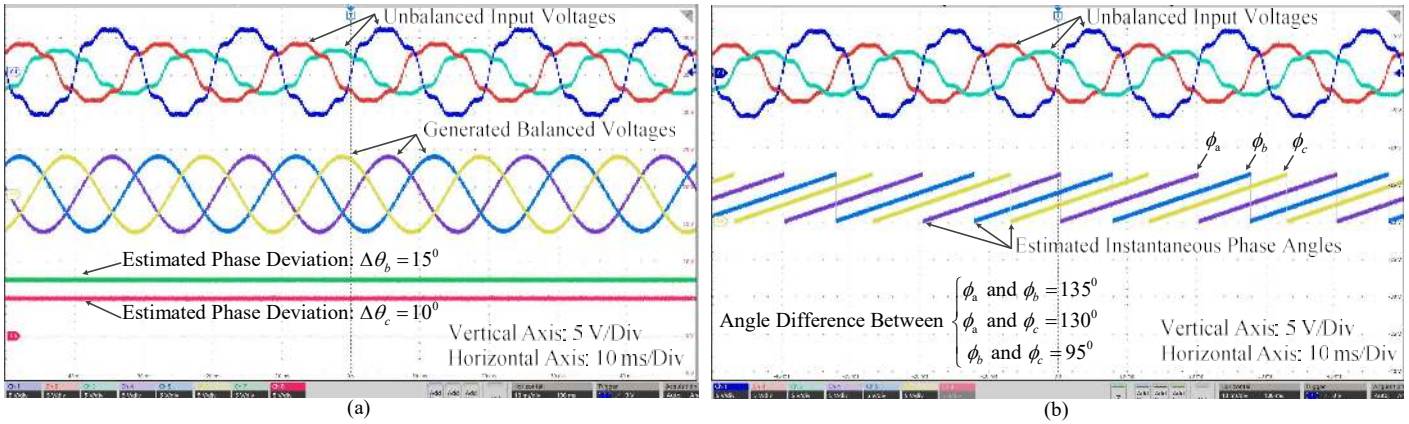

Fig. 15: Experimental results for both the unbalanced amplitudes (A_a=1 to 1.2 p.u., A_b=1 to 0.80 p.u., and A_c=1 to 0.60 p.u.) and unbalanced phase angles ($\Delta\theta_b$=15° and $\Delta\theta_c$=10°). (a) Input unbalanced three-phase voltages, generated balanced three-phase voltages, and estimated phase angle deviations of phases 'b' and 'c'. (b) Input unbalanced three-phase voltages and estimated instantaneous phase angles of three-phase unbalanced voltages.

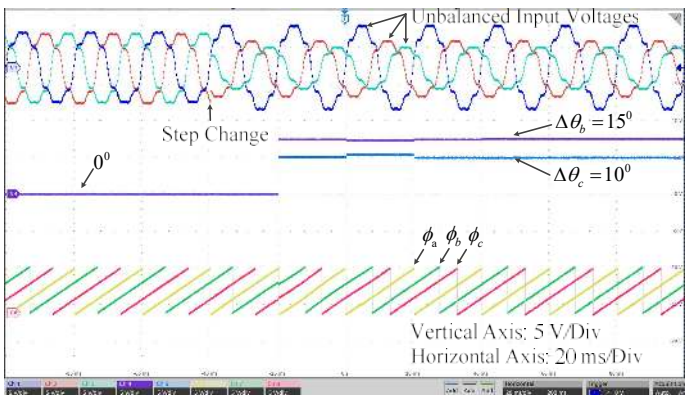

Fig. 16: Experimental results when unbalanced fundamental amplitudes (A_a=1.2 p.u., A_b=0.80 p.u., and A_c=0.60 p.u.) and unbalanced phase angle displacement ($\Delta\theta_b$=15° and $\Delta\theta_c$=10°) are created by a step from 1 p.u. and 0°, respectively.

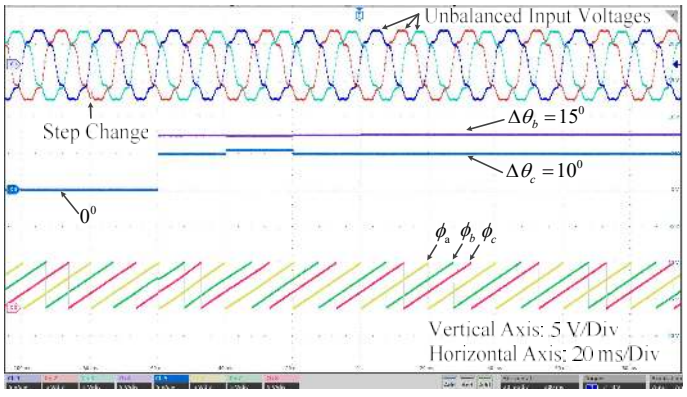

Fig. 17: Experimental results when unbalanced phase angle displacement ($\Delta\theta_b$=15° and $\Delta\theta_c$=10°) are created by a step from 0°.

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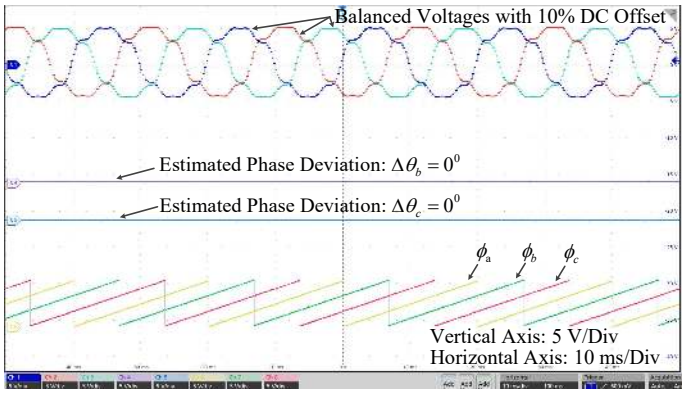

Fig. 18: Experimental results under balanced voltages and 10% DC offset.

V. Conclusions

An adaptive technique based on three-phase PLL has been proposed in this paper for estimating the instantaneous phase angles of the three-phase voltage system under amplitude and/or phase angle unbalanced conditions including harmonic pollutions and time-varying frequency environments. It relies on an amplitude balanced signal generator and a phase balanced signal generator for removing the negative consequences caused by the unbalanced conditions. It can effectively produce accurate phase angles of three-phase voltages under amplitude and/or phase angle unbalanced condition by using only a single PLL. The negative outcome of harmonics is also eliminated effectively by the proposed technique. When compared to the existing CDSC-PLL and *dq*CDSC-PLL algorithms, the proposed technique can provide better phase estimation under amplitude and phase unbalanced condition. The performance of the proposed technique has been verified by both simulated and real-time experimental results.

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