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Three-Phase Power Converter Based Real-Time Synchronous Generator Emulation

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I am submitting herewith a dissertation written by Liu Yang entitled "Three-Phase Power Converter Based Real-Time Synchronous Generator Emulation." I have examined the final electronic copy of this dissertation for form and content and recommend that it be accepted in partial fulfillment of the requirements for the degree of Doctor of Philosophy, with a major in Electrical Engineering.

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Three-Phase Power Converter Based Real-Time Synchronous Generator Emulation

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Abstract

To bridge the gap between power system research and their real application in power grids, a Hardware Test-Bed (HTB) with modular three-phase power converters has been developed at the CURENT center, the University of Tennessee, Knoxville, to emulate transmission level power systems with actual power flowing.

This dissertation focuses on the development and verification of a real-time synchronous generator (SG) emulator in the HTB. The research involved in this dissertation aims at designing a proper control to achieve emulator performance goal and investigating the sources of error and its influence on interconnected SG-emulator networks.

First, different interface algorithms (IAs) are compared, and the voltage type ideal transformer model (ITM) is selected based on the accuracy and stability. At the same time, closed-loop voltage control with current feed-forward is proposed to decrease the error caused by the non-ideality of the power amplifier.

The emulation is then verified through two different methods. First, the output waveforms of the emulator in experiment are compared with the simulation under the same condition. Second, a transfer function perturbation (TFP) based error model is obtained and redefined as the relative error for the amplitude and phase between the emulated system and the target system over the frequency range of interest. The major cause of the error is investigated through a quantitative analysis of the error with varying parameters.

Third, the stability issue associated with the interconnection of two SG emulators is studied. The small signal models of the two-generation system with constant current and constant impedance load are developed, and the main sources of instability are researched and verified. The

developed SG emulator is also verified in the two-area system by comparing the system dynamics visually.

Last, the 6^{th}-order SG model including transformer voltages and saturation effect is applied in the three-phase symmetrical fault scenario. Control parameters are designed based on the TFP error evaluation of the fault condition. The developed SG emulator is then tested and verified in line-to-line fault condition. In addition, the stability of the new SG emulator is studied again and compared with the previous emulation.

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Nomenclature

The *d*-axis, *q*-axis, and 0-axis components are denoted with the subscripts "*d*," "*q*," "0". In SG models the subscript "*fd*" denotes field winding, "*kd*" and "*kq*" denote *k*th damping circuits on *d*-axis and *q*-axis. Δ indicates linearized small signal variables.

u_d, u_q, u_0	SG terminal voltage on *dq0*-axis (emulator voltage references)
u_t	SG terminal voltage amplitude
i_d, i_q, i_0	SG stator currents on *dq0*-axis
e_{fd}	SG field voltage
ω_r	SG rotor speed
ω_s	Synchronous speed
i_{fd}, i_{kd}, i_{kq}	SG field and damping circuit currents
R_{fd}, R_{kd}, R_{kq}	SG rotor circuit resistances
X_{ffd}, X_{kkd}, X_{kkq}	SG rotor circuit self-reactance
X_{ad}, X_{aq}	SG mutual reactance between rotor and stator circuits
X_l	SG stator leakage reactance
R_a	SG armature resistance per phase
ψ_d, ψ_q, ψ_0	SG stator flux linkages
ψ_{fd}, ψ_{kd}, ψ_{kq}	SG rotor flux linkages
T_e	SG torque
X_d, X_q	SG stator self-reactance
X'_d, X'_q	SG transient reactance
X''_d, X''_q	SG sub-transient reactance
T'_{do}, T'_{qo}	SG transient open-circuit time constant
T''_{do}, T''_{qo}	SG sub-transient open-circuit time constant
E'_d, E'_q	SG transient back EMF
E''_d, E''_q	SG sub-transient back EMF

P_m	SG mechanical power
P_e	SG electric power
H	SG inertia
M	SG inertia constant
D	SG damping factor
δ	SG rotor angle
T_G	Main servo time constant of a governor
T_{CH}	Time constant of main inlet volumes and steam chest
T_{RH}	Time constant of reheater
F_{HP}	Fraction of total turbine power generated by high pressure section
U_{tref}	SG terminal voltage amplitude reference
K_A	SG excitation system gain
T_e	SG excitation system time constant
$Z_f = L_f s + R_f$	Converter filter impedance
V_{dc}	Converter DC side voltage
v_d, v_q	Converter output voltages on dq-axis
d_d, d_q	Converter duty cycles on dq-axis
$Z_L = L_L s + R_L$	Load impedance
L_{fc}, R_{fc}	Current feed-forward parameters
$F_V = \frac{\omega_V}{s + \omega_V}$	First order low pass filter (LPF) on voltage sensing
$F_I = \frac{\omega_I}{s + \omega_I}$	First order LPF on current signals
Δt	Total time delay in a converter
K_p, K_i	PI controller parameters
ER_{TFP}	Transfer function perturbation (TFP) based error
$[Z_g] = \begin{bmatrix} Z_{gdd} & Z_{gdq} \\ Z_{gqd} & Z_{gqq} \end{bmatrix}$	SG model output impedance matrix on dq-axis
$[G_{gf}] = \begin{bmatrix} G_{gfd} \\ G_{gfq} \end{bmatrix}$	SG model gain matrix on excitation voltage on dq-axis

$[Z_{\mathrm{c}}] = \begin{bmatrix} Z_{cdd} & Z_{cdq} \\ Z_{cqd} & Z_{cqq} \end{bmatrix}$	Converter output impedance matrix on dq-axis
$[G_v] = \begin{bmatrix} G_{vd} & 0 \\ 0 & G_{vq} \end{bmatrix}$	Converter gain matrix on reference voltages on dq-axis
$[Z_p] = [G_v][Z_g] + [Z_{\mathrm{c}}]$	SG emulator output impedance matrix on dq-axis
$[G_{vg}] = [G_v][G_{gf}]$	SG emulator gain matrix on the excitation voltage on dq-axis
$[Z_T]$	Local line impedance matrix on dq-axis

1 Introduction

Electric power system research, including design, testing, and application, is mainly performed through two different ways: digital simulation and hardware based testing.

1.1 Digital Simulation

Digital simulation, including off-line and real-time, is done by solving differential and algebraic equations of the target system represented by mathematical models for each component, thus predicting the behavior of the system in time domain [5]. The accuracy of the mathematical models and the robustness of the numerical method in use, therefore, dictate the validity of the simulated results.

Off-line simulation is widely used for preliminary design due to its easy accessibility, installation, intuitive user interface, unlimited power level and number of buses. However, the complexity of mathematical models has to compromise on computational resources and simulation running time. Therefore, different simulation software have been developed aiming at areas that involve various level of model complexity. Table 1-1 lists several widely used simulation tools designed and optimized for various power system and power electronics research purposes [6]-[8]. Simulation tools such as Power System Simulation for Engineering (PSS/E) and Transient Security Assessment Tool (TSAT) are designed mainly for studying dynamics of large scale power systems and the behavior of high level controllers. Sometimes hundreds or thousands of buses are involved in one simulated system; simplified generator, transmission line, and load models are thus applied with large integration time steps to minimize computation time [6]. Electromagnetic Transient Program (EMTP) based simulation tools such as PSCAD/EMTDS, ATP and EMTP-RV are implemented with complicated component models that can accommodate network nonlinearities

and unbalanced conditions and therefore generate more accurate results in a high frequency domain [8]. SABER, on the other hand, is designed for analog, digital, mixed-signal, and mixed-technology simulations. The simulation time step can be set as small as several nano-seconds, making the software suitable for simulating electronic circuits with very high frequencies [7].

Table 1-1. Off-line simulation tools.

Name	**Time Step**	**Integration Method**	**Application**
PSS/E	Fixed	Explicit Trapezoidal	Electromechanical
TSAT	Fixed	Variable	
MATLAB/Simulink	Variable/fixed	Variable	Generic
ATP, PSCAD/EMTDC, EMTP-RV (EMTP Based)	Fixed	Implicit Trapezoidal	Electromagnetic
SABER	Variable	Variable	Semiconductor devices modeling

Real-time (RT) simulation tools, on the other hand, are capable of performing simulations synchronized with a real-time clock. Unlike off-line simulation where variable integration time step can be applied to accelerate simulation time, fixed time step is the only choice for RT simulators in order to synchronize with a RT clock. Usually, special hardware devices with multiple digital processors are required to guarantee fast computation. Commercial real-time simulators such as RTDS [9], Opal-RT, and RT-LAB [10] have been developed and widely used in various applications. RT simulation tools are typically used for two purposes: (1) full digital simulation as an extension of off-line simulation [11] and (2) hardware-in-the-loop (HIL) simulation.

Digital simulation tools in general are widely used in the early stage of modeling and developing control algorithms and device prototypes. However, because of their absolute dependency on

numerical calculation, they suffer from problems such as numerical oscillation due to discontinuities and interpolation without proper selection of time step or integration method [5]. At the same time, even though mathematical models of diverse devices are well developed, many users of digital simulation tools tend to simplify or ignore critical conditions such as measurement error, time delay, non-linearity, electromagnetic interference, etc. This leads to scenarios with impractical and unrealistic simulation parameters. Currently, there is no comprehensive simulation software that takes every possible aspect into consideration. Furthermore, in spite of a sophisticated design methodology, a defect in equipment or a system cannot be detected or noticed without field testing. All of the above reasons stimulate the need of testing facilities to bridge the gap between simulation and real world application.

1.2 Hardware Based Testing

As mentioned above, field testing of a hardware under test (HUT) is an irreplaceable step before the actual application. In power system studies, diverse experimental platforms have been developed for testing either control algorithms or real equipment.

In the early 1920s, miniature systems with small three-phase generators, loads, and artificial transmission lines were built to investigate power flow characteristics with multiple generators. Two example systems used 3.75 kVA, 440V, and 200-600 kVA, 2.3 kV machines, respectively [1]-[2].

In 1929, an AC network analyzer was first introduced and demonstrated by MIT and GE [3]. The network analyzer utilized phase-shifting transformers to represent synchronous generators, while scaled down resistors, inductors, and capacitors were used to represent transmission lines and loads in single phase. It was designed to run at 200 V, 0.5 A, and a frequency higher than 60 Hz, such as 440 Hz or 480 Hz, to reduce the size of the components. The network analyzer was

applied to general calculation of load flow and fault events, but the absence of machine mechanical models limited its capability to simulate electromechanical dynamics.

The National Renewable Energy Laboratory (NREL) has developed a large testing platform that has an 8.8 MW wind farm, 1 MW PV array, 7 MVA controllable grid interface (CGI), and 2.5 MW dynamometer for grid integrated renewable generation and energy storage [12][13].

The Consortium for Electric Reliability Technology Solutions (CERTS) microgrid (MG) concept has been demonstrated at the CERTS microgrid-American Electric Power (AEP) test bed, located near Columbus, Ohio and operated by AEP. The test bed is implemented with three 60 kVA combined-heat-and-power units and four load banks including induction motor [14][15].

Florida International University developed a smart grid testbed at its Energy Systems Research Laboratory with a total power capability of up to 72 kW [17][18]. The smart grid consists of an interconnected AC and DC grid. The AC grid operates at 208 V with four 13.8 kVA synchronous generators, passive and induction motor loads. The DC grid operates at 300 V with battery storage, 3 kW solid oxide fuel cells (SOFC) emulators, and DC loads.

However, hardware based testing also has many disadvantages. First, the experimental platforms are bulky, expensive, and less accessible, while a digital simulation environment is comparatively cheap and can be installed on a personal computer. Second, testing facilities generally require much more effort to start or reconfigure, and they have a limited number of buses. Third and foremost, a scaled down version of an original high voltage level system is required to achieve cost effectiveness in experimental platforms. However, although transmission lines and load parameters can be scaled down to the laboratory application precisely by using corresponding components with smaller ratings, a large rotating machine cannot be represented by a smaller one. Since the inertia is related to a machine's mass and the resistance to inductance ratio varies

dramatically with respect to the size, different machines will have distinct dynamic behavior. At the same time, the high cost of large machines also constrains the development of such experimental platforms.

1.3 Hybrid Simulation

The advancement of microprocessors and the invention of real-time simulators such as RTDS and Opal-RT in the 1980s gave rise to a new trend of combining digital simulations and physical tests together to form a "hybrid simulation" environment—hardware-in-the-loop (HIL) [9]-[11]. In this way, the testing efficiency and effectiveness can be largely improved with the flexibility of a digital simulation tool. HIL has been widely applied in many areas, such as automotive systems [20][21], robotics [23], power systems [22][25][26], power electronics [24], and off-shore systems [32]. At the same time, the utilization of power amplifiers allows power level HIL (PHIL) testing of a HUT. This makes a scaled-down machine with the original inertia time constant and inductance to resistance ratio feasible through the digital modeling.

PHIL, also called converter based emulation, implements power amplifiers, such as converters, as interfaces to test different equipment. The RT simulator controls the power amplifier to behave like the interfacing point to the HUT with proper interface algorithms to guarantee the correct operation. The power amplifier can provide or absorb power, thus a bidirectional structure is needed. The HUT then can be tested with both the controller and the power stage with actual power exchange, as shown in Fig. 1-1.

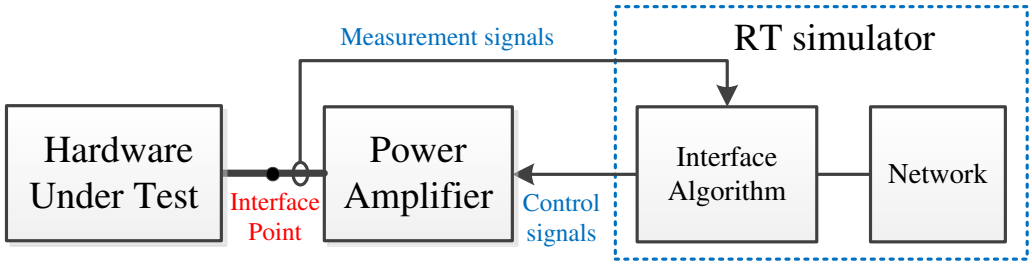


Fig. 1-1. Power-level HIL simulation

Most applications of PHIL systems are designed for testing only one equipment, but several platforms also utilized this technology to improve their flexibility for testing system level control algorithms, where the emulation of multiple power grid components are required. At low voltage level, a microgrid test bed has been developed by United Technologies Research Centre Ireland and University College Cork. The generators, motors, and loads in the test facility are emulated by programmable converters [65]. However, this platform aims at microgrid testing; it is thus not suitable for transmission level power system research. At the same time, since lumped inductors and resistors are used for emulating lines, the line distance is not easy to modify. At medium voltage level, the Power System Simulator developed by Central Research Institute of the Electric Power Industry (CRIEPI) in Japan implemented a PHIL system in addition to their existing platform to study wide area power system operation [95]. Even though the PHIL system can emulate a large area, most power system components in the platform are still represented by real generators and loads with large ratings, which is costly and also has limited flexibility.

Therefore, a transmission level testing facility with maximized flexibility, comprehensive testing environment, and cost effectiveness for reproduction is in the need for the verification of power system control algorithms.

2 The CURENT Hardware Test-Bed

Based on the PHIL concept, a Hardware Test-Bed (HTB) developed by the CURENT center at the University of Tennessee, containing modular and reprogrammable three-phase converters and a reconfigurable structure is proposed to emulate large scale power systems. The HTB will allow testing, integration and demonstration of various key technologies in monitoring, control, actuation, and visualization. With HTB, it is also convenient to test different system architectures such as HVDC vs. HVAC by reconfiguring the system structure. The impact of renewable energy sources, responsive loads, and energy storage to the power grid can also be evaluated [71]. The converters in the HTB are connected at both AC and DC side, with an active rectifier to provide steady DC side voltage [72], as shown in Fig. 2-1. In this way, each of the converters can be bidirectional, and with power circulating between AC and DC buses, the total power consumed from the grid is only to make up the losses in the test-bed.

The HTB in a way can be viewed as a parallel computation system where the network solutions are realized by laws of physics, while its true merit lies in its comprehensive inspection of a hardware under test (HUT) or a control algorithm under realistic circumstances before its application in power grids. Compared with digital simulation, the HTB has the following advantages:

1) Integrates real-time communication, protection, control, and cyber security
2) Able to test the reliability of the system incorporating real communication, measurements, and various equipment
3) Provides a platform for research on converter control and design in utility applications, such as AC/DC microgrid

4) Capable of performing prolonged real-time experiments, and demonstrating detailed system information simultaneously

5) Less dependency on numerical calculation, while allowing more flexibility of the whole system

Many different kinds of emulators have been developed or are under development: steam turbine synchronous generator emulator [73][74]; constant impedance, constant current, and constant power (ZIP) load emulator [71]; induction motor emulator [75]; wind turbine emulator with permanent magnetic synchronous generator (PMSG) [76]; solar emulator with two stage PV inverter [77]; transmission line emulator [78]; energy storage emulator (flywheels); HVDC emulator; and real-time simulator interface.

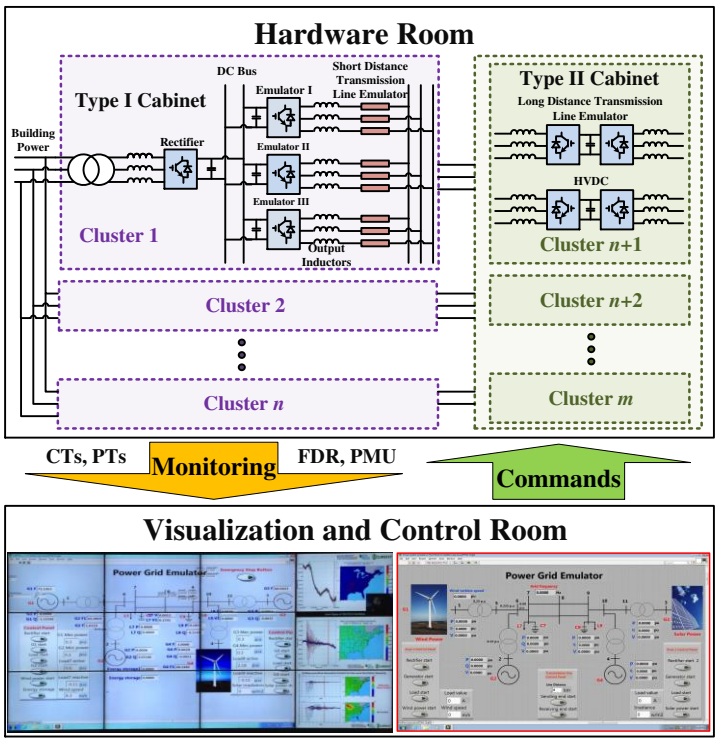


Fig. 2-1. Architecture of CURENT HTB.

2.1 HTB Structure

The cabinets in the HTB can be divided into two categories: Type I cabinet, which includes three power generation or load emulators, one rectifier or RTDS interface, and local transmission line and/or transformer emulators (inductors); and Type II cabinet, which consists of three sets of back-to-back converters to emulate HVDC or long-distance transmission line. Currently, the HTB has four cabinets: three Type I cabinets and one Type II cabinet. All the cabinets apply 75 kVA commercial converters produced by VACON, as demonstrated in Fig. 2-2. At the same time, the four cabinets connect with a multi-terminal HVDC system fed by two off-shore wind farm emulators to form a three-area system as shown in Fig. 2-3. Areas 1 and 2 are based on a very fundamental and typical two-area power grid system presented in [79]. In area 2, generator 3 is replaced by a wind farm. The three areas are interconnected by 220 km, 110 km, and 66 km transmission lines, respectively. In addition, with the RTDS interface in cabinet/area 1 and 2, the emulators will not be limited to emulating a single generation or load unit, but instead a local area, as an example shown in Fig. 2-4.

In the HTB, each emulator is designed to be 208 V, 15 kVA. To emulate power system components, often with megawatt and kilovolts level units, proper rescaling is necessary. The rescaling principle is that after rescaling, the per unit value of the physical and electrical parameters based on generator ratings will stay the same, but the time scale of the system can be varied by changing the base frequency to maintain the same local transmission line inductance in different systems. With the same structure, power system stabilizer (PSS) parameters can be directly used in the rescaled system.

(a) Front row (b) back row

Fig. 2-2. HTB cabinets.

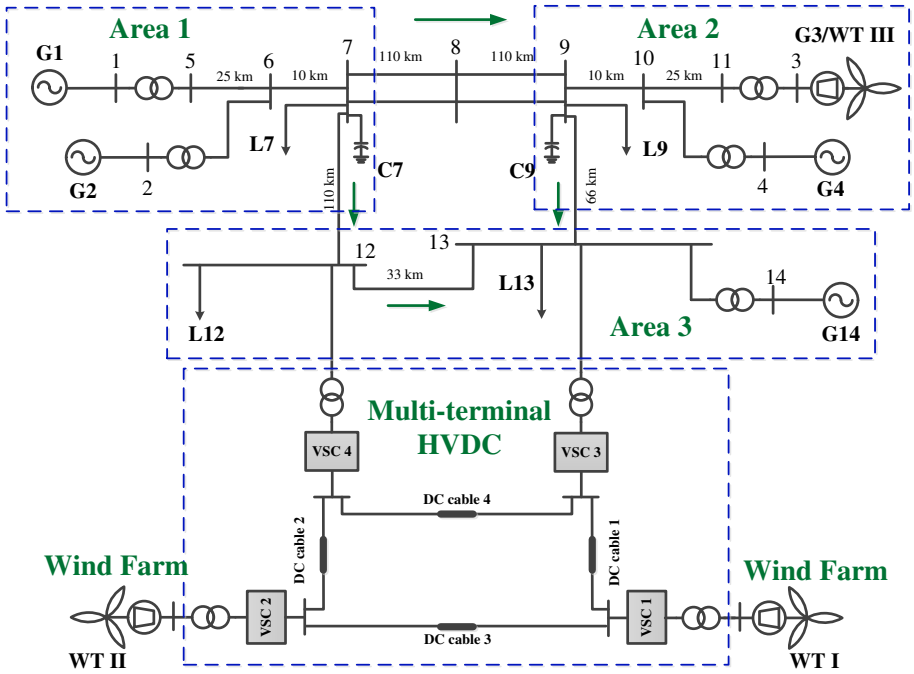


Fig. 2-3. Structure of the three-area system.

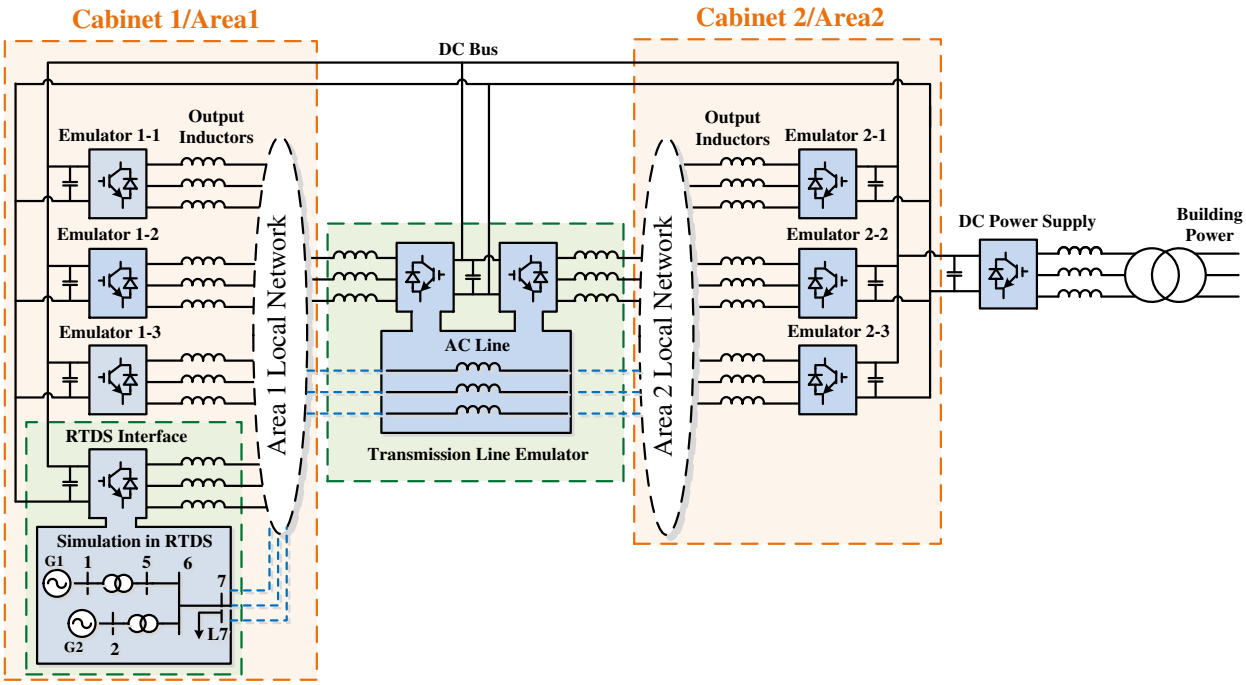


Fig. 2-4. HTB with RTDS interface.

2.2 Communication, Control, and Visualization

NI LabVIEW interface is applied to realize power system level communication and control. By using a CompactRIO-9081 made by NI, the HTB can be controlled remotely. The CompactRIO includes three NI 9205 analog input modules with 16-bit resolution and 250 kS/s aggregate sampling rate, an 8-slot Spartan-6 LX75 FPGA for real time calculation, two Gigabit Ethernet, two serial, two high-speed CAN interface ports, and a 14-port CAN breakout box for connectivity and expansion.

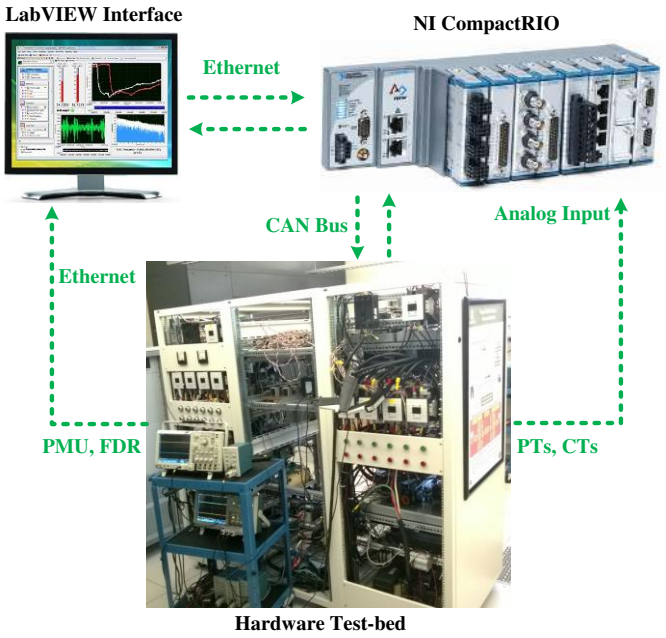


Fig. 2-5. HTB communication structure.

The communication between the computer (LabVIEW interface) and the NI CompactRIO is realized through Ethernet, which enables remote control of the HTB. Each emulator is implemented with a Texas Instrument DSP TMS320F28335, which receives commands (start and stop of the emulators) or data (wind speed, radiation, load consumption, etc.) from and sends data to the NI CompactRIO through the CAN bus, as shown in Fig. 2-5.

In addition to the communication with the NI CompactRIO, one designated emulator sends a PWM synchronization signal to the rest of the emulators to eliminate high frequency circulating current caused by the structure of the HTB [82].

To mimic a real control center in the power system, potential transformers (PTs), and current transformers (CTs) are installed at bus 1, 2, 3, 4, 7, and 9 to monitor the power flow, voltage amplitude and angle independently. Signals from PTs and CTs are directly delivered to the analog

input of the NI CompactRIO. At the same time, frequency and phase information monitored by PMUs and FDRs are sent to the LabVIEW interface through Ethernet.

For the control part, secondary/Automatic Generation Control (AGC) and tertiary frequency control are accomplished in LabVIEW. In traditional AGC, as shown in Fig. 2-6, Δω is the frequency deviation in one area, ΔP_{12} is the tie-line power flow difference (measured from Bus 7) [81]. The discrete integrator integrates every two seconds, and the output will be combined with droop output to adjust generation. In addition to the traditional integration, AGC can be also realized through state estimation or other improved methods. Tertiary frequency control can be realized directly by changing the power generation and consumption reference of each emulator. For wind/solar energy emulators, data with random wind speed/irradiance level changing with time can be generated in the LabVIEW and sent to the emulator.

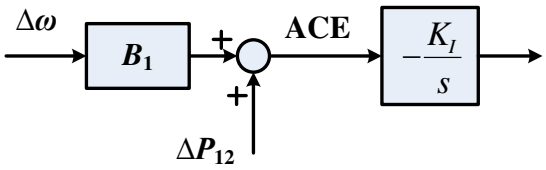


Fig. 2-6. AGC structure.

2.3 Summary

Since SGs are the most important components in power grids, the primary goal of this paper is to develop an SG emulator with high precision for various testing scenarios in the HTB. The next chapter will discuss the procedures of developing an SG emulator by using a three-phase voltage source converter, challenges, state of art technologies, and proposed solutions.

2.4 Dissertation Organization

The dissertation report is organized as follows:

Chapter 3 gives a detailed literature review on the state of the art technologies in developing SG emulators. The challenges are discussed and addressed, and the corresponding research objectives and approaches are introduced.

Chapter 4 compares the three different SG electric models and introduces the mechanical models. Common numerical methods in real-time computation of SG models are studied.

Chapter 5 establishes the converter control target and corresponding algorithm to fulfill the performance target.

Chapter 6 verifies the developed SG emulation both visually and quantitatively. The main factors that influence the performance are discussed and verified.

Chapter 7 studies the stability issues related to the interconnection of multiple SG emulators. The main causes of instability are investigated. Verification of the developed SG emulator is also conducted in the two-area system.

Chapter 8 develops the SG emulator with 6^{th}-order SG model in order to accommodate the fault emulation requirement. Control parameters are designed based on the error evaluation, and the stability of multiple interconnected SG emulators are studied.

Chapter 9 summarizes the dissertation's key contributions to and potential future efforts in synchronous generator emulation research.

3 Literature Review on Converter Based Emulation

In order to test the power stage of a real-time system, PHIL is preferable considering the testing scope, the development cycle, and the cost effectiveness. The development of a PHIL system involves several aspects, including defining the scope of testing, selecting a RT simulator and numerical method, designing the proper interface algorithm and controller, and verifying the fidelity of the emulator. Fig. 3-1 shows the process of developing an SG emulator. Each of the steps will be discussed in detail in this chapter.

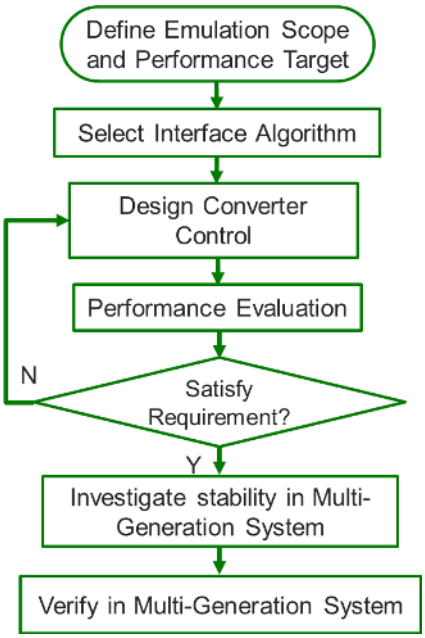


Fig. 3-1. Procedure for developing SG emulators.

3.1 Emulation Scope

The bandwidth (up to several kHz) of a three-phase voltage source converter (VSC) is limited by the switching frequency (up to tens of kHz for IGBT based converters). That means, a converter

based emulation can cover all of the electromechanical and only part of electromagnetic events in the power system, as demonstrated in Table 3-1 [80].

Table 3-1. Classification of power system transients.

Mode	Frequency (Hz)	Event
Electromechanical Phenomena	0.001	Load Frequency Control
	0.01	
	0.1	
	1	Transient Stability
	10	Stabilizer
	10^2	Short-circuits, Sub-synchronous resonance, Harmonics, Power Conversion Phenomena
Electromagnetic Phenomena	10^3	
	10^4	Switching Transients
	10^5	
	10^6	Traveling Wave Phenomena
	10^7	Transient Recovery Voltage

Even though large bandwidth can be achieved by converters, all the previous work on emulating SGs only involved steady state or dynamic emulation with small disturbance, and little effort has been reported in emulating SGs during fault conditions [31][32][50][51][52][64]. Since short-circuit fault is an important research area in power systems, it is then required to guarantee the experimental capability of the HTB.

In a synchronous generator, the electromagnetic phenomena, including transient and subtransient dynamics, play an important role in determining the corresponding short-circuit current. Accurate SG models with the above parameters need to be selected, and the control bandwidth has to be designed large enough to cover the dynamic behaviors. In addition, the fault current in an SG can reach as high as ten times the rated current, which demands a further down-scaling of the SG ratings where the converter rating is high enough to produce the fault current.

3.2 Interface Algorithm

The digital to analog IA is a key element in PHIL simulation. Take the system described in Fig. 3-2 as an example, where Z_s is the source impedance and Z_L is the load impedance. The IA defines the type of input and output signals transmitted between the simulation and the hardware and how the signals are processed, as shown in Fig. 3-3. The ideal transformer model (ITM) algorithm is the most common choice in various PHIL applications because of its simplicity [31][34][40]-[50]. There are two types of ITM based IA: the voltage type and the current type. As shown in Fig. 3-4 (a), the voltage type IA takes the current information as input in the digital computation and gives voltage signal as output to the analog side, denoted as V_M. The current type, on the other hand, takes voltage as input and provides current as output as shown in Fig. 3-4 (b).

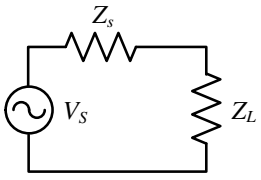


Fig. 3-2. The target system.

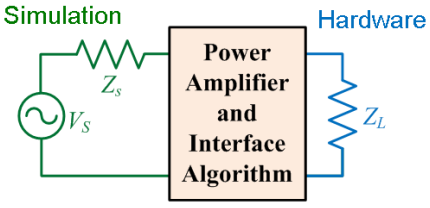
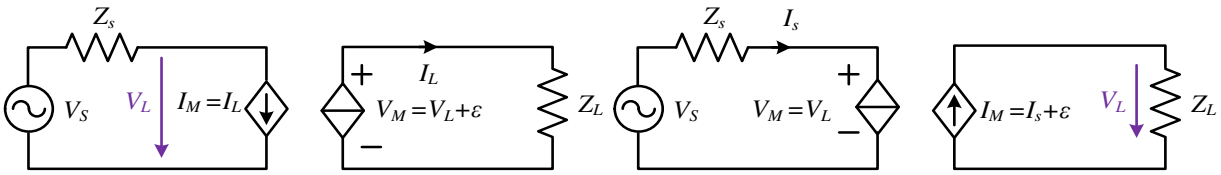


Fig. 3-3. PHIL simulation of the target system.



(a) Voltage type ITM. (b) Current type ITM

Fig. 3-4. Emulator types.

However, power amplifiers—especially the ones with high power ratings—are non-ideal. The non-ideality of a VSI, represented by ε in Fig. 3-4, mainly comes from two sources: time delay and modulation. Normally, nonlinearity due to over modulation can be avoided, switching harmonics can be filtered, and dead time can be compensated, which leaves time delay as the major factor causing errors. In order to decrease the steady-state error and solve the stability problems caused by time delay, improved IAs have been proposed in several papers, such as time-variant first-order approximation (TFA) [35], transmission line mode (TLM) [91], partial circuit duplication (PCD) [38], damping impedance method (DIM) [38], etc. These IAs derive from large-scale circuit simulation methods [92][93], and involve either modified impedance to approximate the time delay or some level of estimation of the load.

In the voltage type ITM, the closed-loop transfer function of the PHIL system can be described as:

$$\frac{i_L}{V_s} = \frac{1}{1 + \frac{Z_s}{Z_L} e^{-s\Delta t}} \frac{1}{Z_L} e^{-s\Delta t} \tag{3-1}$$

where Δt is the time delay. If $\frac{1}{Z_L} e^{-s\Delta t}$ is stable, the stability of the above system can be determined by its open loop transfer function $G_{LP} = \frac{Z_s}{Z_L} e^{-s\Delta t}$ [94]. In [38], the author concluded that the stability is guaranteed if the amplitude ratio $|Z_s/Z_L| < 1$, which is a very conservative criterion. In fact, time delay also influences the stability. For instance, assume $Z_s = 0.1s + 1.2$ and $Z_L = 0.2s + 1$, the bode plot of G_{LP} when $\Delta t = 0.5$ ms and $\Delta t = 1$ ms is demonstrated in Fig. 3-5. Although $|Z_s/Z_L| > 1$, the system can be either stable or unstable depending on the amount of time delay. Apparently, smaller time delay will improve the system stability. The time delay in a VSI is caused by sensing, digital processing, and the driving of the switching devices, while in a PHIL system, additional time delay is introduced by digital computation in a RT simulator and its

communication with a power amplifier [39]. An RT simulator is needed when a complicated network structure is involved in simulation. If only a simple component is considered, reduction of time delay can be realized by directly coding the digital simulation within the same switching cycle with the converter control in the digital processor on a VSI. In the CURENT HTB, the typical time delay of a converter with 10 kHz switching frequency is 150 μs, while 500 μs and 425 μs in the PHIL systems were reported in [38] and [39], respectively. Moreover, the improved IAs all have voltage type output signals in order to realize the open loop control of a VSI. In fact, proper converter closed-loop control can compensate the time delay phase lag in the VSI within its control bandwidth, thus eliminating the steady state error. In conclusion, ITM with closed loop converter control is adequate in emulating an SG.

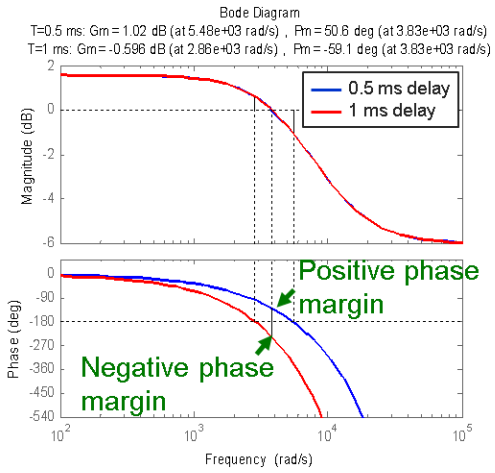


Fig. 3-5. Bode plot of G_{LP} when $\Delta t = 0.5$ ms and $\Delta t = 1$ ms.

Theoretically, both voltage and current type ITM are suitable for emulating SGs. In electromagnetic simulation environments, such as Matlab/Simulink and RTDS, SGs are modeled as current sources [83]. As shown in Fig. 3-6, K_s^r is the transformation matrix from the stationary

reference frame to the rotor reference frame. This is because machines are inductive in nature, and the circuit model equations are naturally driven by input voltages. If a steady voltage can be provided by the rest of the network, current type ITM can be utilized to interface with the current type SG model, such as in [50]. This method is also very popular in motor emulation [42]-[49]. However, if the SG itself is the voltage source of the whole network, the current type ITM will not be feasible. First, there is no steady voltage input. Second, current controlled VSI cannot work under open circuit condition. Considering that the load emulators require voltage input, it will be very difficult to start up the whole HTB system. In addition, SGs are designed to have small output impedance, which is beneficial for microgrid stability when the emulators/converters are controlled as voltage sources [94]. Therefore, a voltage type ITM with the voltage source SG model is necessary. In this case, the SG model, opposite from the current type, takes current as input and voltage as output, as shown in Fig. 3-7.

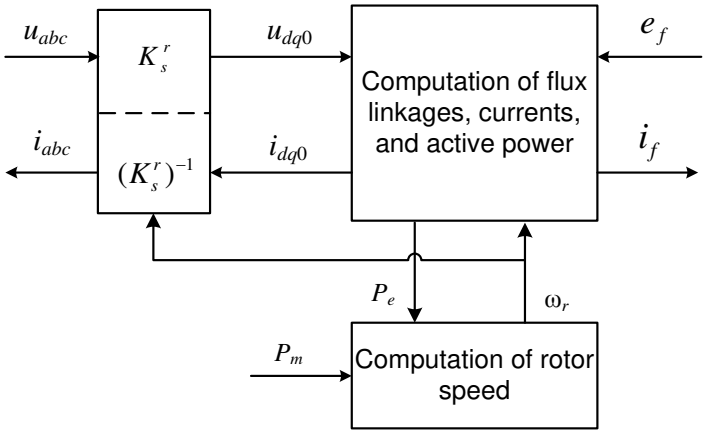


Fig. 3-6. Simulation of an SG in rotor reference frame with voltage as input from [83].

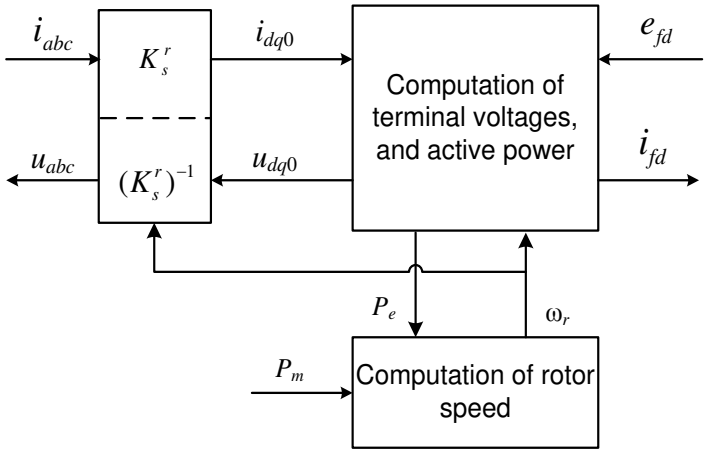


Fig. 3-7. Simulation of an SG in rotor reference frame with current as input.

But this also brings up another challenge: the calculation of the transformer voltages $\dot{\psi}_d$ and $\dot{\psi}_q$ in the stator equations of the SG circuit model. To avoid the computation of the derivative part, an external equivalent inductor is placed at the terminal of the voltage source in [86], a small parasitic resistive load is included at the terminals of the current type SG model in [31], the load impedance is estimated through the RMS values of the terminal voltage and current in [52], and the derivative is neglected in [51]. In fact, the transformer voltages are often neglected in large-scale power system analysis in order to simplify calculation [81]. In addition, the rotor speed is assumed be 1 p.u since the frequency deviation is very small. Based on the above assumptions, the derived 2nd-7th order SG models with operational parameters are widely applied.

3.3 Converter Control Design

The voltage controller can be either open-loop or closed-loop. The open-loop control is a very common choice in SG emulators with VSCs because of its simplicity. In [54], the output inductor is used to represent the stator inductance, and the converter works as back EMF. However, converters are never ideal voltage sources. They are non-linear and also have time delays. A typical

average time delay in a converter is one and a half switching cycles. Assuming that the switching frequency is 10 kHz, the 1.5 cycle time delay will cause a 3.24° phase shift in steady state, which cannot be ignored compared with SG parameters. On the contrary, closed-loop control can achieve unity closed-loop gain and compensate the time delay in the frequency range of interest. Since the primary goal of [54] was not to ensure the accuracy of the emulation, the problem was not mentioned. On the other hand, due to the structure of the HTB, where converters are connected in both the AC and DC side, it provides a path for zero sequence circulating current. The circulating current consists of two parts, where one part contains mainly switching frequency components. When the parallel converters have the same modulation waveform but unsynchronized carrier waveforms, the switching positions of the converters will be different, which results in a different closed path between the converters when they have a common DC link. The other part is the long time period current caused by the non-identical converter parameters. Although the circulating current does not affect the control objectives, it will cause current distortion and unbalance. A good way to eliminate the long term circulating current is to add a zero sequence current controller [82]. In conclusion, closed-loop voltage control is necessary in the development of an SG emulator in the HTB.

The closed-loop control design of a three-phase VSC in PHIL is slightly different from other applications such as grid-connected distributed energy sources (DERs), UPS systems, motor drives, etc. In these applications, most controllers are designed according to the classic gain margin and phase margin based control theory. However, the converter model and control loop in PHIL systems are embedded in the original system loop, thus largely influencing the system behavior and emulation accuracy. Although several papers have discussed the IA or VSC filter structure's

impact on the emulation accuracy, no one has systematically addressed voltage control loop design method in PHIL applications [48][58].

3.4 Verification Method

Verification of a PHIL system can be performed in many different ways. The most widely used method is to visually inspect the emulator output waveforms. In [31] and [42], the emulator output waveforms are compared with real equipment. The problem with this method is that the accuracy of the emulation is also related to the model and parameters in use, and it is difficult to determine the major source of the discrepancy. In [43] and [44], the calculated current inside the motor emulator is compared with the real motor connected to the same bus. This method only investigates the validity of the motor model calculation, and the converter influence on the closed-loop system is not mentioned. The actual output current of the load emulator is compared with its current reference in [66] and [67]. As mentioned above, comparison between the reference and actual output of the emulator does not give any useful information. In addition to the inspection of the output waveforms, verification can also be done through the comparison between the measured and simulated original output impedance in the frequency domain [53].

In [90], the steady-state power transfer limit of a PHIL system influenced by time delay is studied. References [59] and [60] utilized wavelet theory to analyze the difference between the emulation and the original system waveforms. Although the two methods provide quantitative results, the obtained error is still a mix of many uncertain or inaccurate factors, such as model parameters. In the above comparison waveforms, the error can be caused by the inaccurate modeling of the HTB parameters or the improper converter control design. Therefore, the influence of the VSI to the whole system has to be investigated thoroughly and separately from the other sources of error.

One effective way to quantitatively evaluate the discrepancy caused by converters is the transparency based method [97]. This method is widely used in bilateral teleoperation systems in robotics. It compares the output impedances of the PHIL system and the original system. Higher transparency indicates smaller error in emulation. However, this method only considers the open loop performance of the PHIL system. Since the load model also contributes to the behavior of system voltage and current, a closed-loop inspection is necessary. To solve this problem, a transfer function perturbation (TFP) based error model is proposed by W. Ren et al. [57][58][95]. The basic idea is to evaluate the difference between the PHIL system and the original system by the relative error between their closed-loop frequency domain responses. This method involves all the information needed to perform a thorough performance evaluation under different loads. Nevertheless, references [57] and [58] only investigate the error on amplitudes at a specific frequency, while the characterization of a system is represented by the aggregation of data on magnitude and phase over a certain frequency range. As a conclusion, the relative error on both magnitude and phase should be calculated over a certain frequency range.

3.5 Performance Target

Even though PHIL has been studied by several people, the performance target still remains unclear. Since the accuracy and performance of a PHIL system is hard to quantify, as discussed in 3.4, most of the previous work stopped after a visual comparison is given and the results roughly match. One exception is given in [96], where a specific requirement is provided by the IEC 61400-21 standard about the voltage sags in emulating grid faults. As demonstrated in Fig. 3-8, the standard posts a limit on the steady state and dynamic performance of the voltage output. Assume that the frequency domain characteristics of the developed grid emulator can be represented by a typical second order system as shown in (3-2). In order to satisfy the requirement, i.e. less than

10% overshoot and 20 ms rising time, a damping ratio $\xi = 0.59$ and the cutoff frequency $\omega_n = 159$ rad/s.

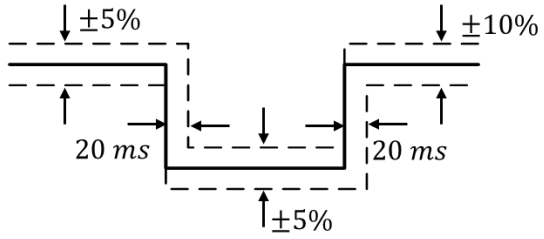


Fig. 3-8. Tolerance for fault ride through voltage sags in emulating grid fault according to IEC 61400-21 standard.

$$G(s) = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{3-2}$$

The step response of the above system in time domain is shown in Fig. 3-9. The TFP based error is then applied to the system to give a deeper and better sense of the correspondence between the error and the dynamic performance in time domain.

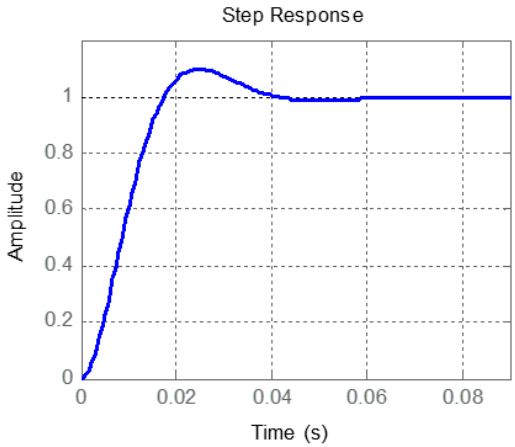


Fig. 3-9. Step response of the designed second order system in (3-2).

Assume that the original system is ideal, meaning its transfer function is unity over the whole frequency domain. The TFP based relative error between G(s) and the original system over a frequency range from 0 to 60 Hz on magnitude is calculated as 47%.

To compare with the above result, 13% relative error at 60 Hz and 94% at 300Hz is achieved in [58], and 0.0414 absolute error (8.83% relative error) at 60 Hz is achieved in [48]. The converter switching frequency in [58] and [96], 1 kHz and 2.5 kHz respectively, is much lower than the 10 kHz in [48] and the HTB, which is the main cause of larger error.

In this work, since the high switching frequency in the HTB can guarantee large enough system bandwidth, a challenging target is set to be 5% TFP based error on both magnitude and phase over frequency range of interest including fault conditions. To achieve is target, the control loop and parameters will be carefully designed, and the major cause of errors will be investigated thoroughly.

3.6 Multi-SG Emulation System Stability

Interaction between multiple or even a large aggregation of SGs is an important research area in power systems. As mentioned in chapter 2, the HTB now has a three-area structure with four interconnected SGs. As discussed previously, the converter and its control will cause error and thus interfere with the whole system's performance. In some cases, even though the control design can guarantee enough stability margin and accuracy, the interconnection of multiple SG emulators may still cause unpredictable stability issues. Since all the previous PHIL systems were designed for testing single equipment, there are no known publications concerning issues with parallel SG emulators or even PHIL systems.

On the other hand, stability issues with interconnected converters, such as in microgrid and DC distribution systems, are well studied. Generally, there are two methods to analyze the stability.

One way is to establish the state-space model of the whole system and analyze eigenvalues [98]. This method is widely used in studying microgrids. The dominant eigenvalues are usually related to higher level control parameters such as droop or other current sharing algorithms, which can be then used to guide the design. The problem with this method is that it is mostly applied to study the impact of low bandwidth controllers, and the effect of the time delay is not taken into consideration. The other way is the impedance based stability criterion [94]. This method is widely applied in DC distribution systems [99] and was recently used to analyze three-phase systems with distributed generation (DG) [100]-[103]. The basic idea of the impedance based method is to compare the output impedance of a DG and the input impedance of the rest of the system at the connecting point. The ratio of the impedances must satisfy the Nyquist stability criterion. This method enables various applications of virtual impedance such as oscillation damping, power sharing, and so on [103]. It also focuses more on the converter inner loop design instead of higher level/outer loop, which meets the research purpose in this work – investigating the voltage control loop influence on the stability of a multi-SG emulation system.

3.7 Research Objectives and Approaches

The objective of this research is to develop a synchronous generator emulator with less than 5% TFP error within the frequency range of interest including the symmetrical fault condition. Corresponding to the challenges discussed in this chapter, the research approaches are listed as follows:

1. The design targets of the voltage controller for the converter interface is established based on the 4^{th}-order SG model, and the main factors that influence the emulator accuracy are investigated. A single voltage control loop with current feed-forward is proposed to minimize the error caused by the converter interface in chapter 5.

2. Visual inspection of the experimental and simulation results is adopted preliminarily to verify the developed SG emulator. TFP based error evaluation method on both amplitude and frequency response is then applied to quantitatively evaluate the error caused by the converter interface. The factors that influence the error are discussed and verified by simulation or experiment. At the same time, the influence of the error on the generator closed loop control system such as the excitation system is researched. The evaluation method and results are given in chapter 6.

3. Synchronization method of a generator emulator is proposed in order to form a multi-generation system. At the same time, the stability issue associated with the interconnection of two SG emulators is studied. The small signal models of the two-generation system with constant current and constant impedance load are developed, and the main reasons that cause instability are researched and verified. The developed SG emulator is also verified in the two-area system by comparing the system dynamics visually.

4. To fully expand the capability of the developed SG emulator, the 6^{th}-order SG model including transformer voltages and saturation effect is applied in a three-phase symmetrical short-circuit fault scenario. Control parameters are designed based on the TFP error evaluation of the fault condition, and proper parameters are selected to achieve the performance target. The developed SG emulator is then tested and verified in line-to-line fault conditions. In addition, the stability of the new SG emulator is studied again and compared with the previous emulation.

4 Synchronous Generator Model

In this chapter, the behavior of a synchronous generator with different models is studied and compared. The numerical methods for computing the SG electric model in real-time are discussed.

4.1 Electrical Model

SG models have been established in many books [81][83]. The models in this research are based on the following assumptions:

1) The stator windings are sinusoidally distributed along the air-gap.
2) The stator slots cause no serious variation of the rotor inductance with rotor position.
3) Magnetic hysteresis is negligible.
4) Magnetic saturation is neglected.

The classical SG model transforms stator components onto rotor reference frame, as defined by (4-1), where the quadrature axis is leading the direct axis by 90 degrees.

$$K_s^r = \frac{2}{3}\begin{bmatrix} cos\omega_r t & \cos\left(\omega_r t - \frac{2\pi}{3}\right) & \cos\left(\omega_r t + \frac{2\pi}{3}\right) \\ -sin\omega_r t & -\sin\left(\omega_r t - \frac{2\pi}{3}\right) & -\sin\left(\omega_r t + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{4-1}$$

Per unit stator voltage equations:

$$u_d = p\psi_d - \psi_q\omega_r - R_a i_d \tag{4-2}$$
$$u_q = p\psi_q + \psi_d\omega_r - R_a i_q$$
$$u_0 = p\psi_0 - R_a i_0 \tag{4-3}$$

Per unit rotor voltage equations:

$$e_{fd} = p\psi_{fd} + R_{fd}i_{fd} \tag{4-4}$$

$$0 = p\psi_{1d} + R_{1d}i_{1d} \tag{4-5}$$

$$0 = p\psi_{1q} + R_{1q}i_{1q} \tag{4-6}$$

$$0 = p\psi_{2q} + R_{2q}i_{2q} \tag{4-7}$$

Per unit stator flux linkage equations:

$$\psi_d = -(X_{ad} + L_l)i_d + X_{ad}i_{fd} + X_{ad}i_{1d} \tag{4-8}$$

$$\psi_q = -\left(X_{aq} + X_l\right)i_q + X_{aq}i_{1q} + X_{ad}i_{2q} \tag{4-9}$$

$$\psi_0 = -X_0 i_0 \tag{4-10}$$

Per unit rotor flux linkage equations:

$$\psi_{fd} = X_{ad}i_{fd} + X_{ad}i_{1d} - X_{ad}i_d \tag{4-11}$$

$$\psi_{1d} = X_{ad}i_{fd} + X_{11d}i_{1d} - X_{ad}i_d \tag{4-12}$$

$$\psi_{1q} = X_{11q}i_{1q} + X_{aq}i_{2q} - X_{aq}i_q \tag{4-13}$$

$$\psi_{2q} = X_{aq}i_{1q} + X_{22q}i_{2q} - X_{aq}i_q \tag{4-14}$$

Per unit air-gap torque:

$$T_e = \psi_d i_q - \psi_q i_d \tag{4-15}$$

where *p* denotes differential operator *d*/*dt*.

The above reactances and resistances of the stator and rotor circuits are called fundamental or basic parameters. In reality, those parameters cannot be determined directly from measurements or tests. Therefore, operational parameters are obtained through certain tests and then used for representing machine characteristics. Many literatures have discussed the relationship between fundamental parameters and operational parameters, such as [81] and [83].

In practice, the speed voltages $\psi_d\omega_r$ and $\psi_q\omega_r$ due to flux change in space are the dominant components of the stator voltage. Under steady-state conditions, the transformer voltages $p\psi_d$ and

$p\psi_q$ due to flux change in time are equal to zero. In most cases, the transformer voltages can be neglected without causing significant errors. In the analysis of a three-phase short-circuit at the terminals of an SG, the transformer voltage is usually neglected in order to eliminate the dc offset in the phase current. Therefore, in order to simplify numerical calculation, the derived 2nd through 7th order models of the synchronous generator are based on two important assumptions:

1. The stator transients are neglected so that the model becomes algebraic equations: $p\psi_d$ and $p\psi_q$ are assumed to be 0.

2. The rotor speed is assumed to be 1 p.u so that the model becomes linear.

In the fourth-order model, as shown in (4-16), the damping winding on the *d* axis and the second damping winding on the *q* axis are neglected. This simplified model only considers the transient components, and is widely used in large-scale power system stability calculations. Sometimes, this model is further simplified by neglecting stator resistance.

$$\begin{aligned} u_d &= E'_d + X'_q i_q - R_a i_d \\ u_q &= E'_q - X'_d i_d - R_a i_q \\ T'_{qo} p E'_d &= -E'_d + (X_q - X'_q) i_q \\ T'_{do} p E'_q &= e_{fd} - E'_q - (X_d - X'_d) i_d \end{aligned} \tag{4-16}$$

In the more complicated sixth-order model, only zero sequence signals are not taken into consideration. In the HTB at the CURENT, because of the common mode choke installed in series with the converters, zero sequence components cannot exist. The transient parameters and variables have the same definition as the fourth-order model.

$$
\begin{aligned}
u_d &= E_d'' + X_q'' i_q - R_a i_d \\
u_q &= E_q'' - X_d'' i_d - R_a i_q \\
T_{qo}' p E_d' &= -\frac{X_q - X_l}{X_q' - X_l} E_d' + \frac{X_q - X_q'}{X_q' - X_l} E_d'' + \frac{(X_q - X_q')(X_q'' - X_l)}{X_q' - X_l} i_q \\
T_{do}' p E_q' &= e_{fd} - \frac{X_d - X_l}{X_d' - X_l} E_q' + \frac{X_d - X_d'}{X_d' - X_l} E_q'' - \frac{(X_d - X_d')(X_d'' - X_l)}{X_d' - X_l} i_d \\
T_{qo}'' p E_d'' &= \frac{X_q'' - X_l}{X_d' - X_l} T_{qo}'' p E_d' - E_d'' + E_d' + (X_q' - X_q'') i_q \\
T_{do}'' p E_q'' &= \frac{X_q'' - X_l}{X_d' - X_l} T_{do}'' p E_q' - E_q'' + E_q' - (X_d' - X_d'') i_d
\end{aligned}
\tag{4-17}
$$

Assume that the excitation voltage e_{fd} is constant during the small signal time step, and the rotor speed in the fundamental/circuit mode is 1 p.u. The linearized generator models, based on the above fundamental/circuit model, 4th order, and 6th order model, can be summarized in the following form,

$$
\begin{aligned}
\begin{bmatrix} \Delta u_d \\ \Delta u_q \end{bmatrix} &= [G_{gf}] E_{fd} - [Z_g] \begin{bmatrix} \Delta i_d \\ \Delta i_q \end{bmatrix} \\
[G_{gf}] = \begin{bmatrix} G_{gfd} \\ G_{gfq} \end{bmatrix}, [Z_g] &= \begin{bmatrix} Z_{gdd} & Z_{gdq} \\ Z_{gqd} & Z_{gqq} \end{bmatrix}
\end{aligned}
\tag{4-18}
$$

where $[Z_g]$ is termed as the SG output impedance on *dq*-axis.

The frequency domain responses of $[Z_g]$ in different models with the rescaled parameters shown in Table 4-1 are compared in Fig. 4-1 to Fig. 4-3. Clearly, the major difference between the circuit model, described in (4-2) to (4-11), and the derived models is the inclusion of the transformer voltage, which is represented by an inductive impedance on Z_{gdd} and Z_{gqq}. For Z_{gdq} and Z_{gqd}, the circuit model and the 6th order model overlaps with each other, while the 4th order model presents a slight difference. Considering that the subtransient dynamics are mostly related with faults, the 4th order model is adequate in normal operating conditions and will be used for preliminary SG emulation.

Table 4-1. Generator parameters before and after rescaling.

Name	Original	Rescaled
P_{gen}	900 MVA	15 kVA
V_{gen}	20 kV	208 V
f_{base}	60 Hz	60 Hz
X_d	1.8 p.u	1.8 p.u
X_q	1.7 p.u	1.7 p.u
X_l	0.2 p.u	0.2 p.u
X'_d	0.3 p.u	0.3 p.u
X'_q	0.55 p.u	0.55 p.u
X''_d	0.25 p.u	0.25 p.u
X''_q	0.25 p.u	0.25 p.u
R_a	0.0025 p.u	0.0025 p.u
T'_{d0}	8 s	8 s
T'_{q0}	0.4 s	0.4 s
T''_{d0}	0.03 s	0.03 s
T''_{q0}	0.05 s	0.05 s
H	6.5/6.175 p.u	6.5/6.175 p.u

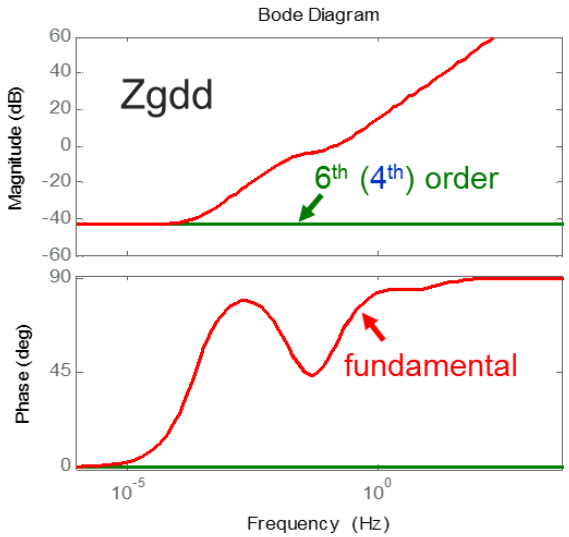


Fig. 4-1. Bode plot of Z_{gdd}/Z_{gqq} in the fundamental/circuit model, 4th order, and 6th order model.

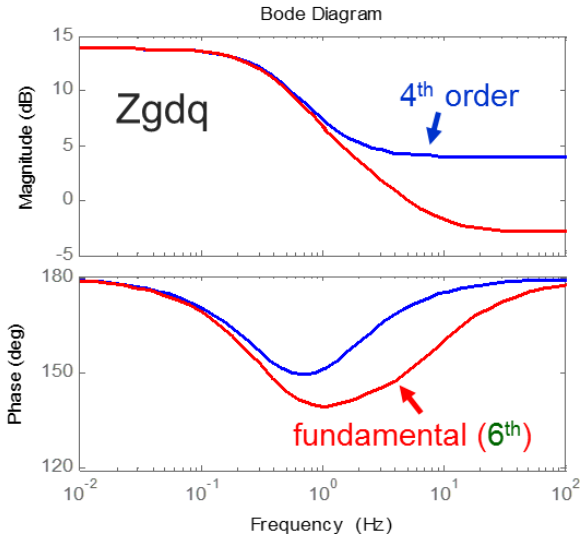


Fig. 4-2. Bode plot of Z_{gdq} in the fundamental/circuit model, 4th order, and 6th order model.

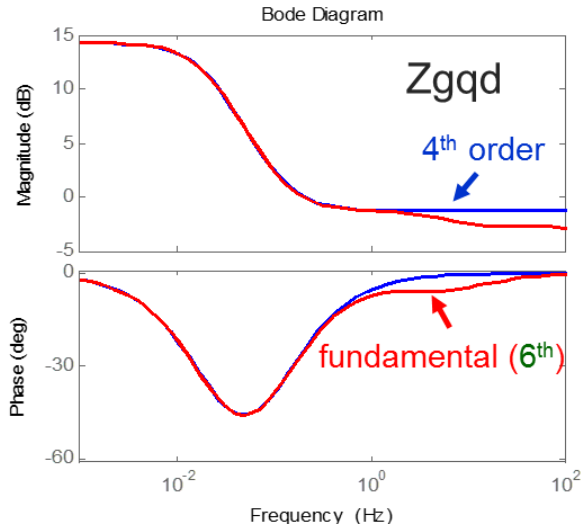


Fig. 4-3. Bode plot of Z_{gqd} in the fundamental/circuit model, 4th order, and 6th order model.

4.2 Mechanical Model

The swing equation of the generator is given as:

$$\begin{aligned} \dot{\delta} &= \Delta\omega_r = \omega_r - \omega_0 \\ \dot{\omega} &= \frac{1}{M}(P_m - P_e - D\omega) \end{aligned} \tag{4-19}$$

where, ω_r is the angular rotor speed in rad/s, ω_0 is its rated value/synchronous speed, $\Delta\omega_r$ denotes the deviation of the rotor speed from synchronism, ω_{ref} is the speed reference, P_m is mechanical power, P_e is electrical power, M is the inertia constant, D is the damping factor caused by mechanical friction. Rotor angle δ is given to Park transformation in the converter based generator emulator to convert the three phase signals onto and back from dq axis. The relationship between inertia constant M and H is given in (4-20) in per unit system, where S_{ng} is generator capacity, P_{base} is the chosen base power.

$$M = \frac{2H}{\omega_s} \cdot \frac{S_{ng}}{P_{base}} \tag{4-20}$$

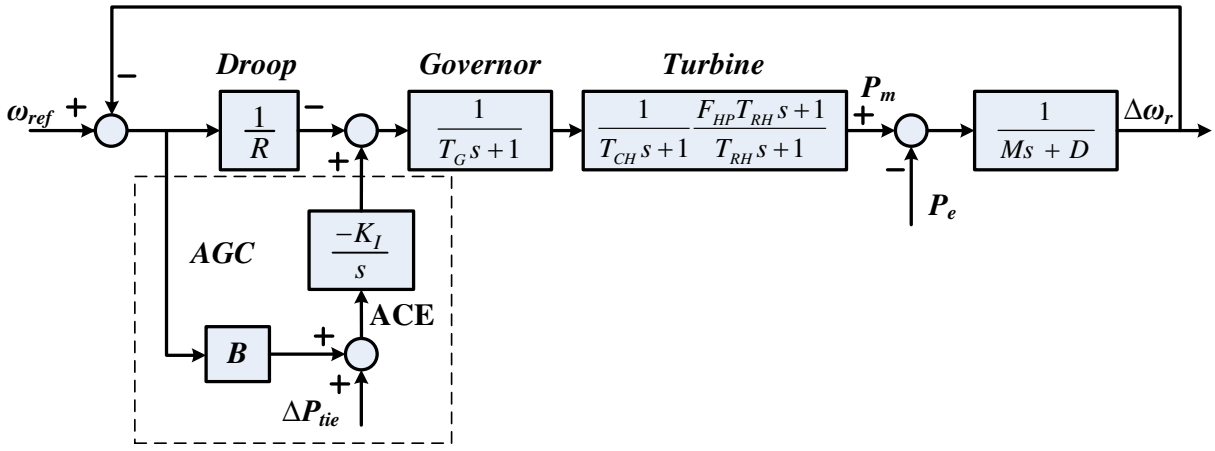


Fig. 4-4. Mechanical model of a steam synchronous generator.

A simplified thermal turbine is chosen to model. Governor, droop control, Automatic Generation Control (AGC), Power System Stabilizer (PSS), and excitation system with Automatic Voltage Regulator (AVR) are also included, as shown in Fig. 4-4 and Fig. 4-5. The control signal combining the frequency deviation and the tie line flow deviation ΔP_{tie} weighted by a bias factor B is called area control error (ACE) [81].

The mechanical model is developed based on the assumption that the generator is running under steady state (synchronism) before a transient process caused by a small disturbance starts. Therefore, a proper controller should be adopted at the startup process of the HTB system, and mechanical part is not connected until steady state is reached.

In the excitation system shown in Fig. 4-5, u_t is generator terminal voltage amplitude, U_{tref} is the reference, K_A and T_e are the gain and time constant of the excitation system. E_{fmax} and E_{fmin}, determined by the reactive power capacity of the generator, are the output boundaries for e_{fd}.

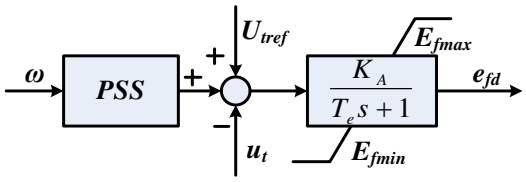


Fig. 4-5. Excitation model of a synchronous generator.

4.3 Numerical Method for Discretization of Synchronous Generator Model

Fourth-order Runge-Kutta (RK4) and implicit trapezoidal methods are two common choices for solving the time dependent differential equations in SG or induction motor model [84][87]. Especially in current type SG model, the stator differential equations are nonlinear when the rotor

speed variation is considered. During fault conditions with large frequency deviation and alternating components on *dq*-axis due to dc offset in three-phase current, improper integration method can easily cause numerical instability. For explicit integration methods, a step size smaller than the smallest time constant in the model is usually required to ensure stability. For example, RK4 requires a step size less than 1/5 of the smallest time constant [84]. On the contrary, the stability boundary of the implicit trapezoidal method is not limited by step size, while with less accuracy compared with RK4.

However, in the voltage type SG model, the nonlinear part of the equations, i.e. speed voltages $\psi_d\omega_r$ and $\psi_q\omega_r$, are no longer involved in integration. The terminal voltages of an SG model can be obtained from the summation of the speed voltages, transformer voltages, and the voltages over stator resistance. This largely lowers the requirement for the integration method. Therefore, implicit trapezoidal method is adopted in this work because of its simplicity and robustness.

4.4 Summary

The behavior of synchronous generators with different models presents small difference, especially in steady-state. The fourth-order model, which includes transient parameters, is adopted preliminarily because of its simplicity. Since the SG model is voltage type, the differential equation is no longer non-linear, and a trapezoidal method is applied for computing the model in real-time.

5 Control Algorithm Design of a Single Generator Emulator

As discussed in chapter 3, improved IAs are needed only when time delay is very large and open loop control is used. Voltage type ITM is selected for SG emulation since the generator is the only voltage source in the HTB system. Closed-loop voltage control is applied to compensate the phase lag caused by time delay in low frequency. The overall diagram of the SG emulator is demonstrated in Fig. 5-1. This chapter discusses the design targets of the voltage controller, and the corresponding design method.

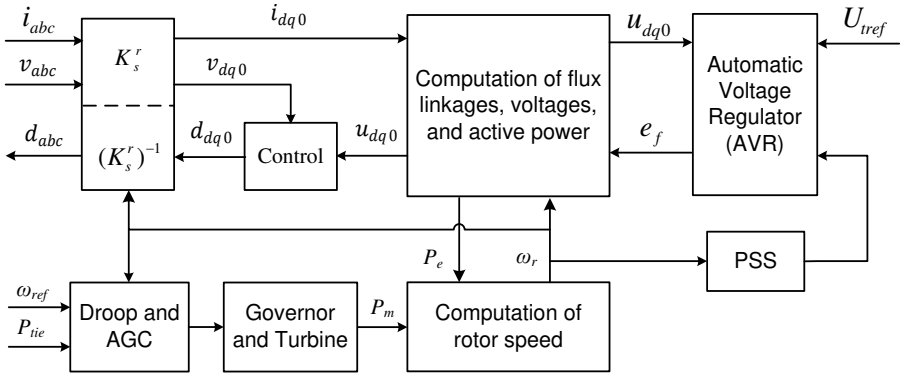


Fig. 5-1. Overall diagram of the developed SG emualtor.

5.1 Control Design Targets

In the fourth order SG model, also called the two-axis model, the damping winding on the d axis and the second damping winding on the q axis are neglected, and the output impedance and G_{gf} is given by (5-1):

$$Z_{gdd} = Z_{gqq} = R_a$$
$$Z_{gdq} = -\frac{X'_q T'_{q0} s + X_q}{T'_{q0} s + 1}, Z_{gqd} = \frac{X'_d T'_{d0} s + X_d}{T'_{d0} s + 1} \tag{5-1}$$
$$G_{gfd} = 0, G_{gfq} = \frac{1}{T'_{d0} s + 1}$$

where X'_d and X'_q are the *d*-axis and *q*-axis transient reactance, T'_{do} and T'_{qo} are termed the *d*-axis and *q*-axis transient open-circuit time constant.

VSIs with the structure shown in Fig. 5-2 generally can be depicted by input/output characteristics as (5-2), where $[\Delta u_{dq}]$ is the converter voltage reference, $[\Delta v_{dq}]$ is the converter output *dq* voltage, $[\Delta i_{dq}]$ is the converter output current, $[G_v]$ is the closed loop voltage gain, and $[Z_c]$ is the converter output impedance.

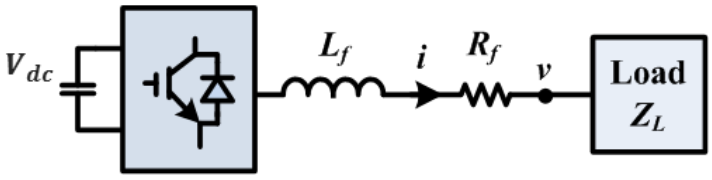


Fig. 5-2. Structure of a VSI in HTB.

$$[\Delta v_{dq}] = [G_v][\Delta u_{dq}] - [Z_c][\Delta i_{dq}] \tag{5-2}$$

Combine (4-18) and (5-2),

$$[\Delta v_{dq}] = [G_v][G_{gf}]E_{fd} - ([G_v][Z_g] + [Z_c])\Delta i_{dq} \tag{5-3}$$

Apparently, the behavior of the converter based generator emulator is now determined by not only the generator model, but also the converter's loop gain and output impedance. In order to make the converter based emulator behave exactly like the model, three requirements in the frequency range of interest need to be achieved according to (5-3):

1) The loop gain G_v should be 1 within the frequency range of interest

2) Controller bandwidth should be larger than the fastest dynamic in an SG model

3) The converter output impedance should be 0, or as small as possible.

As shown in Table 5-1, the smallest time constant in an SG model can be 0.01 s [81]. Thus, the converter voltage control bandwidth then has to be designed larger than 100 Hz to ensure accuracy.

Table 5-1. Typical range of open circuit time constants in hydro and thermal units.

Parameters		Hydro Units	Thermal Units
Transient OC Time Constant	T'_{do}	1.5 – 9.0 s	3.0 – 10.0 s
	T'_{qo}	–	0.5 – 2.0 s
Subtransient OC Time Constant	T''_{do}	0.01 – 0.05 s	0.02 – 0.05 s
	T''_{qo}	0.01 – 0.09 s	0.02 – 0.05 s

5.2 Single Voltage Control Loop

Traditionally, a VSI that controls its output voltage is usually implemented with a LC filter. A cascaded voltage outer-loop and a current inner-loop can be used to control the output voltage. Assume that unity loop gain can be achieved by the inner current closed loop, the controlled plant of the outer voltage loop is known and thus the corresponding compensator can be designed easily. The cascaded control has two benefits: first, the inner current loop imposes a current limiting function to the voltage controlled converter; second, it enlarges the controllable voltage loop bandwidth when using only a PI compensator. However, designing of the voltage compensator in the cascaded controller will be difficult without the filtering capacitor, since the current reference to output voltage transfer function is now solely determined by the load model Z_L.

The small signal model of the above VSI on the rotor reference frame is demonstrated in Fig. 5-3, where Z_L is the load impedance, $F_V(s)$ is the first order low pass filter (LPF) with the cutoff frequency ω_V on the voltage sensing path.

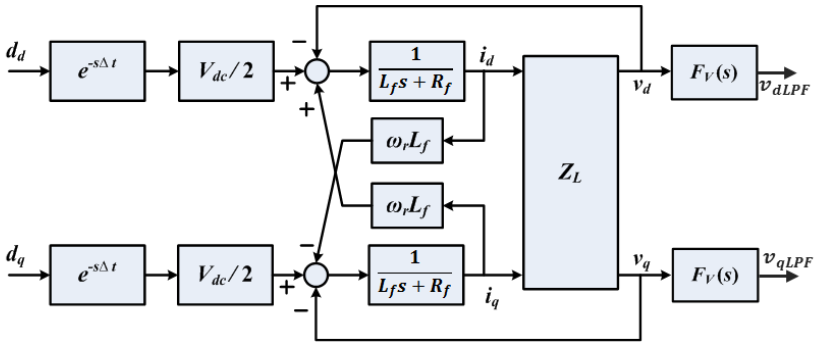


Fig. 5-3. VSI model on *dq*-axis.

The *d*-axis voltage to output transfer function is given by:

$$\left.\frac{\Delta v_{dLPF}}{\Delta d_d}\right|_{\Delta d_q=0} = \frac{V_{dc}}{2}\frac{Z_L e^{-s\Delta t}F_v}{L_f s + R_f + Z_L} \tag{5-4}$$

The output filter inductance L_f of a three-phase converter is normally designed to be small enough to have minimum voltage drop and reactive power, while limiting the current ripple. In the CURENT HTB, $L_f = 0.5$ mH, corresponding to 0.065 p.u. Thus, (5-4) can be rewritten as (5-5) with L_f and R_f ignored compared to large load impedance.

$$\frac{\Delta v_{dLPF}}{\Delta d_d} = \frac{V_{dc}}{2}e^{-s\Delta t}F_v \tag{5-5}$$

The simplified transfer function of the control plant is independent from the load impedance, and a single PI controller with unified parameters can be designed and applied for most loading conditions. To verify this assumption, the bode plot of (5-4) with varying loads and (5-5) are shown

in Fig. 5-4. Only resistive and/or inductive loads are considered since they are the major load in power grids. Apparently, when the load is RL type, (5-4) can be represented by (5-5) with very small error. When the load is purely resistive, (5-4) can be represented by (5-5) when the resistance is large under low and medium frequency range.

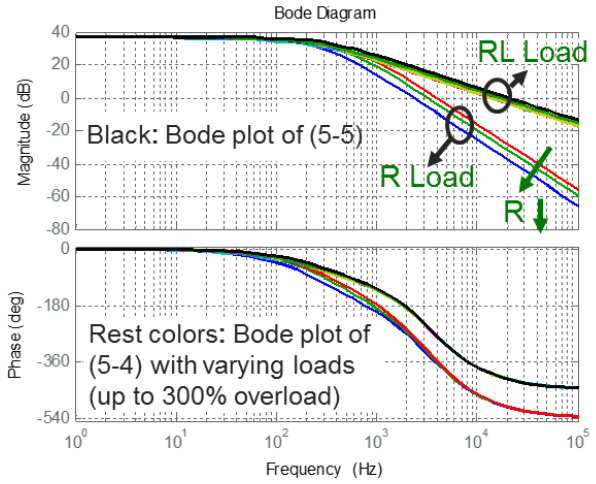


Fig. 5-4. Bode plots of (5-4) with varying loads and (5-5).

The block diagram of the converter and its voltage control on *d*-axis is then demonstrated in Fig. 5-5. The VSI model (5-2) can be expressed in detail in (5-6).

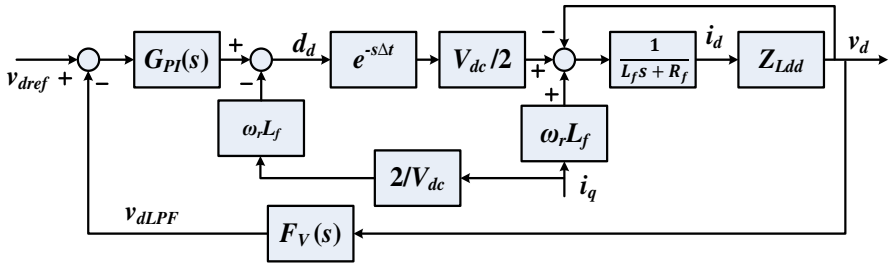


Fig. 5-5. Block diagram of the converter with single voltage control loop on *d*-axis.

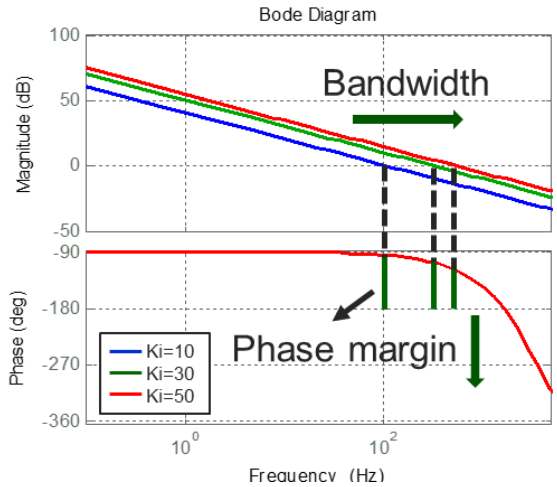
$$\begin{bmatrix}\Delta v_d\\ \Delta v_q\end{bmatrix}=\begin{bmatrix}G_{vd} & 0\\ 0 & G_{vq}\end{bmatrix}\begin{bmatrix}V_{dref}\\ V_{qref}\end{bmatrix}-\begin{bmatrix}Z_{cdd} & Z_{cdq}\\ Z_{cqd} & Z_{cqq}\end{bmatrix}\begin{bmatrix}\Delta i_d\\ \Delta i_q\end{bmatrix} \tag{5-6}$$

where

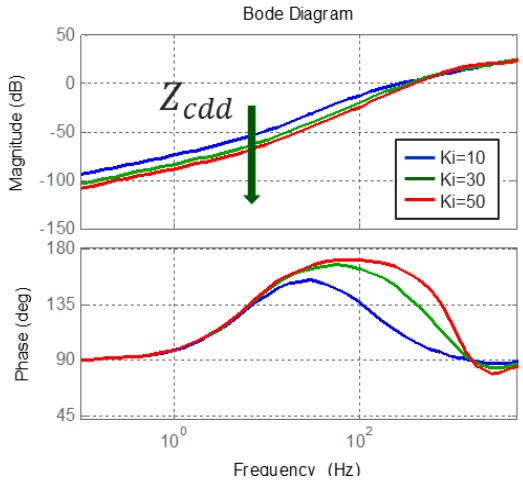
$$\begin{aligned}G_{vq}=G_{vd}&=\left.\frac{\Delta v_d}{V_{dref}}\right|_{\substack{\Delta i_d=0\\ \Delta i_q=0}}=\frac{\frac{V_{dc}}{2}G_{PI}(s)e^{-s\Delta t}}{1+\frac{V_{dc}}{2}G_{PI}(s)F_V(s)e^{-s\Delta t}}\\ Z_{cqq}=Z_{cdd}&=\left.\frac{\Delta v_d}{\Delta i_d}\right|_{\substack{\Delta i_q=0\\ V_{dref}=0}}=\frac{L_f s+R_f}{1+\frac{V_{dc}}{2}G_{PI}(s)F_V(s)e^{-s\Delta t}}\\ -Z_{cqd}=Z_{cdq}&=\left.\frac{\Delta v_d}{\Delta i_q}\right|_{\substack{\Delta i_d=0\\ V_{qref}=0}}=\frac{(e^{-s\Delta t}-1)\omega_r L_f}{1+\frac{V_{dc}}{2}G_{PI}(s)F_V(s)e^{-s\Delta t}}\end{aligned} \tag{5-7}$$

The PI controller has the form $G_{PI}(s)=\frac{K_i(K_p s+1)}{s}$. Design $K_p=0.00027$ to cancel the pole in the LPF $F_V(s)$. The open-loop transfer function of the PI controller and the control plant described in Fig. 5-5 is demonstrated in Fig. 5-6 (a). With increasing K_i, the system bandwidth increases while the phase margin decreases. At the same time, larger system bandwidth results in smaller converter output impedance amplitude, as shown in Fig. 5-6 (b) and (c).

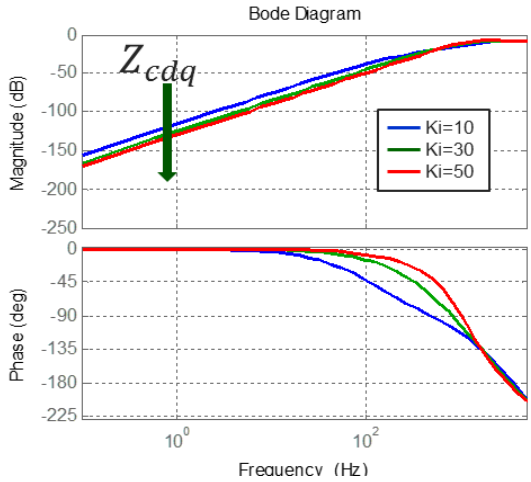
In order to achieve the converter control goals mentioned above, i.e. small converter output impedance, the PI controller parameters should be large enough. But they should also be small enough to leave plenty of phase margin. The problem then rises about how large the PI controller parameters should be and is the single voltage control loop adequate to achieve the performance target.



(a) Bode plot of the open loop transfer function including PI control and the control plant.



(b) Bode plot of converter output impedance Z_{cdd}.



(c) Bode plot of converter output impedance Z_{cdq}.

Fig. 5-6. Converter open loop transfer function and output impedance with different K_i.

5.3 Controller Performance Evaluation

The overall block diagram of an SG emulator in *dq*-axis is shown in Fig. 5-7, where the coupling and decoupling of the filter inductor are not included.

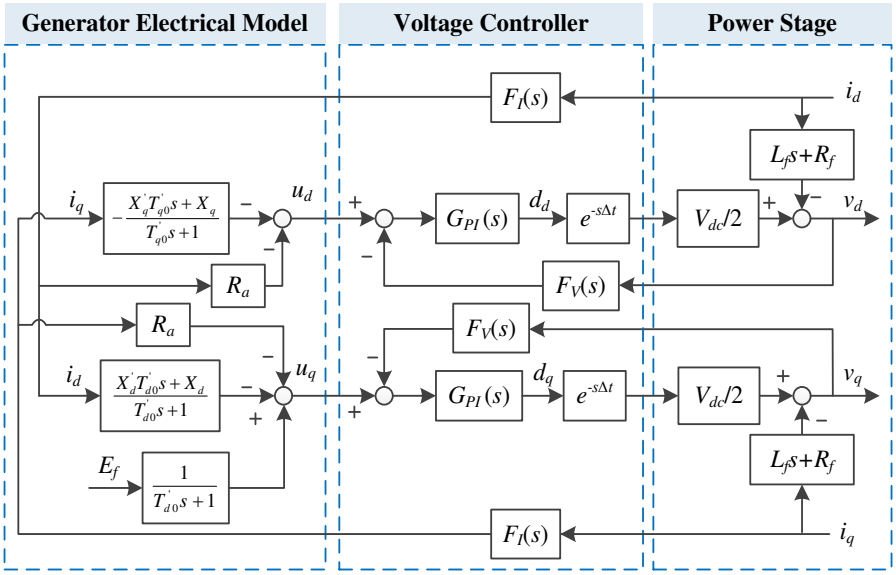
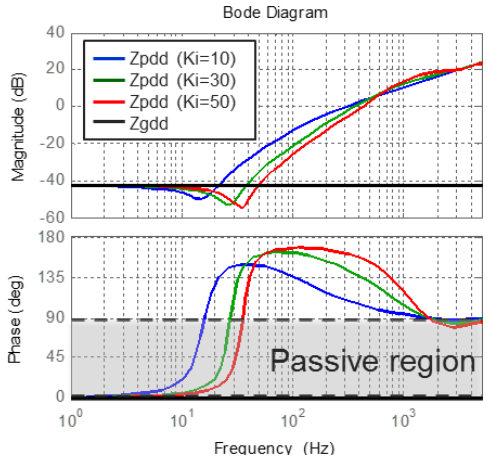
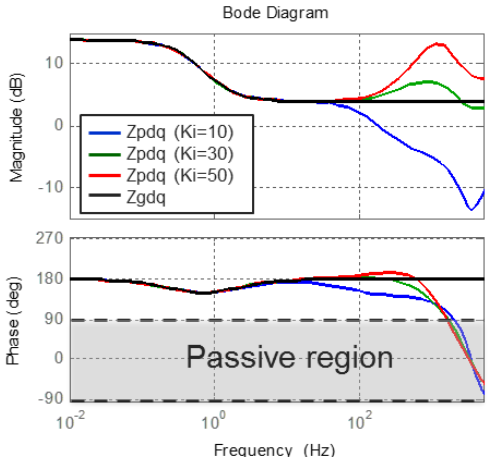


Fig. 5-7. Overall block diagram of an SG emulator

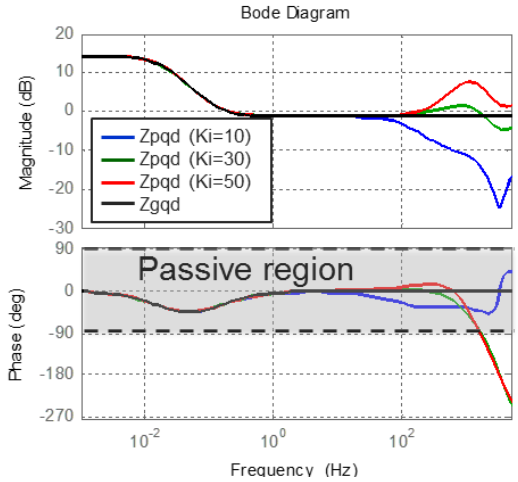
Define the output impedance of an SG emulator $[Z_p] = [G_v][Z_g] + [Z_c]$, as described in (5-3), and plot the bode diagram of $[Z_p]$ and $[Z_g]$ in Fig. 5-8 with the parameters in Table 4-1. Taking Z_{pdd} and Z_{pdq} as examples, Z_{pdd} approximates Z_{gdd} in magnitude with less difference with the increase of control parameters, but with larger difference on phase, whereas for Z_{pdq} error on amplitude increases both when control parameters are too small or too large. That means, PI parameters cannot increase indefinitely.



(a) Bode plot of Z_{pdd} with varying PI parameters and Z_{gdd}.



(b) Bode plot of Z_{pdq} with varying PI parameters and Z_{gdq}.



(c) Bode plot of Z_{pqd} with varying PI parameters and Z_{gqd}.

Fig. 5-8. Bode plot of $[Z_p]$ and $[Z_g]$.

Furthermore, the deviation in Z_{pdq} starts from converter control cutoff frequency, while the deviation in Z_{pdd} starts at a much lower frequency. Since the SG impedance Z_{gdd} is very small in this case, the emulator output impedance Z_{pdd} is dominated by the converter output impedance Z_{cdd}. As defined in (5-7), the amplitude of Z_{cdd} is also a factor of the filter inductance and resistance, which contributes to the discrepancy on Z_{pdd} within the control bandwidth.

A current feed-forward loop is thus designed to eliminate the error caused by the voltage drop on the filter inductor, as demonstrated in Fig. 5-9. L_{fc} and R_{fc} are the compensation value of the filter inductance and resistance. F_I is the first order current filter with a cutoff frequency of 5 kHz. The converter output impedance Z_{cdd} is then rewritten as (5-8), while Z_{cdq}, Z_{cqd}, and G_v stay unchanged.

$$Z_{cdd} = \frac{L_f s + R_f - \left(L_{fc} s + R_{fc}\right) F_I(s) e^{-s\Delta t}}{1 + \frac{V_{dc}}{2} G_{PI}(s) F_V(s) e^{-s\Delta t}} \tag{5-8}$$

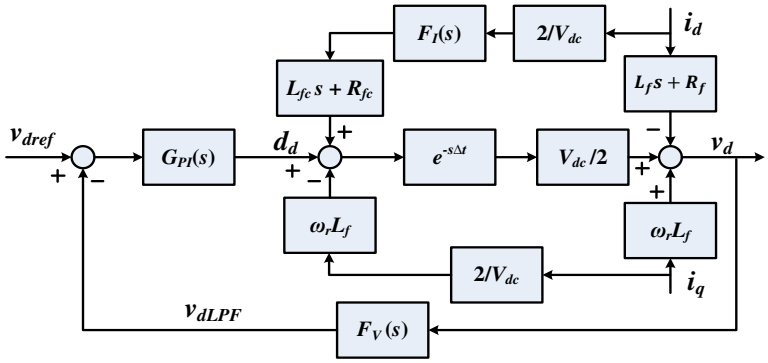
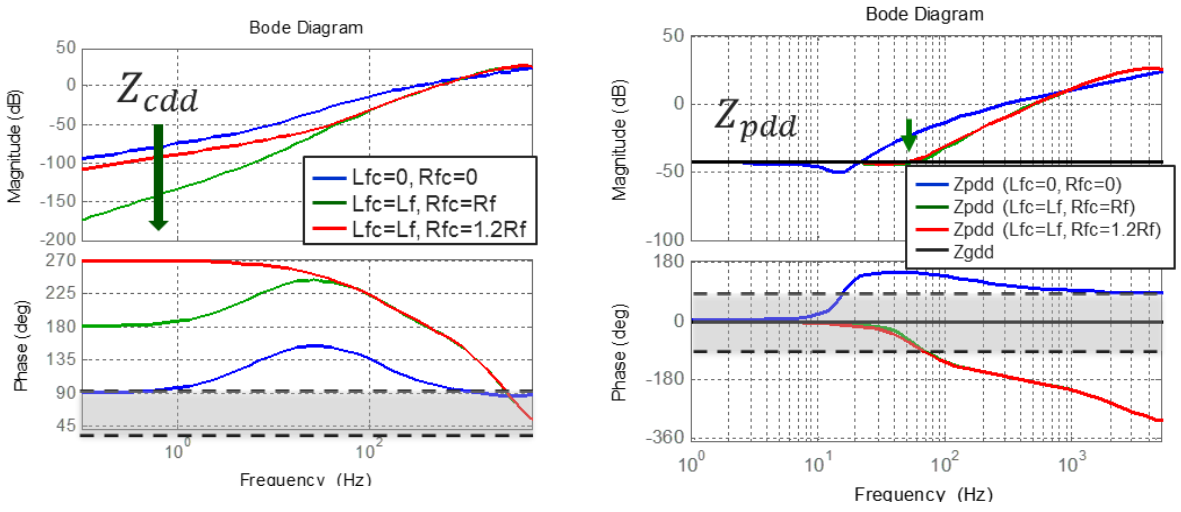


Fig. 5-9. Block diagram of the converter control on *d*-axis.

The bode plots of Z_{cdd} with different L_{fc} and R_{fc} are shown in Fig. 5-10 (a). When $L_{fc} = 0$ and $R_{fc} = 0$, Z_{cdd} has the same form as (5-7). Apparently, the best effect can be achieved by making $L_{fc} = L_f$ and $R_{fc} = R_f$, where the current feed-forward compensates the voltage drop on the converter output filter. This feed-forward can largely decrease the magnitude of Z_{cdd} even when the compensation value is different from the filter inductor parameter. In this way, the corresponding error between Z_{pdd} and Z_{gdd} is reduced significantly within the control bandwidth, as demonstrated in Fig. 5-10 (b), where $K_i = 10$. But at the same time, the current feed-forward also moves the phase response in Z_{cdd} further away from the passive region (-90° to 90°), which makes the converter more prone to instability under certain capacitive loads, especially with large capacitance, compared with the control without the feed-forward.



(a) Z_{cdd} with different L_{fc} and R_{fc}. (b) Z_{pdd} with different L_{fc} and R_{fc} and Z_{gdd}.

Fig. 5-10. Bode plots of Z_{cdd} and Z_{pdd}.

To verify the effectiveness of the current feed-forward, comparative experiments have been conducted with the structure as shown in Fig. 5-11. Inverter 1 is implemented with voltage control discussed above, and Inverter 2 works as a current source. In case 1, $L_{fc} = 0$ and $R_{fc} = 0$, while $L_{fc} = 0.6 \times 10^{-3}$ and $R_{fc} = 0$ in case 2. Under the same load current step, inverter 1 output voltage *V* has a smaller sag in case 2 than in case 1, as shown in Fig. 5-12 (a) and (b). At the same time, voltage and current data on *dq*-axis during the current step are obtained from the DSP with 10 kHz sampling, as shown in Fig. 5-12 (c) and (d). Detailed voltage signals on *dq*-axis during the load step transient are demonstrated in Fig. 5-12 (e) and (f). Since the filter inductance is already very small and the current step is not very large, the effect of the current feed-forward is obvious but not significant. However, under large load step, especially in the fault condition, it will play an important role in shaping the emulator behavior.

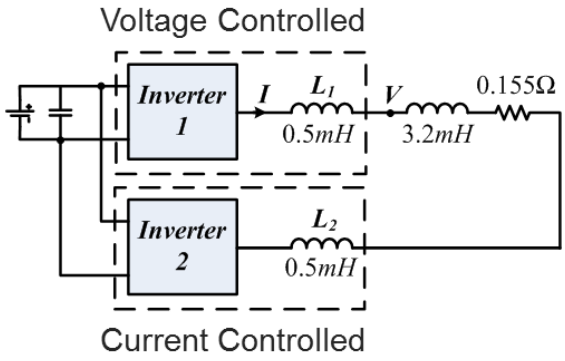
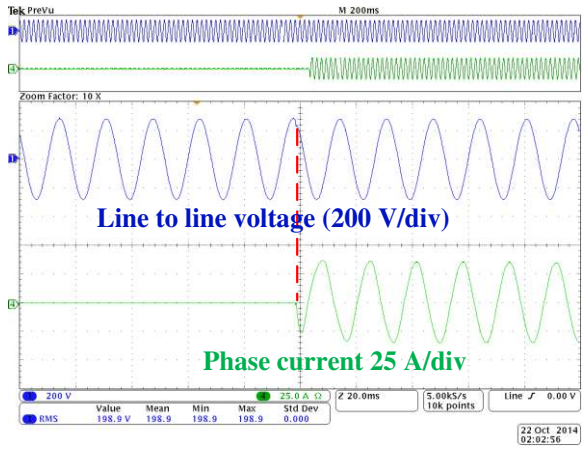
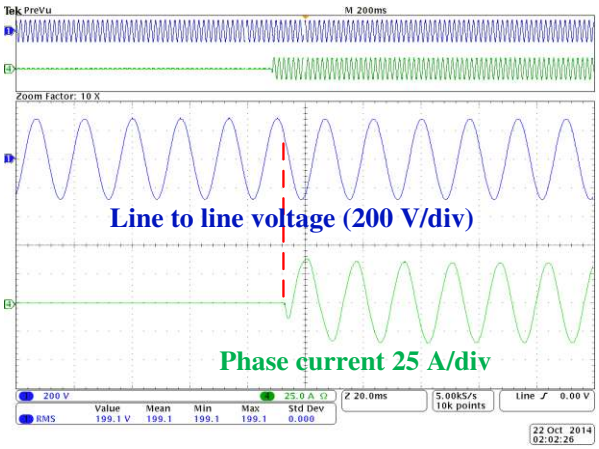


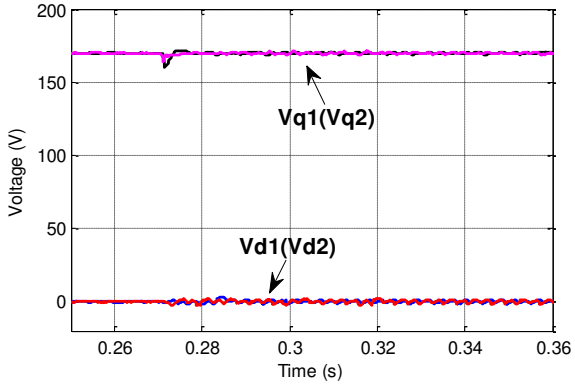
Fig. 5-11. Experiment layout with the VSI implemented with the voltage control loop.



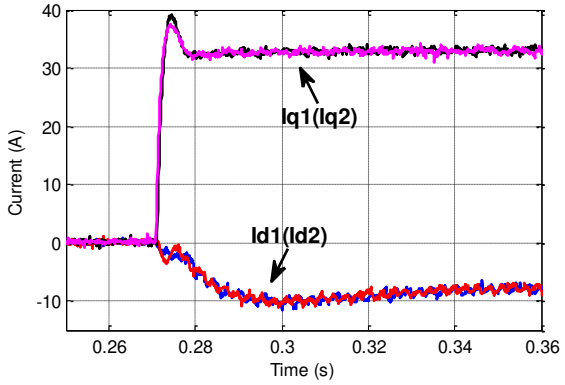
(a) Line voltage and phase current without current feed-forward.



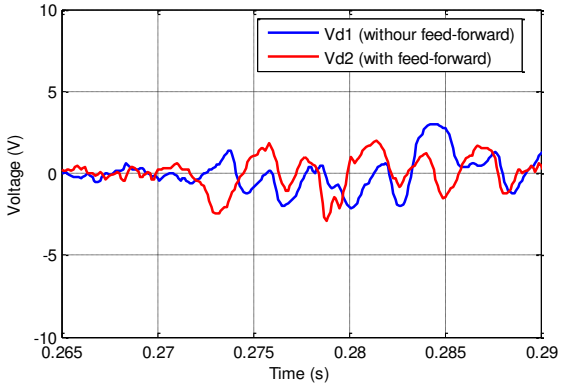
(b) Line voltage and phase current with current feed-forward.



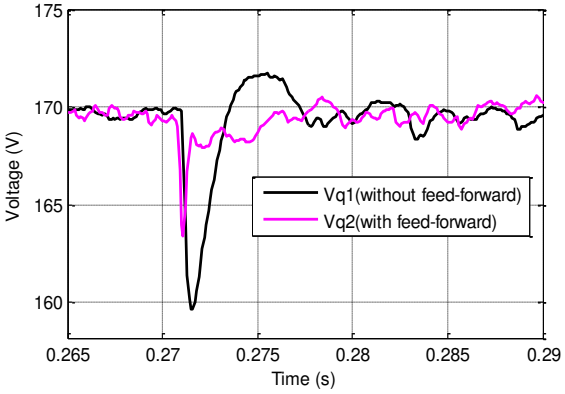
(c) Comparison of the output voltage on *dq* axis with and without current feed-forward.



(d) Current step change.



(e) Detailed *d*-axis voltage during current step with and without current feed-forward.



(f) Detailed *q*-axis voltage during current step with and without current feed-forward.

Fig. 5-12. Experimental data of inverter 1 output current and voltage in case 1 and 2.

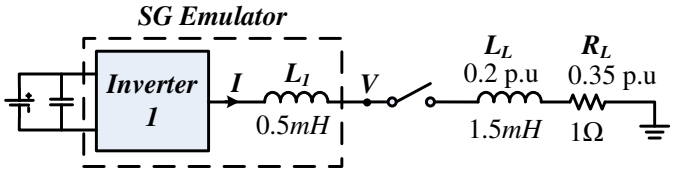
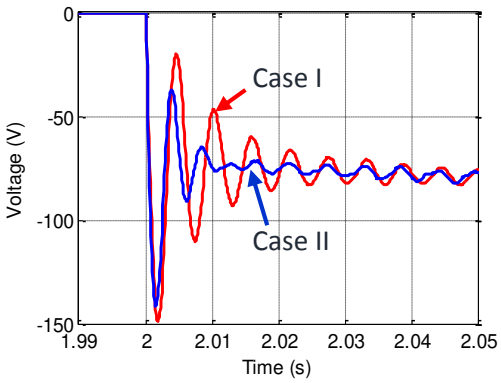
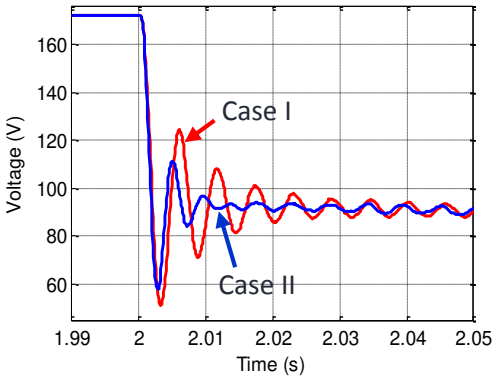


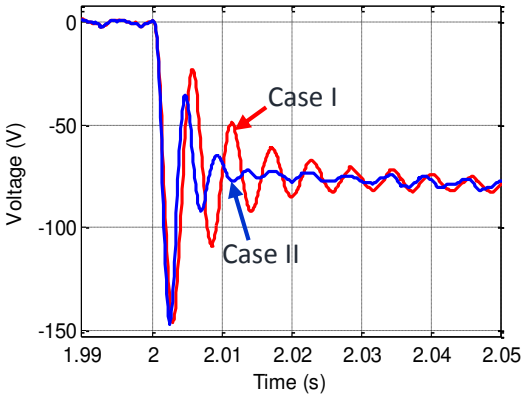
Fig. 5-13. Simulation of a single SG emulator under load change.



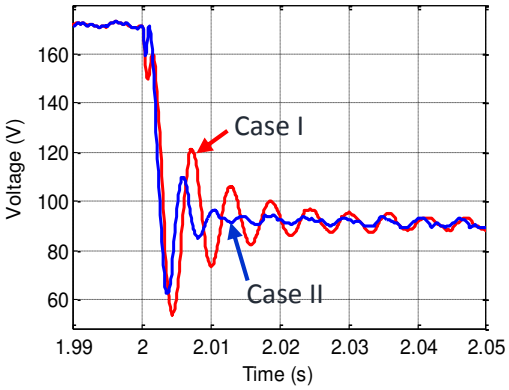
(a) Emulator voltage reference u_d.



(b) Emulator voltage reference u_q.



(c) Emulator output voltage v_d.



(c) Emulator output voltage v_q.

Fig. 5-14. Simulation results of the SG emulator voltage references and output.

As shown in Fig. 5-13, simulation of a single SG emulator with switching model is performed by using Matlab/Simulink. The breaker closes when $t = 2$ s, and two cases are studied: $L_{fc} = 0$ and $R_{fc} = 0$ in Case I and $L_{fc} = 0.5 \times 10^{-3}$ and $R_{fc} = 0$ in Case II. The emulator voltage reference and output exhibit large difference in the two cases, as demonstrated in Fig. 5-14. Since the VSI is embedded into the original system, its characteristic will influence the closed-loop behavior of the whole PHIL system. Even though the voltage output *v* can track the reference *u* well in both cases, it does not necessarily mean that both emulations are correct. In simulation, the original system can be developed for comparison, while in practice the input signals resulting from the original system response is actually unavailable, which requires a better way to evaluate the error other than simply to compare the reference and the output curves.

5.4 Conclusion

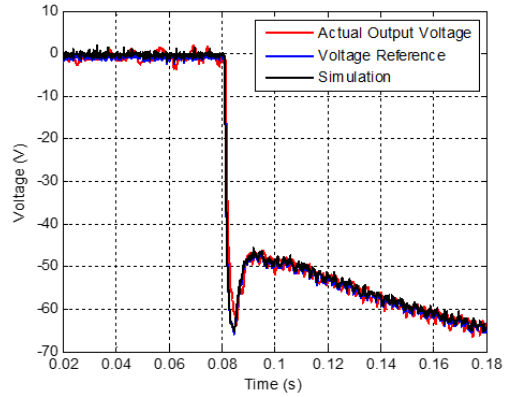
The control design targets of an SG emulator are to have large enough bandwidth and small converter output impedance. A single voltage controller is adequate for the converter topology with only an inductor filter, since the inductance is small enough and its voltage drop can be ignored compared with the load. Limited reduction of the converter output impedance is realized by increasing the control parameters. A current feed-forward can further decrease the difference between the emulator and the target SG. This feed-forward can reduce the amplitude of the converter output impedance Z_{cdd} and Z_{cqq} without increasing PI parameters, especially when the load impedance is small. The best effect can be achieved when the feed-forward parameters are exactly the same with the filter inductor parameters. However, it will also make a converter more prone to instability under certain capacitive loads. The effect of the feed-forward is verified through experiment.

6 Accuracy Evaluation and Verification of Converter Based Generator Emulator

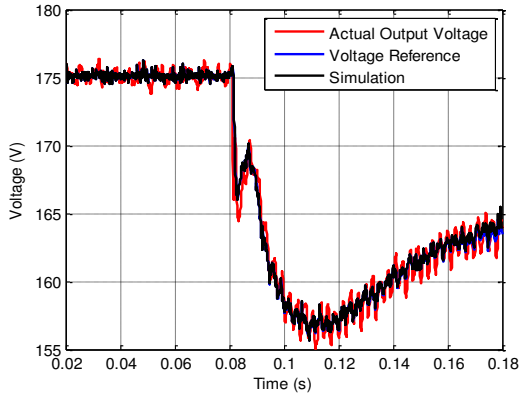
This chapter verifies the developed SG emulator by two methods: visual inspection of the experimental and simulation waveforms, and quantitative error model calculation. Based on the error model, the main factors that influence the emulator performance are investigated.

6.1 Verification of the SG Emulator by Visual Inspection

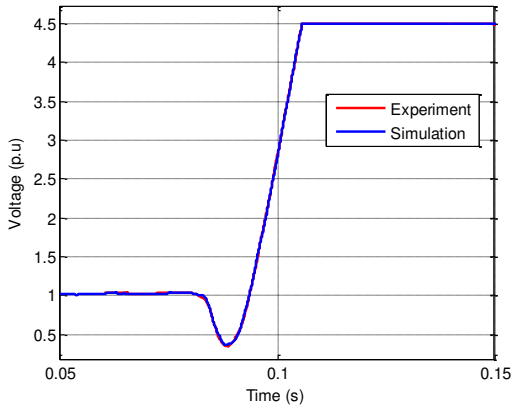
Even though visual inspection on the output waveforms does not deliver any quantitative analysis on the error, it can still give a preliminary verification. Since the SG with the corresponding rating is not available, the simulation of the original system can be chosen as the reference. The experimental setup is the same with Fig. 5-11, where Inverter 1 works as an SG emulator and Inverter 2 as a ZIP load. A step change of load active power from 0 p.u to 0.6 p.u is applied. First, the current data in the experiment is used as current input in the simulation by MATLAB/Simulink, and the corresponding voltage output in the simulation is compared with the experimental result to verify the SG model. As shown in Fig. 6-1, the actual output voltages are the emulator output voltage v_d and v_q, and the voltage references are the real time calculation of the SG terminal voltages u_d and u_q based on the input current. u_d, u_q, and the excitation voltage e_{fd} in the experiment match very well with simulation results, which verifies the discretized SG model in the DSP. At the same time, the actual emulator output voltages v_d and v_q has a small discrepancy influenced by the control bandwidth during the transient.



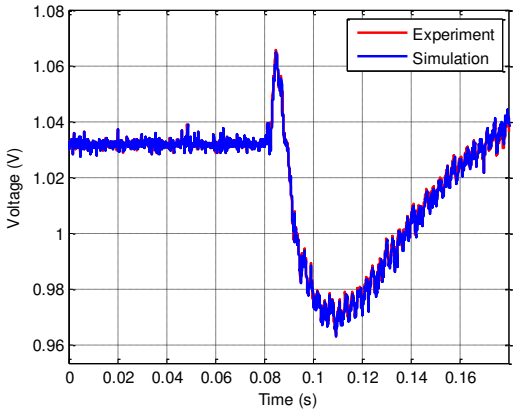
(a) Voltage on d-axis



(b) Voltage on q-axis



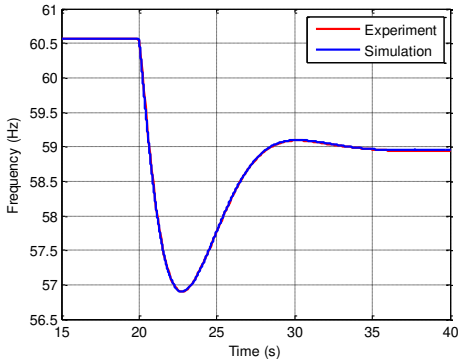
(c) Excitation voltage



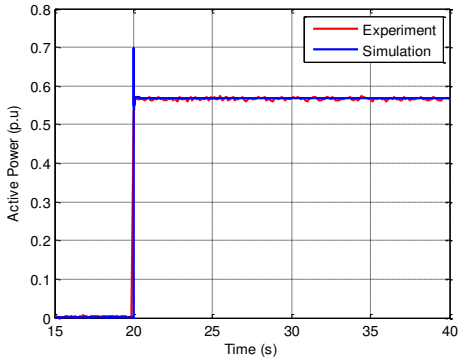
(d) Terminal voltage amplitude

Fig. 6-1. Comparison between experimental and simulation data for verifying the SG model.

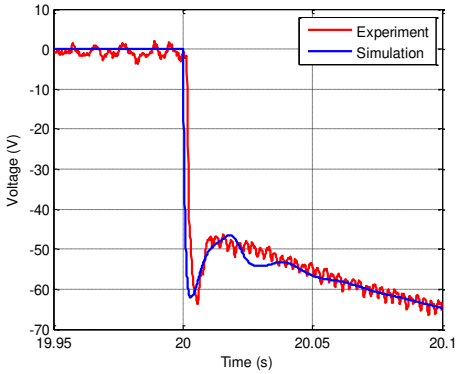
To validate the emulation with the embedded converter and its control, data from an independent simulation with exactly the same network structure and parameters are required. In the simulation through Matlab/Simulink, Inverter 1 is replaced by the corresponding generator model, and Inverter 2 is realized by the average model of the load emulator including 20% constant impedance, 20% constant current, and 60% constant power. Comparison results are demonstrated in Fig. 6-2. The frequency and the electric power data of the SG emulator is acquired from LabVIEW with 10 Hz sampling frequency, and the rest are obtained from the DSP.



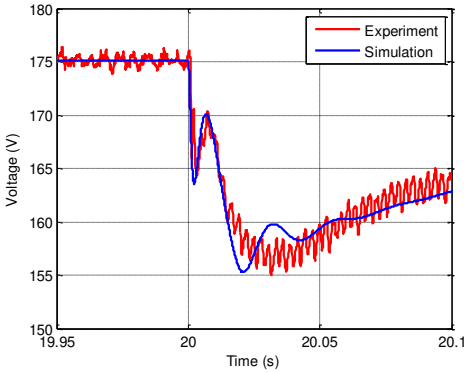
(a) Generator frequency



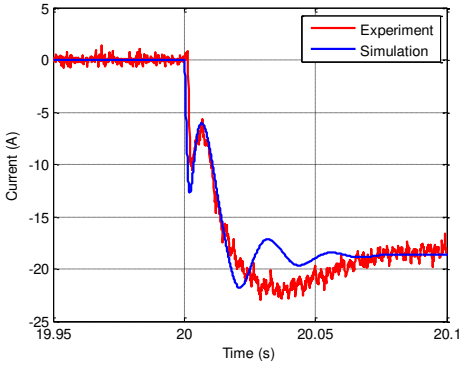
(b) Generator electric power



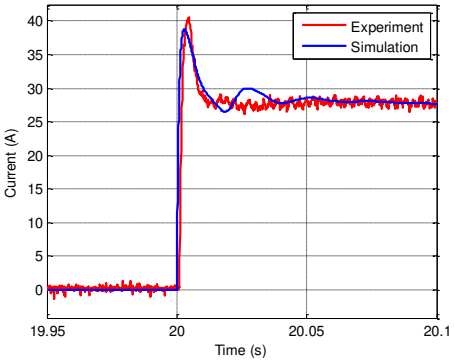
(c) Generator terminal voltage on *d*-axis



(d) Generator terminal voltage on *q*-axis



(e) Generator output current on *d*-axis



(d) Generator output current on *q*-axis

Fig. 6-2. Comparison between the emulation and the simulation of the original system.

The generator terminal voltages in the experiment are the converter output voltages v_d and v_q, as shown in Fig. 6-2 (c) and (d). The steady state and dynamic results of the experiment and the simulation match very well except for some small discrepancies on the voltage and current amplitude during the disturbance. In the above waveforms, the error can be caused by the inaccurate modeling of the HTB parameters or the improper converter control design. But the real cause is difficult to conclude simply based on visual comparison. Therefore, the influence of the VSI on the whole system has to be investigated thoroughly and separately from the other sources of error.

6.2 TFP Based Error Estimation and Evaluation

Traditionally, the error of a control system is defined as the difference between the input and the feedback signal. For a PHIL system, the application of the power interface and its controller will change the closed loop transfer function of the whole system, and thus adding errors. This type of error cannot be obtained directly by comparing its reference and the feedback signals, because the behavior of the original system at this point is unavailable.

W. Ren [58] has proposed the transfer function perturbation (TFP) based method to evaluate the error in a PHIL emulation. As shown in Fig. 6-3, $G(s)$ is the original system transfer function, and $\varepsilon G(s)$ is the additional transfer function caused by the PHIL interface and its controller. The error is then defined as the normalized difference, in other words, relative error, between the transfer function of the original system and the PHIL system, as shown in (6-1).

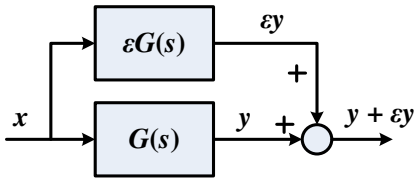


Fig. 6-3. Transfer function perturbation (TFP) based error evaluation.

$$ER_{TFP} = W_o \left| \frac{\varepsilon G(s)}{G(s)} \right| \tag{6-1}$$

A weighting function W_o is applied to investigate the error under different frequency ranges.

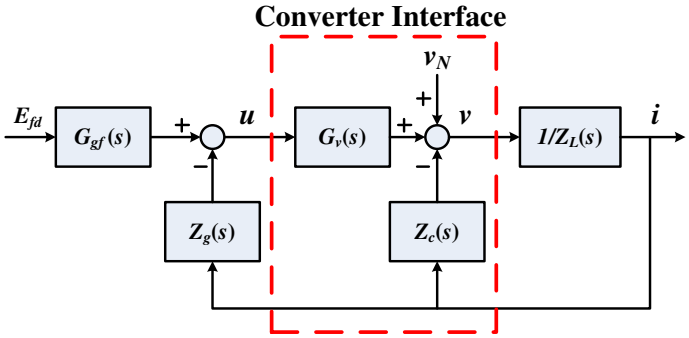


Fig. 6-4. Closed loop diagram of a voltage source emulator.

Based on this concept, a voltage source emulator, as shown in Fig. 6-4, can be viewed as the original system, with the transfer function "1", plus the transfer functions that causes error, [G_{errv}] in Fig. 6-5. v_N denotes the noise caused by the converter interface, such as harmonics.

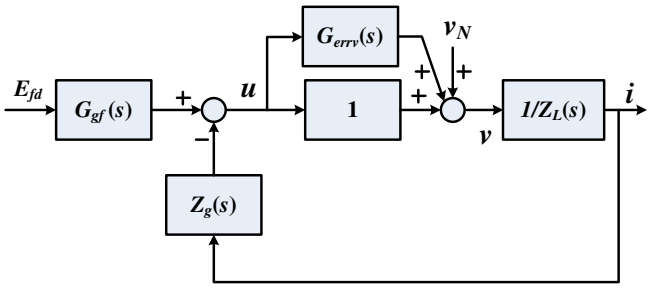


Fig. 6-5. Closed loop diagram of a voltage source emulator with transfer function perturbation.

In the SG emulation system as shown in Fig. 6-4, the closed-loop transfer function is defined as:

$$[G_p] = \frac{[i_{dq}]}{E_{fd}} = \left([G_v][Z_g] + [Z_c] + [Z_L]\right)^{-1}[G_v][G_{gf}] \tag{6-2}$$

The original system transfer function is expressed as:

$$[G_o] = \left([Z_g] + [Z_L]\right)^{-1}[G_{gf}] \tag{6-3}$$

The TFP error is then defined as:

$$[ER_{TFPdq}] = \begin{bmatrix} ER_{TFPd} \\ ER_{TFPq} \end{bmatrix} = \begin{bmatrix} \left|\frac{G_{pd} - G_{od}}{G_{od}}\right| \\ \left|\frac{G_{pq} - G_{oq}}{G_{oq}}\right| \end{bmatrix} \tag{6-4}$$

Apparently, the TFP error involves the model of both the original system and the converter interface, which cannot be represented solely by the open loop transfer function $G_{errv}(s)$. That means, the TFP error is different at varying generator and load parameters. If the system is symmetrical on *abc* axis, the evaluation can be performed on any one of the *abc* axis as a single input single output system. However, the situation is much more complicated for a generator emulator. As shown in Fig. 5-7, an SG model is unsymmetrical on *dq* axis, and the cross coupling impedance Z_{gdq} and Z_{gqd} play the major part in its model. The system now becomes single input multiple output. The evaluation of the TFP error then cannot be easily carried out on the stationary coordinates as mention in W. Ren's work, where only voltage source models were adopted. In

order to avoid analysis on *dq* axis, the rotor dynamics were assumed to be constant in the motor model in [48]. Yet, the neglecting of rotor dynamics will lead to a different FTP error transfer function. Since the main goal of this work is to verify the emulator, the rotor dynamics have to be taken into consideration.

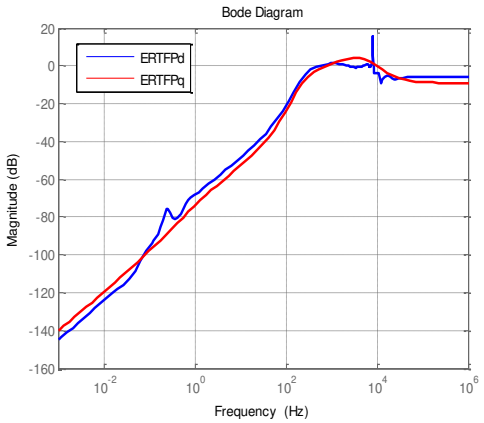
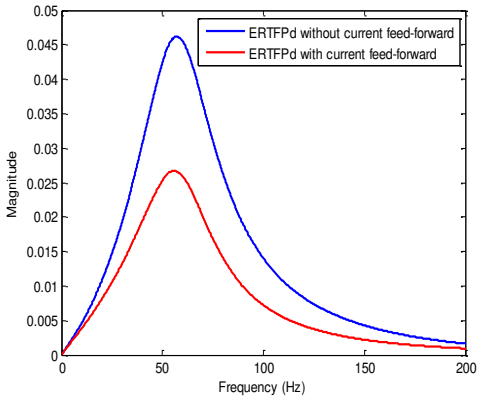
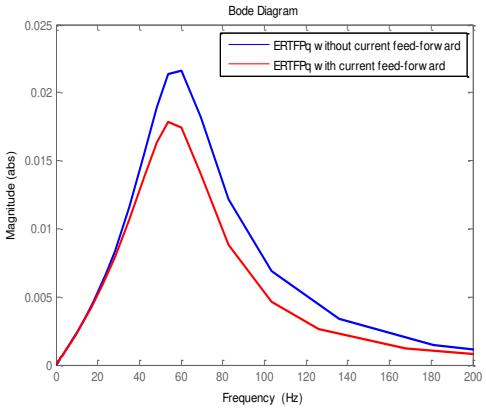


Fig. 6-6. TFP error of the SG emulation system on *dq*-axis.

As demonstrated in Fig. 6-6, the TFP error of the SG emulation on *dq*-axis typically will increase with frequency, caused by the limited converter control bandwidth. Assume that the weighting function $W_o = \frac{1}{\left(\frac{s}{2\pi f_W}\right)^5 + 1}$ and $f_W = 60$ Hz, the TFP error on *dq*-axis with and without the current feed-forward are shown in Fig. 6-7. Clearly, the current feed-forward can decrease the TFP error, which confirms the conclusion drawn in chapter 5.



(a) TFP error on d axis.



(a) TFP error on q axis.

Fig. 6-7. TFP error of the SG emulator with and without current feed-forward.

However, this method only takes into consideration the amplitude response difference between the emulated and the original system in frequency domain, which results in an incomplete evaluation of the error. Besides, it does not give a method to calculate the overall error.

Quantitatively, there are several different ways to assess the error in a vector. The most widely applied methods are the infinity norm and the second norm. The infinity norm of a vector x is defined as the magnitude of the largest component: $\|x\|_\infty = \max_{1\le i\le n}|x_i|$. The second norm of the vector x is defined as: $\|x\|_2 = \sqrt{\sum_{i=1}^{n}|x_i|^2}$. The following analysis will utilize the second norm to evaluate the average distance between curves of the original system and the emulated system on the magnitude and phase in the frequency domain.

Assume that A_p and P_p are the amplitude and phase of G_p, and A_o and P_o are the amplitude and phase of G_o. Define the relative error between G_p and G_o over the frequency range of interest as a second norm on magnitude and phase:

$$A_{ER} = \frac{\|A_p - A_o\|_2}{\|A_o\|_2} \times 100\%$$
$$P_{ER} = \frac{\|P_p - P_o\|_2}{\|P_o\|_2} \times 100\% \quad (6\text{-}5)$$

where A_{ER} is the relative error on amplitude and P_{ER} on phase. Since the error is relative, different selection of the output signal, such as voltage instead of current, will give the same result. In SG emulation, the error on *d*-axis and *q*-axis will be calculated separately. The frequency range is chosen as 0-200 Hz in the following analysis.

Table 6-1. SG emulation error with different control parameters.

Control parameters	**Amplitude**		**Phase**	
	A_{ERd}	A_{ERq}	P_{ERd}	P_{ERq}
$K_i = 10$	0.25	10.25	50.36	57.41
$K_i = 30$	1.11	3.79	7.17	7.32
$K_i = 50$	0.52	1.59	8.12	10.34
$K_i = 30$ (With feed-forward)	0.72	2.37	2.5	3.42

Table 6-2. SG emulation error with different time delay.

Time delay	**Amplitude**		**Phase**	
	A_{ERd}	A_{ERq}	P_{ERd}	P_{ERq}
150 μs	0.72	2.37	2.5	3.42
400 μs	1.73	5.54	4.96	8.77
800 μs	2.53	4.67	25.25	36.26

The emulation error under different control parameters is given in Table 6-1. The error

amplitude decreases with the increase of control parameters. But at the same time, when K_i is too large, the error on phase will increase again. This result matches with the previous analysis in section III, but it also means that the error evaluation based only on amplitude is not correct. In addition, the effect of the current feed-forward is verified through the error index.

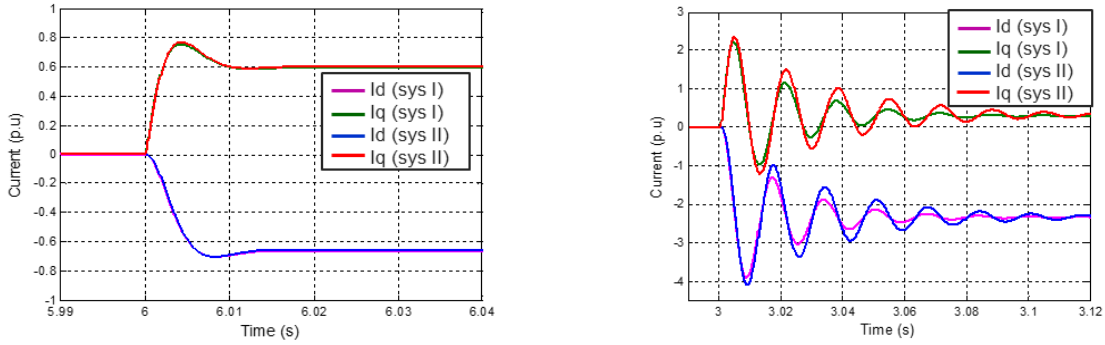
Time delay is another factor that influences error. As shown in Table 6-2, longer time delay will result in larger error both on amplitude and phase. The control bandwidth and the time delay together in a converter indicate its switching frequency. Higher switching frequency with smaller time delay and larger control bandwidth is, of course, preferable to reduce the emulation error.

Table 6-3. SG emulation error with different loading condition.

Load Condition	**Amplitude**		**Phase**	
	A_{ERd}	A_{ERq}	P_{ERd}	P_{ERq}
$R_L = 3.2\ \Omega\ (1.11\ \text{p.u})$ $L_L = 5.2\ mH (0.68\ \text{p.u})$	0.42	0.81	4.39	3.45
$R_L = 2.2\ \Omega\ (0.69\ \text{p.u})$ $L_L = 4.2\ mH (0.55\ \text{p.u})$	0.56	1.28	5.09	4.17
$R_L = 1.2\ \Omega\ (0.43\ \text{p.u})$ $L_L = 3.2\ mH (0.42\ \text{p.u})$	1.11	3.79	7.17	7.32

Moreover, error is also a function of load impedance. Under the same control parameters, the error will increase with the decrease of load impedance. An extreme example of this phenomenon is shown in Fig. 6-8. Sys II is the SG emulation system simulated in Matlab/Simulink with the same structure described in Fig. 5-13. Sys I is the original system with the converter replaced by the corresponding SG model. Under the same load step, the output current on *dq*-axis of the two

systems are compared in Fig. 6-8. When $R_L = 1.2\ \Omega$ and $L_L = 4.2\ mH$, the emulator output current matches with the original system very well, as shown in Fig. 6-8 (a). However, when $R_L = 0.2\ \Omega$ and $L_L = 3.2\ mH$, there is obvious difference between the two systems, which in calculation corresponds to 171% error on the amplitude. Therefore, the control parameters have to be designed for the worst case scenario.



(a) $R_L = 1.2\ \Omega$ and $L_L = 4.2\ mH$ (b) $R_L = 0.2\ \Omega$ and $L_L = 3.2\ mH$

Fig. 6-8. Comparison between the output current in the SG emulation system and the original system under load change.

6.3 Performance Robustness

A generator is usually equipped with several different closed-loop controls, such as AGC and AVR. Errors caused by the converter interface can also influence performances of these controls in a generator emulator. Since the AGC time constant is up to minutes, this paper only focuses on the error influence on AVR. As mentioned in Chapter III, the simplified type I AVR is implemented with a proportional controller. The terminal voltage u_t is obtained by:

$$u_t = \sqrt{u_d^2 + u_q^2} \tag{6-6}$$

Apply small perturbation and linearize the equation,

$$\Delta u_t = \frac{U_{d0}}{U_{t0}} \Delta u_d + \frac{U_{q0}}{U_{t0}} \Delta u_q \tag{6-7}$$

where U_{d0}, U_{q0}, and U_{t0} are the operating point values of u_d, u_q, and u_t.

Assume that $K_A = 200$, $T_A = 0.01$, the bode plot of the two open-loop transfer functions defined by $\Delta u_t / U_{tref}$ under different loads are shown in Fig. 6-9 and Fig. 6-10. With PHIL interface, the phase margin and gain margin will be slightly different from the original. Under light load, as shown in Fig. 6-9, the PHIL interface causes 1.5% difference in gain margin, and less than 1% error on the phase margin and cutoff frequency. Similar under heavy load condition, the PHIL interface does not influence phase margin and cutoff frequency, but will cause 2.4% error on the gain margin.

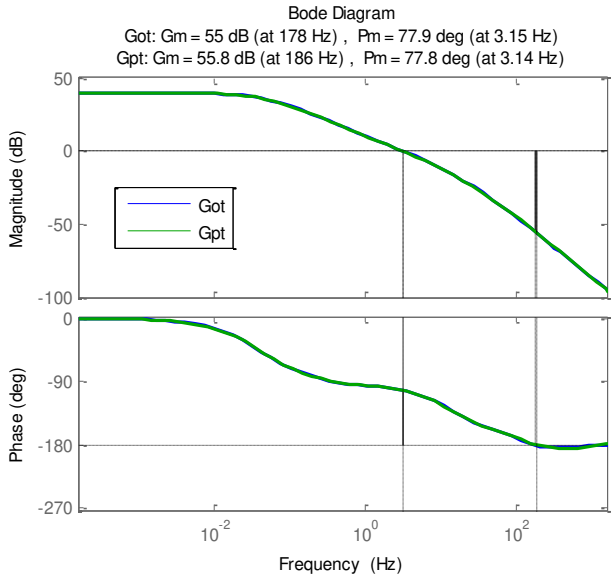


Fig. 6-9. Bode plot of G_{ot} and G_{pt} when $R_L = 3\ \Omega$, $L_L = 2$ mH.

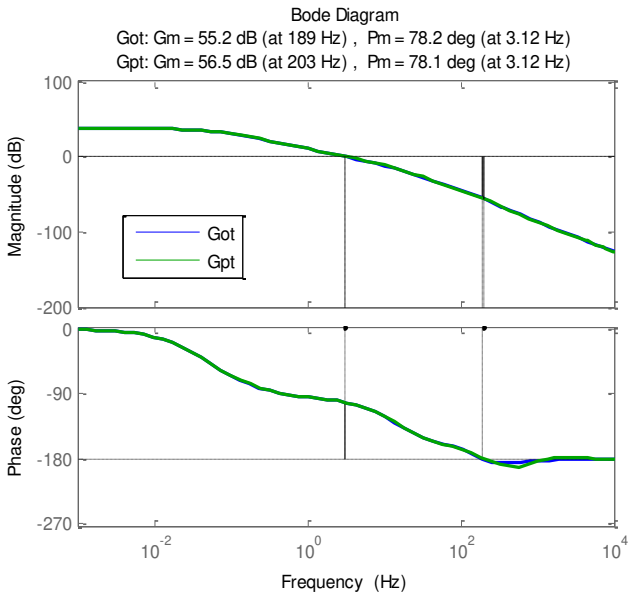


Fig. 6-10. Bode plot of G_{ot} and G_{pt} when $R_L = 2\ \Omega,\ L_L = 0$.

6.4 Conclusion

Verification of the developed SG emulator is first realized by comparing the output waveforms with the corresponding simulation results. Then, the TFP based error model is utilized to investigate the converter influence on emulation accuracy. The TFP method compares the transfer function of the original system without the converter interface, and the PHIL system on the frequency domain. Since a frequency domain response includes not only magnitude but phase characteristics, the TFP error should inspect both aspects. At the same time, the TFP error represents a vetor of errors on different frequencies. In order to develop an overall performance indicator, the second norm is utilized for the relative error vectors. The calculation results verify that the current feed-forwad can decrease the error in the frequency range of interest. At the same time, the error is also related to the amount of time delay as well as loading conditions. With the increase of the load power consumption, the error will increase under the same control parameters. To gurantee the performance target under various conditions, the control parameters should be

designed for the worst case scenario such as a fault. In addition, the converter influence on the closed-loop control, AVR, is very small as long as the emulator performance target is achieved.

7 The Developed Generator Emulator in Multiple Generation System

After the verification of a single generator emulator, the interconnection of multiple SG emulators is discussed in this chapter. Stability issues are studied and the main reasons that cause instability are investigated and verified. The developed SG emulator is also verified in this chapter in a two-area system.

7.1 Generator Emulator Synchronization

In a larger system with multiple generators, proper synchronization process is of great importance. Practically, during synchronization, generators will be started with the same terminal voltage amplitude, and a slightly larger frequency than the grid before connecting to it. If the errors of voltage angle, frequency, and amplitude between the generator and the grid reach the threshold, then the breaker can be closed.

The electric model of the generator is given by the equations (4-16), with open circuit condition, by solving (4-16) under steady state, we obtain $U_d = E'_d = 0,\ U_q = E'_q = E_{fd}$. Interestingly, a phase lock loop (PLL), which is used widely in grid-connected converters, will achieve the same result. By using the same Park's transformation with the SG model, the PLL will force the *d* axis voltage to be zero, and the value of *q* axis voltage will be equal to the amplitude of the terminal voltage. That means, the angle output of a PLL for the grid voltage can be directly used for synchronization purpose. Because the PLL can lock to the grid frequency accurately, there is no need for detecting the synchronization condition anymore.

Based on the above analysis, the synchronization process of an SG emulator is realized by three steps: transition 1 – connect into the system open loop by using a phase lock loop (PLL) to lock the system frequency; transition 2 – enable close loop control; transition 3 – alternate frequency reference from PLL output to mechanical model output. No contactor switch action is required throughout the process.

To further explain the synchronization process, experimental results are shown in Fig. 7-2 based on the structure demonstrated in Fig. 7-1. Frequency and generator output power data are obtained from the DSPs of each emulator.

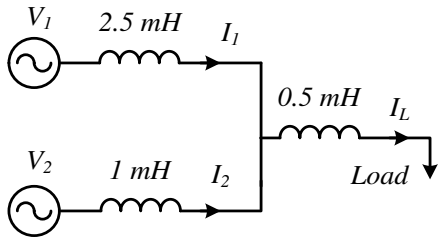
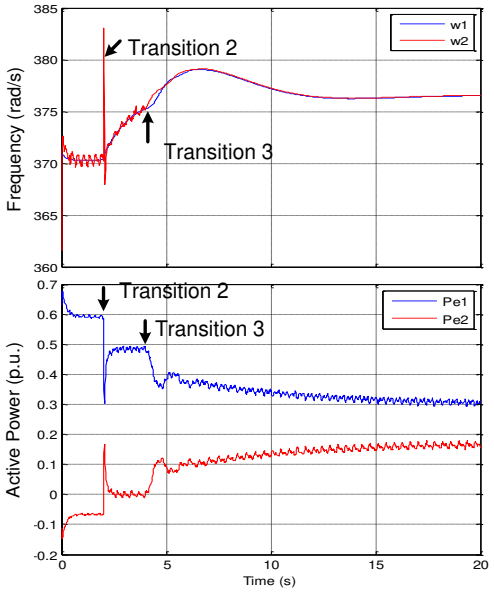


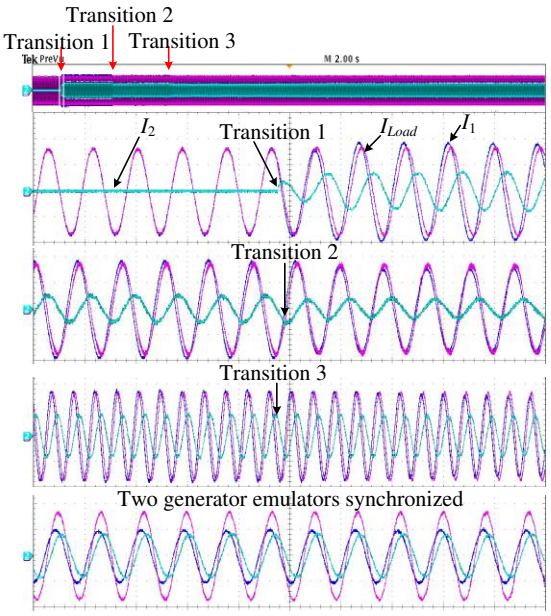
Fig. 7-1. Experiment layout for synchronization.

First, the generator emulator 1 operates in steady state with a constant load. As shown in Fig. 7-2 (b), before transition 1, SG emulator 1 supports all the current needed by the load. Before connection of SG emulator 2, its generator electric model calculates the terminal voltage references $U_d = 0,\ U_q = E_{fd}$. At transition 1, when $t = 0$ s in Fig. 7-2 (a), generator emulator 2 is connected into the system with voltage open loop to avoid large inrush current. As shown in Fig. 7-2 (b), the output current of the generator emulator 2 is mainly reactive, and no inrush current is observed. At transition 2, when $t = 2$ s in Fig. 7-2 (a), closed loop voltage control is enabled. During this process, the PLL aligns the voltage vector with the q-axis (defined by the applied dq transformation), thus

zero output power. At transition 3, the frequency reference switches to the mechanical model output, and the generator emulator 2 starts to output power and share the load with the generator emulator 1. As demonstrated in Fig. 7-2 (a), after transition 3, the frequencies of SG emulator 1 and 2 quickly overlap with each other after a small difference during the first second.



(a) Generator 1 and 2 frequency and electrical power output during synchronization.



(b) Generator 1, 2, and the load current during synchronization (current: 10 A/div).

Fig. 7-2. Generator waveforms during synchronization.

7.2 Stability of Two Interconnected SG Emulators

7.2.1 With Constant Current Load

In a two-generation system as shown in Fig. 7-3, SG_1 and SG_2 share the same current load $[I_L]$. $[Z_{T1}]$ and $[Z_{T2}]$ are the local transmission lines. Assume that the current load is an ideal current source, and the mechanical models of an SG, such as droop, governor, and turbine, are not taken into consideration since the main research of this work is to investigate the interaction between the

developed voltage control and SG electric models. Therefore, even though the two SG emulators have different rotor angles, the linearization of their models does not require any specific operating point when the calculation of power is not involved and the rotor speed is considered to be constant. After linearization, the system can be represented by the structure demonstrated in Fig. 7-4, where $\left[G_{vgi}\right] = [G_{vi}]\left[G_{gfi}\right]$, $i = 1, 2$. The small signal closed-loop system model is then described in (7-2), where Y_s is the characteristic admittance of the system.

According to the control theory, a system is stable if its closed-loop transfer function does not have right half plane (RHP) poles. Otherwise, the system is unstable. Since $\left[G_{vg1}\right]$ and $\left[G_{vg2}\right]$ do not have RHP poles, the stability of the whole system is then decided by the characteristic admittance Y_s.

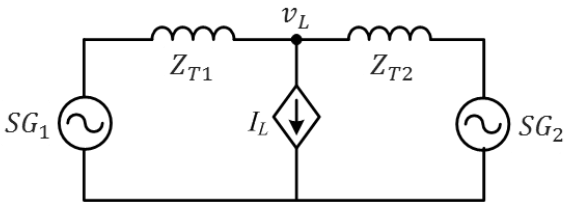


Fig. 7-3. Structure of a two-source system.

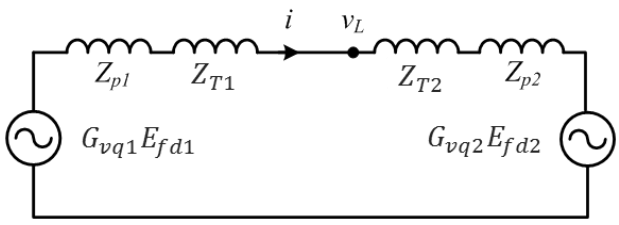


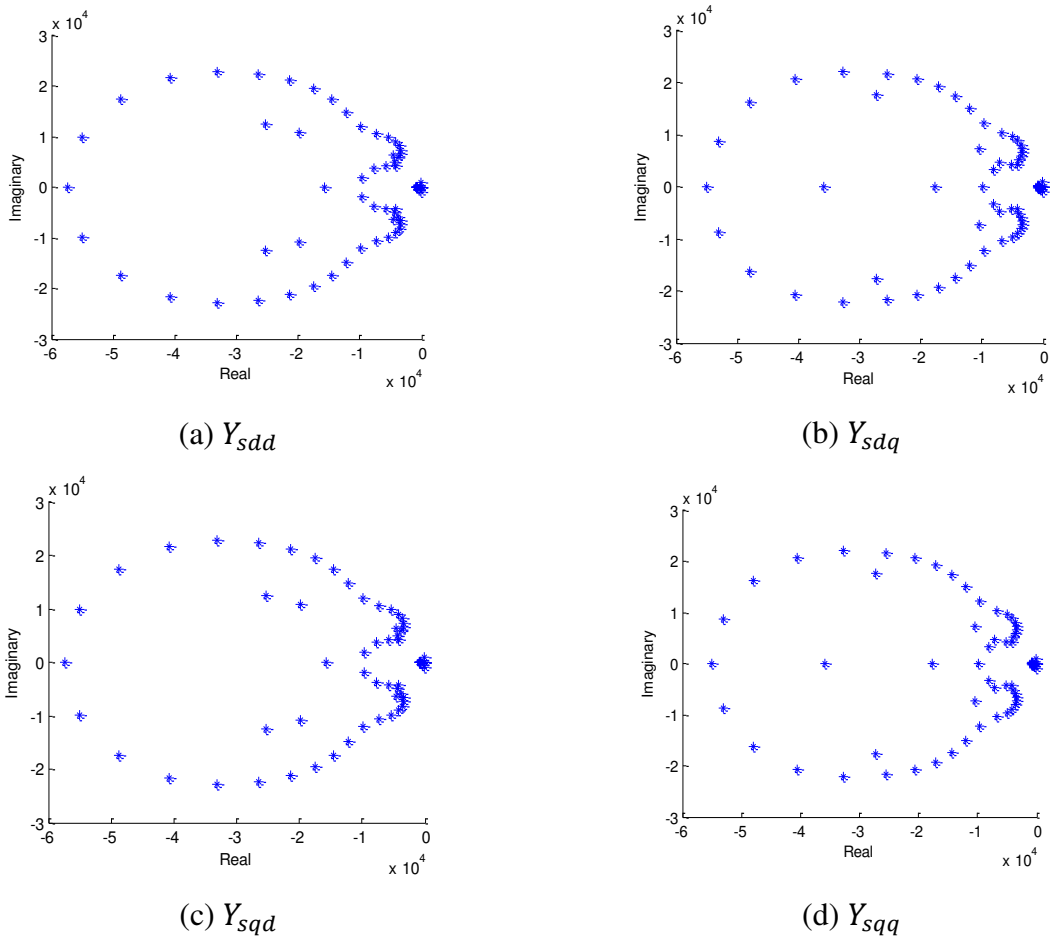
Fig. 7-4. The linearized two-source system.

$$[\Delta i_{dq}] = \left([Z_{p1}] + [Z_{T1}] + [Z_{T2}] + [Z_{p2}]\right)^{-1}\left([G_{vg1}]E_{fd1} - [G_{vg2}]E_{fd2}\right) \quad (7\text{-}1)$$

$$[Y_s] = \left([Z_{p1}] + [Z_{T1}] + [Z_{T2}] + [Z_{p2}]\right)^{-1}$$

Table 7-1. Converter power stage and control parameters.

Δt	V_b	Z_b	V_{dc}	ω_V	ω_I	K_p
150 us	50 V	2.88 Ω	136 V	300 Hz	5000 Hz	0.0053
K_i	L_f	R_f	L_{T1}	R_{T1}	L_{T2}	R_{T2}
30	0.6 mH	0.006 Ω	2.5 mH	0.12 Ω	1.2 mH	0.06 Ω



(a) Y_{sdd} (b) Y_{sdq}

(c) Y_{sqd} (d) Y_{sqq}

Fig. 7-5. Poles of the characteristic admittance Y_s.

The transfer function of an ideal time delay $e^{-s\Delta t}$ is irrational. Padé-approximation is then used in the following analysis. Fig. 7-5 demonstrates a steady case with the converter power stage and control parameters shown in Table 7-1. All the poles of the four elements in Y_s are on the left half complex plane.

The design of a control loop usually aims at achieving different typical systems based on the complexity of the control plant. A single integral controller is adequate to realize a typical type I system if $F_V(s)$ is first order. With the integral controller, the open loop transfer function of the converter system will have infinite gain at the DC component, -20 dB/dec slope crossing 0 dB line and -40 dB/dec slope at high frequency range. Clearly, it is a perfect choice to guarantee both accuracy and robustness, and it works very well in a single SG emulator. However, when two SG emulators are interconnected together with a structure shown in Fig. 7-3, large current swing arises because of instability.

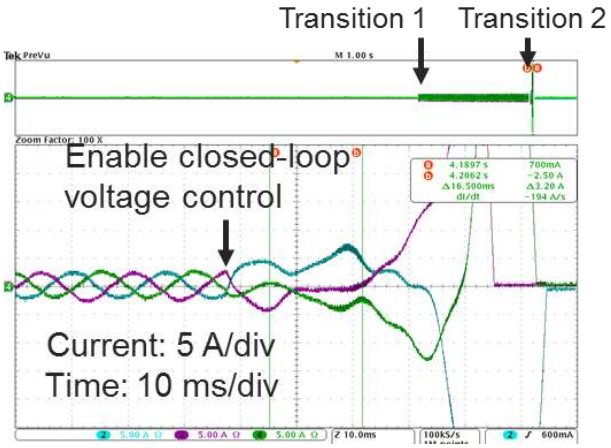


Fig. 7-6. SG emulator 2 three-phase output current when $K_p = 0$ and $K_i = 5$.

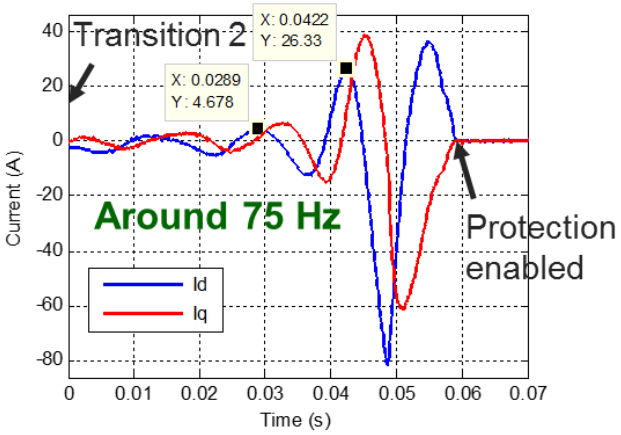
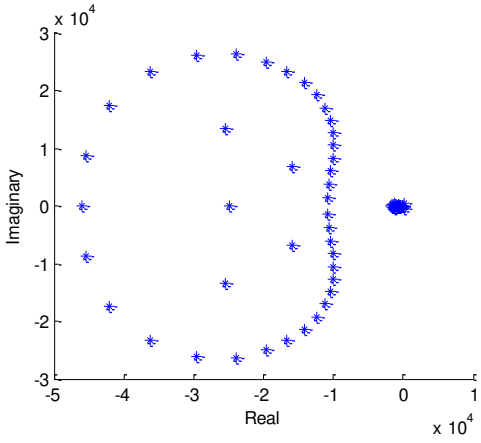


Fig. 7-7. SG emulator 2 output current on dq-axis when $K_p = 0$ and $K_i = 5$.

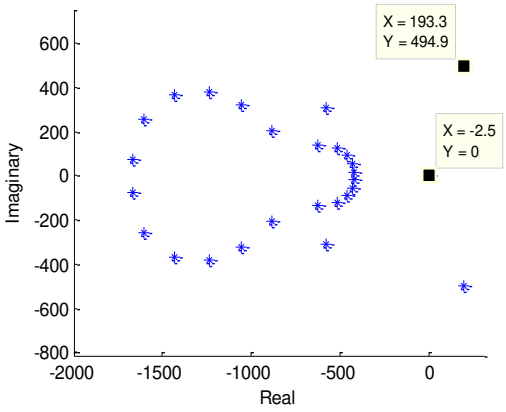
Fig. 7-6 and Fig. 7-7 demonstrate SG emulator 2 output current on stationary and dq reference frame respectively when connected to SG emulator 1. Data on dq-axis is obtained by DSP with a sampling frequency of 10 kHz. After transition 2, where closed-loop voltage control on SG emulator 2 is enabled as discussed earlier, current starts to oscillate with an increasing amplitude until the converter over-current protection kicks in. The oscillation frequency on dq-axis is around 75 Hz. With $K_p = 0$ and $K_i = 5$, the poles in Y_s are plotted in Fig. 7-8. A pair of RHP poles appears in each of the four elements. The imaginary part of the RHP pole corresponds to the oscillation frequency, which in this case is 494.9 rad/s, i.e. 78.8 Hz on dq-axis. The calculated frequency matches very well with the experiment.

To further verify the derived small signal model of the two-generation system, another experiment has been performed when $K_p = 0$ and $K_i = 30$. As shown in Fig. 7-9, the oscillation in the experiment is around 103 Hz on abc-axis and 154 Hz on dq-axis. The calculated result is 161 Hz (1014 rad/s) on dq-axis. Again, the calculation matches with the experiment quite well.

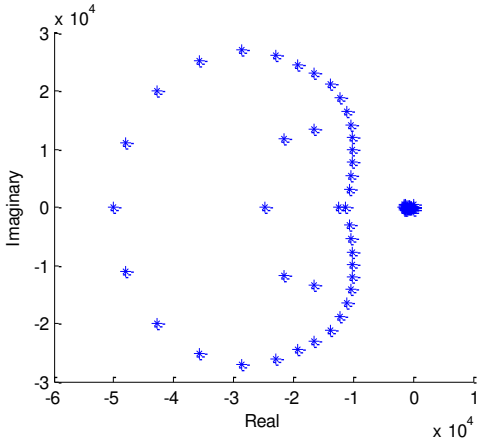
Fig. 7-8. Plots of $[Y_s]$ poles on the complex plane when $K_p = 0$ and $K_i = 5$.



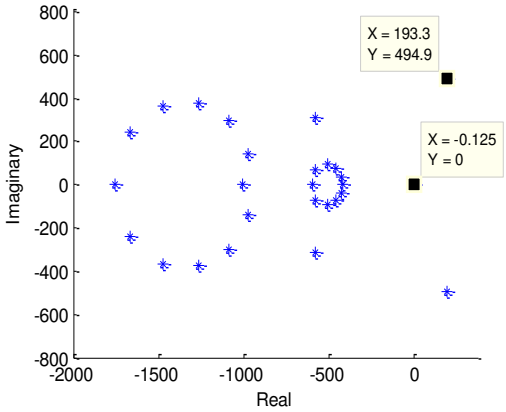
(a) Y_{sdd}



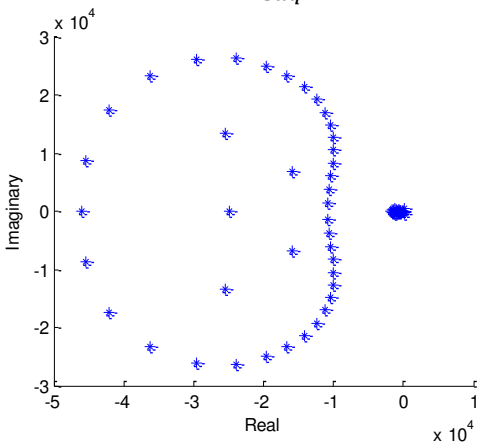
(b) Dominant poles of Y_{sdd}



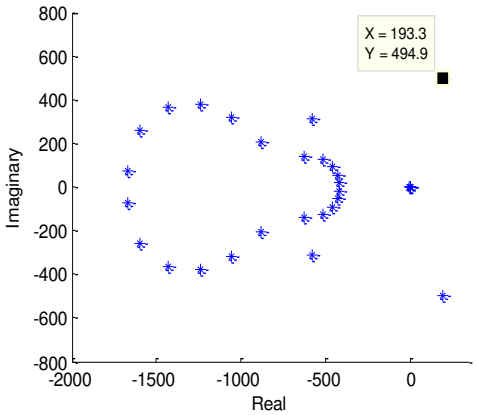
(c) Y_{sdq}



(d) Dominant poles of Y_{sdq}

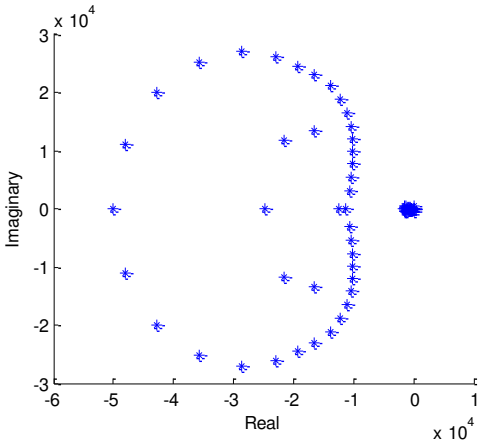


(e) Y_{sqd}

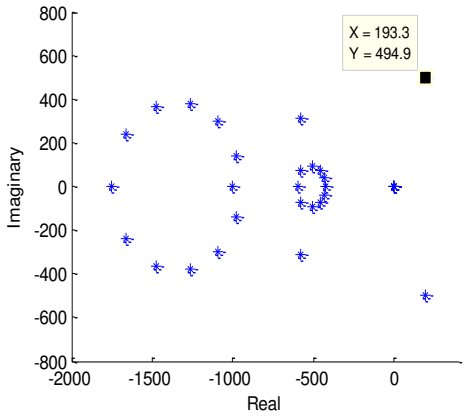


(f) Dominant poles of Y_{sqd}

Fig. 7-8 continued.

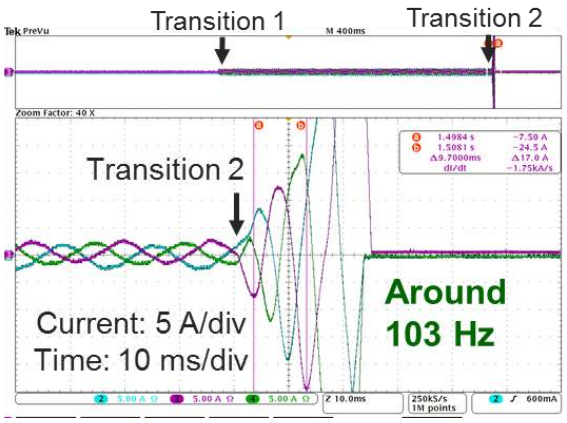


(f) Y_{sqq}

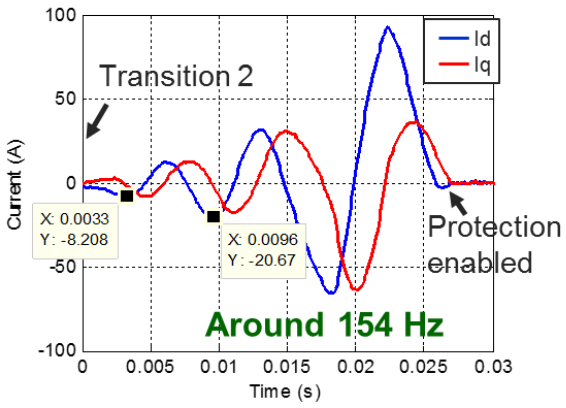


(g) Dominant poles of Y_{sqq}

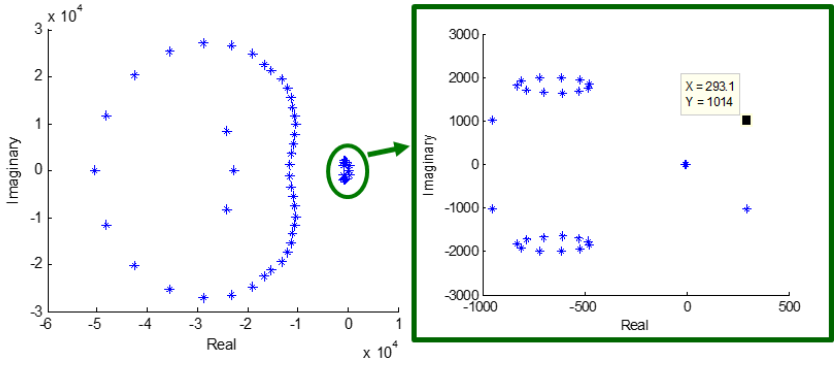
Fig. 7-8 continued.



(a) SG emulator 2 three-phase output current.



(b) SG emulator 2 output current on dq-axis.

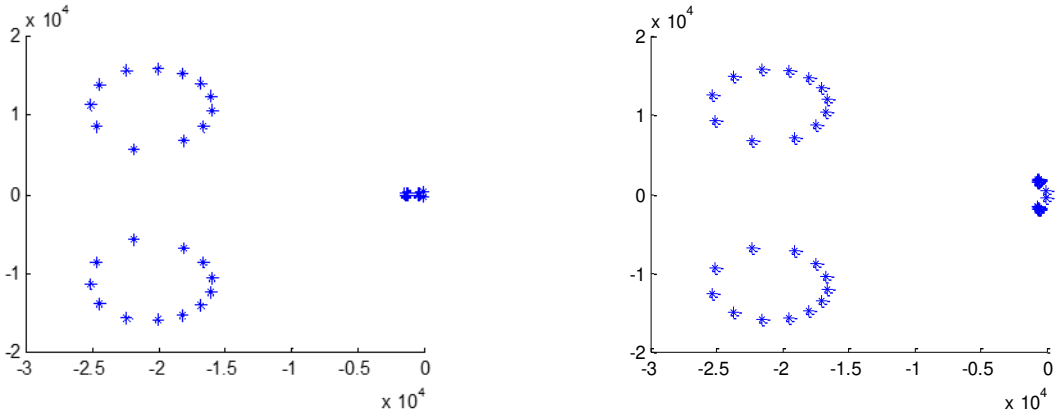


(c) Plot of Y_{sdd} poles on the complex plane.

Fig. 7-9. Experimental and calculated data when $K_p = 0$ and $K_i = 30$.

Then the questions that need to be answered are: is this a general converter paralleling problem, what is the cause of the instability, and how does it influence the stability?

Obviously, instability should not appear in a two-SG system under normal operating conditions, including sharing the same constant current load (CCL). At the same time, if the SG models are ignored and the converters take constant voltage references, i.e. $[Z_p] = [Z_c]$, the system is also stable. As shown in Fig. 7-10, Y_{sdd} does not have any RHP poles in any of the conditions when $K_i = 5$ or $K_i = 30$. As a conclusion, the instability may be created when the SG model is combined with the converter.



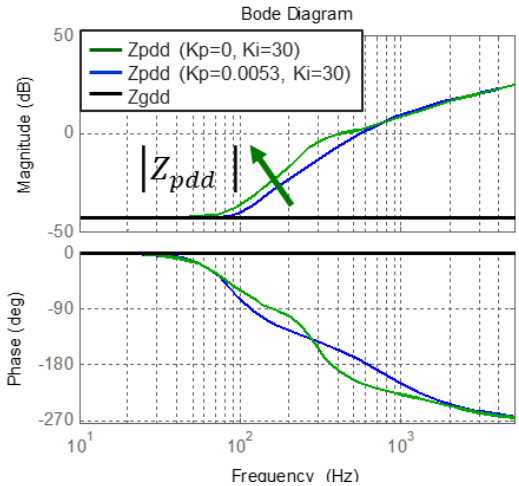
(a) $K_p = 0, K_i = 5$ (b) $K_p = 0, K_i = 30$

Fig. 7-10. Plot of Y_{sdd} poles on the complex plane.

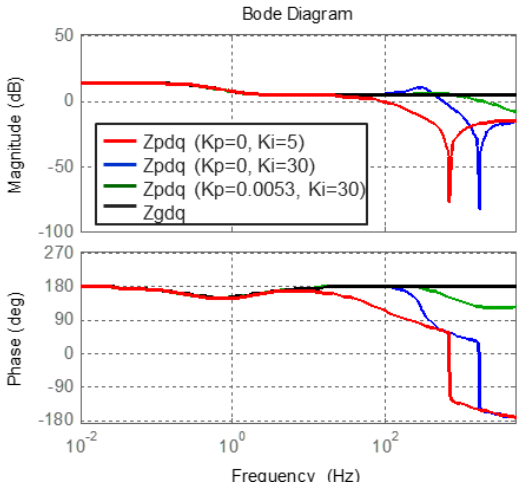
The inverse of an output impedance involves calculation of the inverse of its determinant, as described in (7-2). Since each of the elements in $[Z_p]$ is stable, the creation of the RHP poles is then caused by $1/|Z_p|$. In a 4th order SG model, $|Z_{gdd}|$ and $|Z_{gqq}|$ are much larger than $|Z_{gdq}|$ and $|Z_{gqd}|$ as shown in Fig. 4-1 to Fig. 4-3, thus Z_g^{-1} is stable. In a converter without SG model, $|Z_{cdq}|$ and $|Z_{cqd}|$ are much larger than $|Z_{cdd}|$ and $|Z_{cqq}|$ as shown in Fig. 5-6, thus $[Z_c]^{-1}$ is table too. With the combination of $[Z_g]$ and $[Z_c]$, the four elements of the emulator output impedance Z_p have similar amplitude especially around medium to high frequency range, therefore causing stability problems with improper control design.

$$[Z_p]^{-1} = \frac{1}{Z_{pdd}Z_{pqq} - Z_{pdq}Z_{pqd}} \begin{bmatrix} Z_{pqq} & -Z_{pdq} \\ -Z_{pqd} & Z_{pdd} \end{bmatrix} \tag{7-2}$$

Compared with PI, an integral controller results in larger amplitude of Z_{pdd} and Z_{pqq}, and phase deviation on Z_{pdq} and Z_{pqd}, as demonstrated in Fig. 7-11, which are speculated as the major cause of RHP poles in Y_s.



(a) Bode plot of Z_{pdd} and Z_{gdd}



(b) Bode plot of Z_{pdq} and Z_{gdq}

Fig. 7-11. Bode plot of Z_p when $K_p = 0$ and 0.0053, and Z_g.

As discussed in chapter 5, Z_{pdd} and Z_{pqq} are largely impacted by the converter output impedance Z_{cdd} and Z_{cqq} because Z_{gdd} and Z_{gqq} are small, while Z_{pdq} and Z_{pqd} are mainly influenced by G_{vd} and G_{vq}. Assuming that G_{vd} and G_{vq} are 1 over the whole frequency range, the poles of Y_{sdd} are plotted in Fig. 7-12 and Fig. 7-13. Without the current feed-forward, Y_s still has one pair of RHP poles, while the system becomes stable with the current feed-forward. This verifies that the decrease of Z_{cdd} and Z_{cqq} amplitude is beneficial for system stability.

In addition, if the converters use open-loop control, the two-generation system with the above SG and network parameters is unstable with 150 us time delay ($44.85 \pm 1009j$). Even though the system can gain stability with smaller X'_d and X'_q, for example 0.15 and 0.3 respectively, closed-loop control should be adopted to ensure the robustness of the whole emulation system.

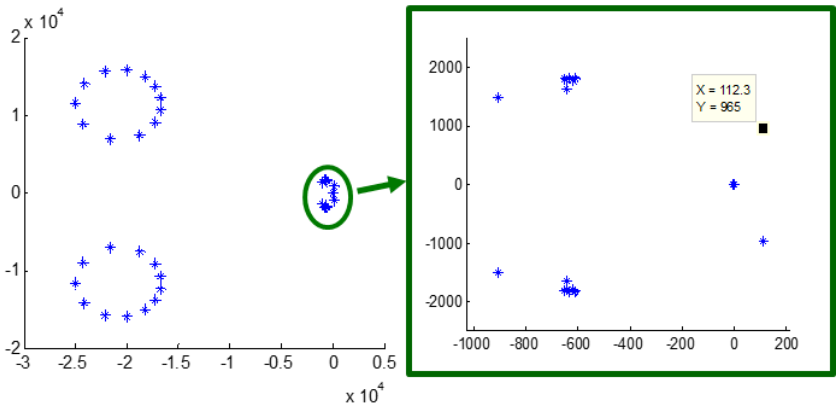


Fig. 7-12. Plot of Y_{sdd} without current feed-forward.

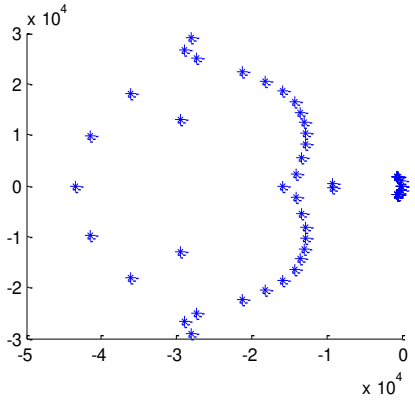


Fig. 7-13. Plot of Y_{sdd} with current feed-forward.

7.2.2 With Constant Impedance Load

When the current source is replaced by a constant impedance load (CIL) $[Z_L]$, as shown in Fig. 7-14, the small signal model of the two-SG emulator system with the load voltage as output becomes:

$$[\Delta v_L] = \left(I + [Z_1]([Z_L]^{-1} + [Z_2]^{-1})\right)^{-1} G_{vg1} E_{fd1} + \left(I + [Z_2]([Z_L]^{-1} + [Z_1]^{-1})\right)^{-1} G_{vg2} E_{fd2} \quad (7\text{-}3)$$

where $[Z_i] = [Z_{pi}] + [Z_{Ti}]$, $i = 1, 2$.

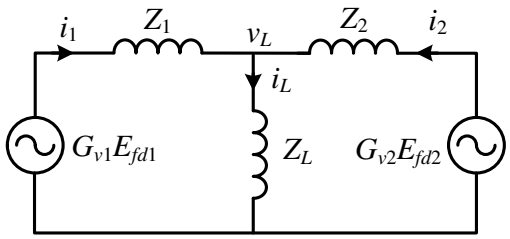


Fig. 7-14. Two-generation system with constant impedance load.

At the same time, the system model can be also rewritten as (7-4) when the output is selected as SG1 output current $[\Delta i_1]$ and (7-5) SG1 output current i_2 based on the same method. In (7-4), if the load impedance $[Z_L]$ is infinite, i.e. constant current load, the system model becomes (7-1).

$$\begin{gathered}[\Delta i_1] = \left(\left[Z_{eq2L}\right] + [Z_1]\right)^{-1}\left(\left[G_{vg1}\right]E_{fd1} - [Z_L]([Z_L] + [Z_2])^{-1}\left[G_{vg2}\right]E_{fd2}\right) \\ \left[Z_{eq2L}\right] = ([Z_L]^{-1} + [Z_2]^{-1})^{-1}\end{gathered} \tag{7-4}$$

$$\begin{gathered}[\Delta i_2] = \left(\left[Z_{eq1L}\right] + [Z_2]\right)^{-1}\left(\left[G_{vg2}\right]E_{fd2} - [Z_L]([Z_L] + [Z_1])^{-1}\left[G_{vg1}\right]E_{fd1}\right) \\ \left[Z_{eq1L}\right] = ([Z_L]^{-1} + [Z_1]^{-1})^{-1}\end{gathered} \tag{7-5}$$

When the load impedance is zero, (7-3) to (7-5) become:

$$\begin{gathered}[\Delta i_L] = [Z_1]^{-1}\left[G_{vg1}\right]E_{fd1} + [Z_2]^{-1}\left[G_{vg2}\right]E_{fd2} \\ [\Delta i_1] = [Z_1]^{-1}\left[G_{vg1}\right]E_{fd1} \\ [\Delta i_2] = [Z_2]^{-1}\left[G_{vg2}\right]E_{fd2}\end{gathered} \tag{7-6}$$

Under this condition, the interaction between the two SG emulators is minimized, and it is equivalent to have the two SG emulators running separately.

When the amplitude of the load impedance varies from zero to infinity, the stability of the two-generation system can be determined by either direct calculation of the poles or the Generalized Nyquist Criteria of the above closed-loop transfer functions [104][105]. The load impedance can provide some damping to the system. With the same power stage parameters shown in Table 7-1,

$K_p = 0.001, K_i = 20$, and current feed-forward disabled, different load impedance can make the two-generation system either stable or unstable. Assume that $R_L = 1\ \Omega$ and $L_L = 0$, the characteristic matrix $[Y_1] = \left(I + [Z_1]([Z_L]^{-1} + [Z_2]^{-1})\right)^{-1}$ has a pair of RHP poles as demonstrated in Fig. 7-15. The corresponding oscillation frequency is 890.1 rad/s (141.7 Hz). To verify the calculation, simulation has been performed in MATLAB/Simulink with the same parameters described above. As demonstrated in Fig. 7-16, large oscillation with 141 Hz frequency can be observed on the output currents of the two SG emulators, which matches with the calculation. When the load impedance decreases by half: $R_L = 0.5\ \Omega$ and $L_L = 0$, the two-generation system becomes stable. The poles of Y_{1dd} in this case is then demonstrated in Fig. 7-17. At the same time, when the load is constant current, the characteristic admittance matrix $[Y_s]$ described in 7.2.1 has a pair of RHP poles in each component: $55.22 \pm 880.5j$.

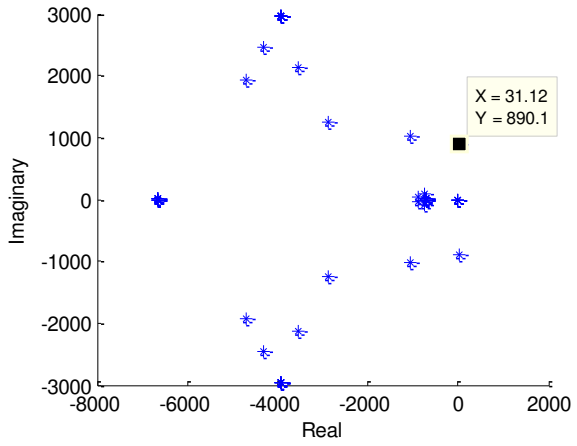
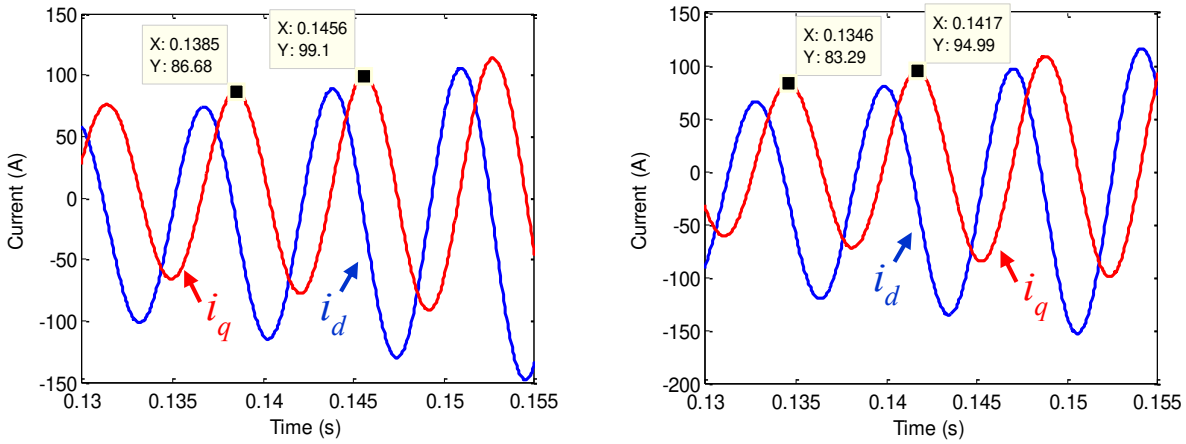


Fig. 7-15. Plot of the poles in Y_{1dd} when $R_L = 1\ \Omega$ and $L_L = 0$.



(a) SG emulator 1 output current on *dq*-axis. (b) SG emulator 2 output current on *dq*-axis.

Fig. 7-16. SG emulators output current on *dq*-axis in simulation.

Since the constant impedance load is passive, its phase response in frequency domain is between $-90°$ to $90°$. According the impedance matching theory, when the amplitude of the source impedance equals to the load impedance, if the phase difference between the two is larger than $180°$, the system is unstable [94]. Therefore, the source of instability is the two SG emulators, whose phase response is beyond the passive range at higher frequency as shown in Fig. 7-11. Take equation (7-4) as an example, the system model can be seen as the equivalent circuit of the load and SG emulator 2 in parallel connects with SG emulator 1. The equivalent impedance $[Z_{eq2L}]$ approaches the load characteristics when it is small enough compared with the SG emulator 2, and thus stabilizing the two-generation system if the SG emulator 1 itself is stable with the load. When the load impedance is infinite, the two SG emulators will have the largest interaction. In addition, the constant power load (CPL) is a static load that only influences large signals. At each small signal time step, a CPL can be seen as a load with certain impedance, thus the stability analysis of a two-generation system with CPL should be the same with the CIL.

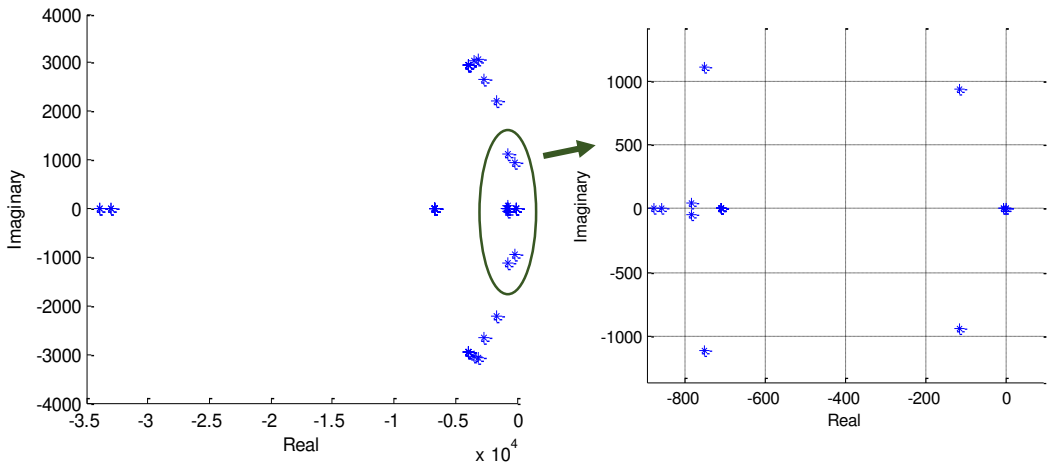


Fig. 7-17. Poles in Y_{1dd} when $R_L = 0.5\ \Omega$ and $L_L = 0$.

As a conclusion, SG emulators have the largest influence on each other with constant current load from the control design point of view, when only static or passive loads are considered. Assuming that each SG emulator is stable with the load separately, the control parameters only have to satisfy the stable conditions described in (7-1), which is much easier than (7-3) to (7-5).

7.3 Verification of the Developed SG Emulators in a Two-Area System

In this section, experiments are performed in the two area system to verify the HTB emulation. The structure of the two-area system is shown in Fig. 2-3. Because the emulators used in the HTB are based on mathematical models of different power system components, the validation is carried out mainly through comparison between experimental and simulation results by Matlab/Simulink.

The original and rescaled parameters used in the two-area system are shown in Table 4-1 and Table 7-2. P_{TLbase} and V_{TLbase} in the original system are the base power and voltage for normalizing the transmission lines. In preliminary experiments, transmission lines are represented by inductors, and lower power and voltage level, 1.3 kVA and 61 V are chosen. In reality, the real inductance

of an inductor is varying with up to ±20% error from the name tag value. At the same time, the equivalent serial resistance representing copper loss and core loss of an inductor can be much different from the transmission line parameters in the textbook. Because of the above reasons and the absence of capacitors, power flow in the emulated two area system will be different from the original. In order to ensure the same operating condition of the simulated and emulated system, measured inductance and resistance values in the HTB system are used in the simulation, as listed in Table III.

Table 7-2. Transmission Line Parameters Before and After Rescaling.

Name	**Original**	**Rescaled**	**Measured**
P_{TLbase}	100 MVA	15 kVA	–
V_{TLbase}	230 kV	208 V	–
f_{base}	60 Hz	60 Hz	–
L1-6	0.0417 p.u	2.8 mH	2.45 mH
L2-6	0.0167 p.u	1.1 mH	1.2 mH
L6-7	0.01 p.u	0.7 mH	0.7 mH
L7-9	0.11 p.u	7.6 mH	10 mH
L3-10	0.0417 p.u	2.8 mH	2.5 mH
L4-10	0.0167 p.u	1.1 mH	0.7 mH
L9-10	0.01 p.u	0.7 mH	0.7 mH
R1-6	0.0025 p.u	0.0648 Ω	0.12 Ω
R2-6	0	0	0.04 Ω
R6-7	0.001 p.u	0.026 Ω	0.035 Ω
R7-9	0.011 p.u	0.285 Ω	0.65 Ω
R3-10	0.0025 p.u	0.0648 Ω	0.12 Ω
R4-10	0	0	0.035 Ω
R9-10	0.001 p.u	0.026 Ω	0.035 Ω

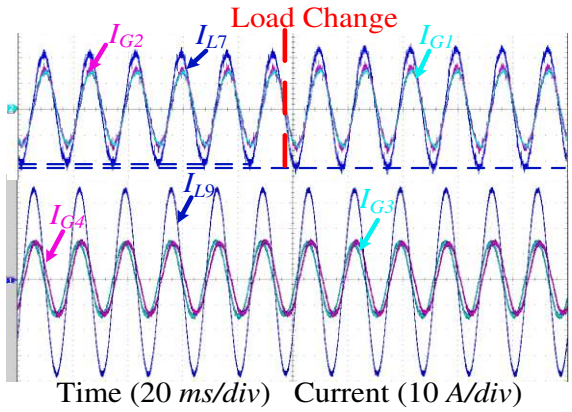
At the same time, generator models with the same equations as (4-16) are also developed in Simulink. Simulation of the generators is realized according to Fig. 3-7, where the calculated three phase voltages are given as input signals to drive three "Controlled Voltage Source" blocks in Simulink. These ideal voltage sources can precisely replicate their input signals. Both of the Simulink and HTB systems are implemented with AGC, automatic voltage regulator (AVR), and power system stabilizer (PSS). In AGC, $B_1 = 21$, $K_I = 0.05$, and in AVR, K_A=200, T_e=0.01 [81]. The capacitors on bus 7 and 9 are combined with the Load 7 and 9 as ZIP loads, which consist 20% constant Z, 20% constant I, and 60% constant P in both simulation and experiment. The operating point of the two-area system is shown in Table 7-3.

Table 7-3. Generator and load operating point (p.u) in Kundur's system.

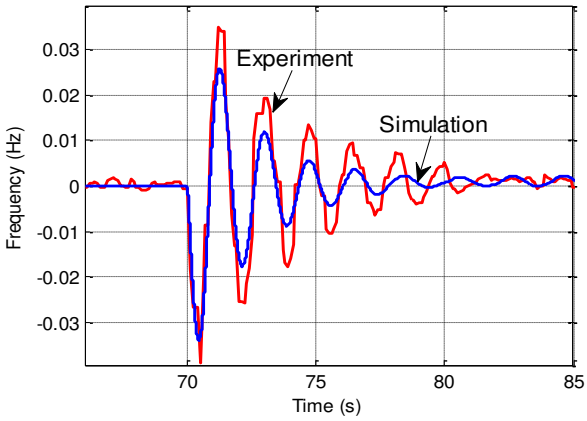
G1 active power	G2 active power	G3 active power	G4 active power	C7 reactive power
0.78	0.78	0.8	0.78	0.209
L7 active power	L7 reactive power	L9 active power	L9 reactive power	C9 reactive power
1.07	0.11	1.96	0.11	0.208

To observe different modes in the two-area system, a step change in the active power at load 7 from 1.07 p.u to 1.17 p.u is applied. Simulated and experimental results of generator frequency, output power response, voltage amplitude of different buses, and inter-area mode (frequency difference between generator 1 and 3 during the disturbance are compared and demonstrated in Fig. 7-18. The above experimental data are acquired from LabVIEW with 10 Hz sampling frequency.

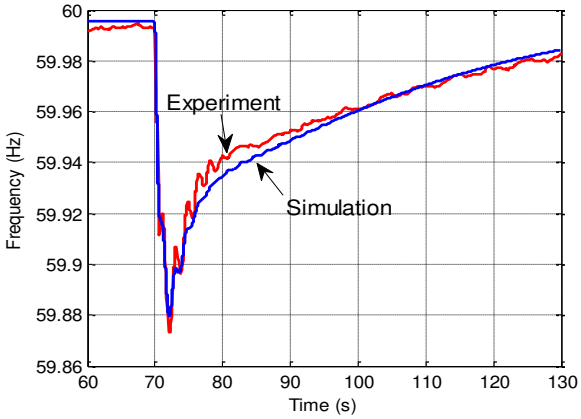
Fig. 7-18. Comparison between simulation and experimental results of the two-area system during the disturbance.



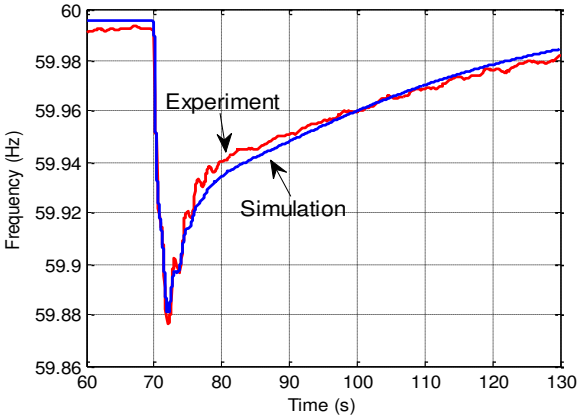
(a) Current output of each emulator



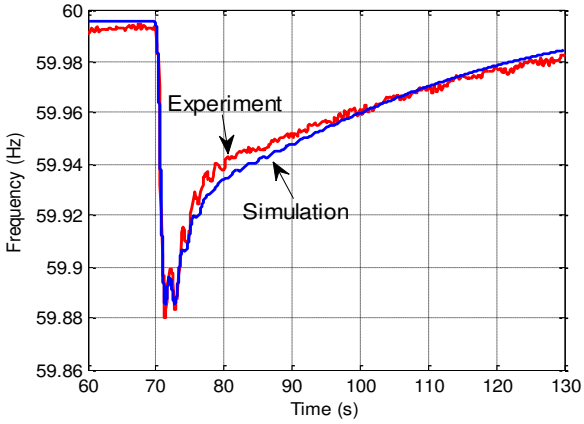
(b) Inter-area mode



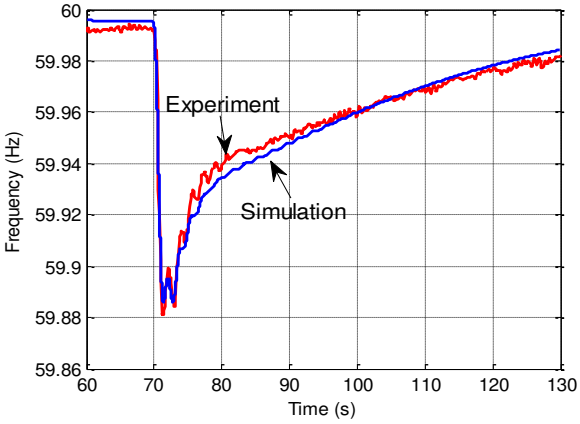
(c) Generator 1 frequency response during disturbance



(d) Generator 2 frequency response during disturbance

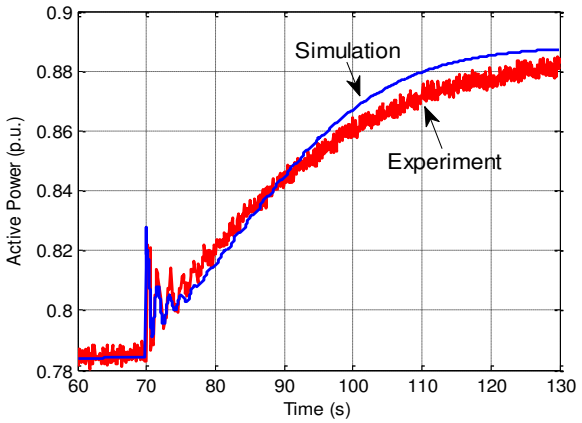


(e) Generator 3 frequency response during disturbance

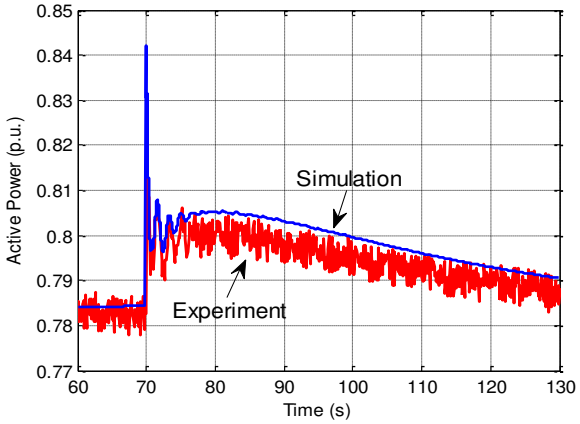


(f) Generator 4 frequency response during disturbance

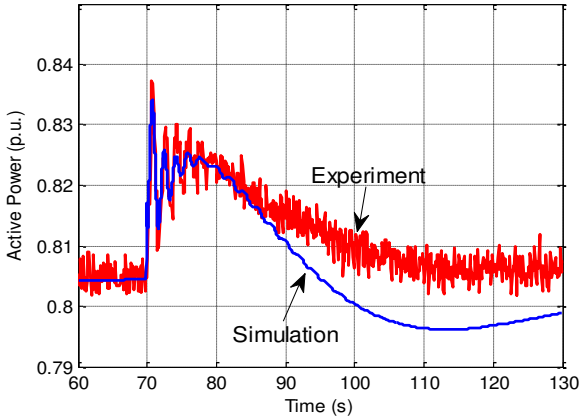
Fig. 7-18 continued.



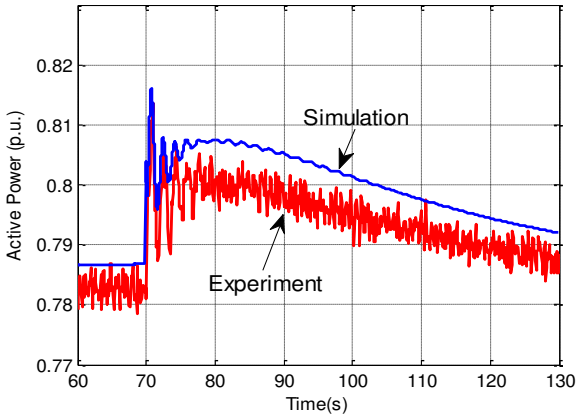
(g) Generator 1 output active power during disturbance



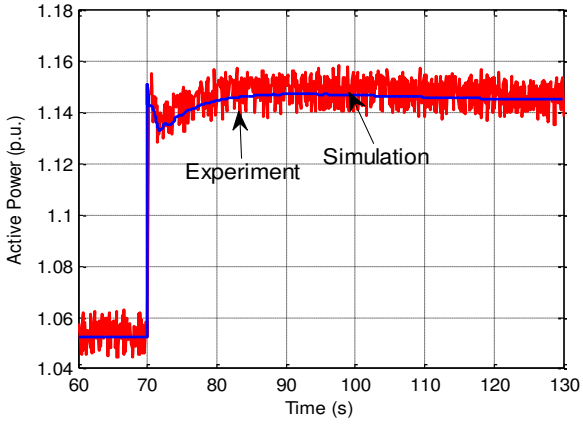
(h) Generator 2 output active power during disturbance



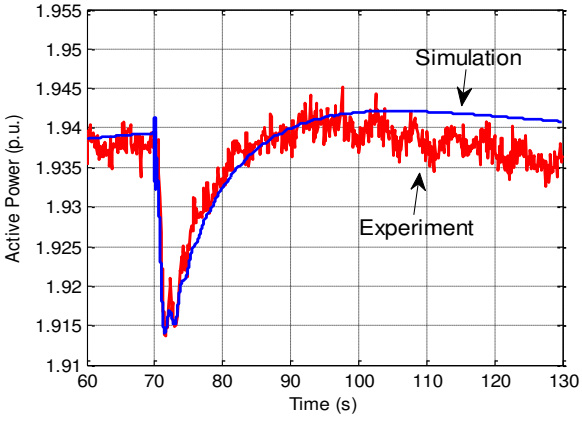
(i) Generator 3 output active power during disturbance



(j) Generator 4 output power during disturbance

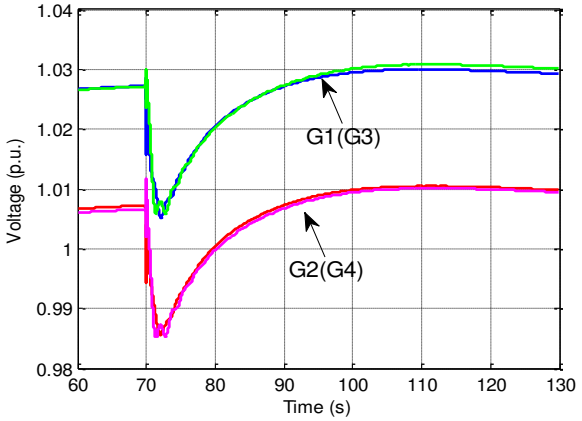


(k) Load 7 power consumption during disturbance

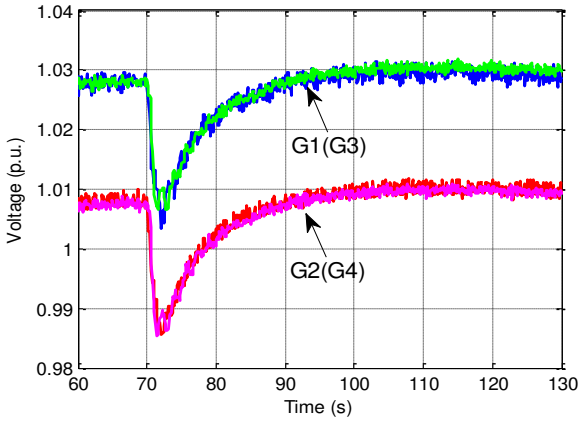


(l) Load 9 power consumption during disturbance

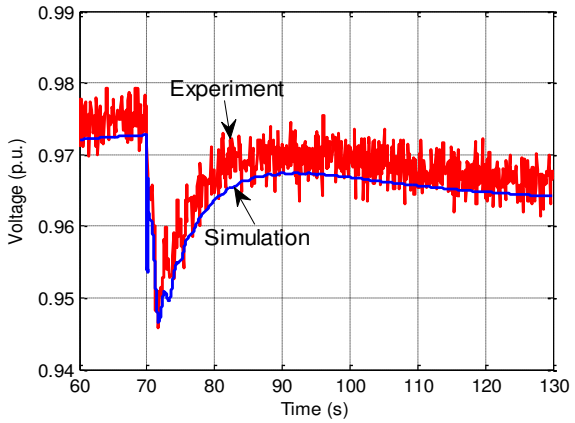
Fig. 7-18 continued.



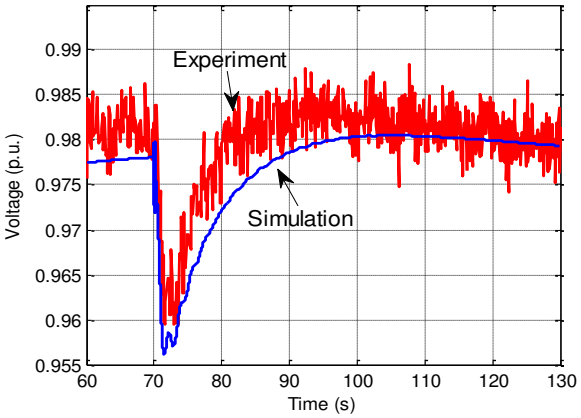
(p) Voltage amplitude of bus 1, 2, 3, and 4 in simulation



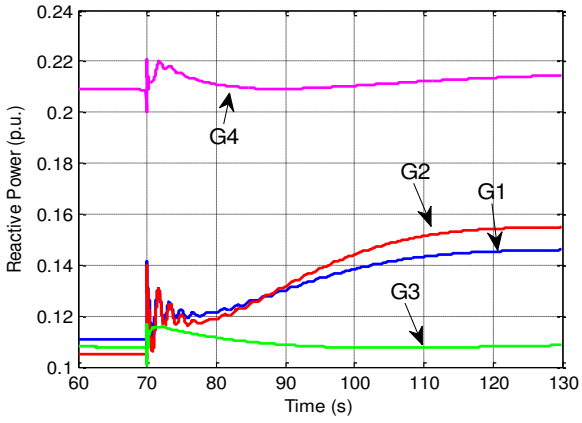
(q) Voltage amplitude of bus 1, 2, 3, and 4 in experiment



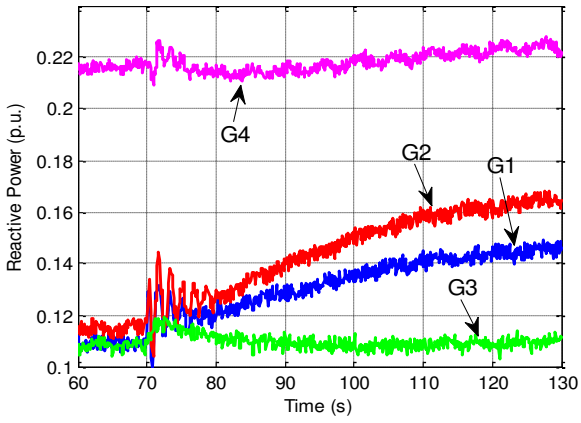
(m) Bus 7 voltage amplitude during disturbance



(n) Bus 9 voltage amplitude during disturbance



(o) Reactive power output of each generator in simulation



(r) Reactive power output of each generator in experiment

Fig. 7-18 continued.

Fig. 7-18 (a) shows the output current of the generator emulator 1-4 and the input current of load emulator 7 and 9 during the disturbance. As demonstrated in Fig. 7-18 (b), the inter-area mode is obtained by subtracting generator 1 to 3 frequency data with the same time stamp. Simulation and experimental result match well in oscillation frequency, but with a slightly different damping ratio. Frequency and output power response from each generator and load emulator during the disturbance are demonstrated in Fig. 7-18 (c)-(l). Voltage amplitude of bus 1-4, 7 and 9, and reactive power output of each generator emulator are shown in Fig. 7-18 (p)-(r). In Fig. 7-18 (b)-(l), (m), and (n), blue curves indicate simulation results, while red curves experimental results. In Fig. 7-18 (p)-(o), and (r), G1-G4 indicates the output of each generator 1-4. The profile of each curve in the experiment is the same as the simulation result with very small error. The discrepancies between the simulation and experimental results are mostly caused by two reasons. First, the converters in the HTB are designed for much higher power ratings than what are used in the experiment. The voltage and current sensors are not accurate enough for subtle changes. Second, copper and core loss in an inductor is very hard to obtain. Some of the inductors used in the HTB, such as line 1-6, 2-6, 7-9, and 3-10 are DC inductors, which are designed for a comparatively narrower working range than AC inductors, and thus have higher loss with alternating current. The difficulty of getting the accurate resistance/loss of an inductor will cause differences in the simulation and experimental results. Therefore, emulating long transmission lines with proper models is of great importance in the HTB. Ongoing work is being conducted in this area by using a back-to-back converter. In conclusion, the HTB is capable of representing a target power grid system correctly and accurately, thereby can be used for various power system research and experiments.

7.4 Conclusion

The instability in a two-generation system is mainly caused by the combination of the 4^{th}-order SG model and the voltage controller in the converter. Especially when a single integral controller is applied, the converter output impedance is much larger compared with PI controller. The current feed-forward is beneficial to the system stability since it decreases the emulator output impedance. When the load impedance amplitude is infinite, i.e., constant current load, the two SG emulators have the largest interaction between each other. Therefore, assuming that each SG emulator is stable with the load, the control design of the interconnected SG emulators has to guarantee no RHP poles in $[Y_s]$ considering only passive loads.

8 Synchronous Generator Emulation under Symmetrical Fault

In this chapter, the 6th-order SG model including the transformer voltages and saturation effect is adopted for fault scenarios. Control parameters are designed according to the error evaluation and performance target. The developed emulator is verified in both three-phase and line-to-line fault conditions. Stability with the developed emulator in the same two-generation system is also studied.

8.1 SG Model under Fault Condition

In a simple three-phase RL circuit, as demonstrated in Fig. 8-1, the short circuit current is composed of two elements: a transient unidirectional component and a steady-state ac component, as shown in Fig. 8-2. Similarly, if a three-phase fault is applied at the terminal of an SG, the short circuit current will also include the above two components. The difference is that in the SG short-circuit case, the magnitude of the fundamental frequency component will decay very rapidly in the first beginning and then slowly later on to a steady-state value, as shown in Fig. 8-3. On *dq*-axis, the fundamental frequency component of the three-phase current is reflected as dc component, while the unidirectional component as a fundamental component.

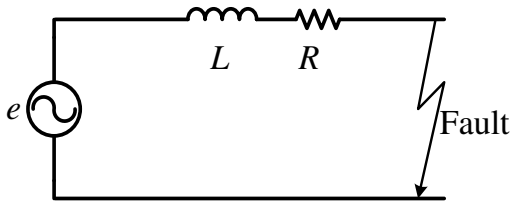


Fig. 8-1. *RL* circuit.

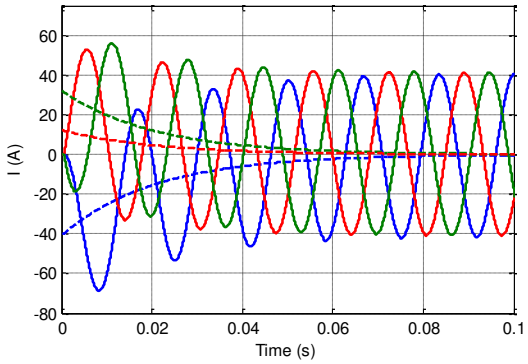


Fig. 8-2. Short-circuit current in a *RL* circuit.

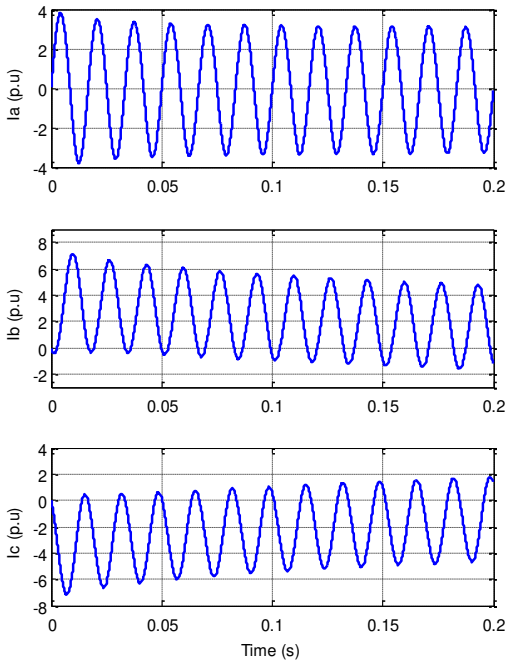


Fig. 8-3. Short-circuit current in an SG at its terminals.

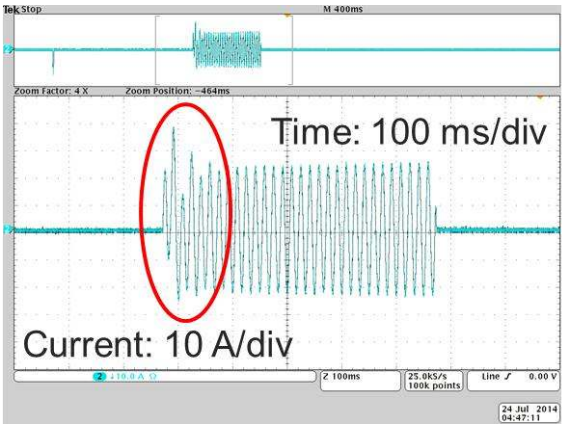
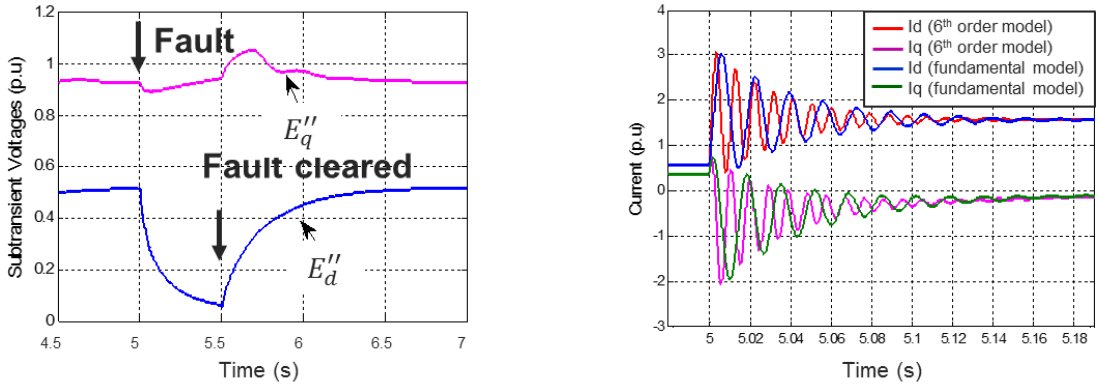


Fig. 8-4. SG emulator phase A fault current.

However, short-circuit at the terminal of a VSC based emulator is not feasible, thus requiring a transmission line with a certain distance between the emulator terminal and the shorted point. An experiment is set up with the same architecture shown in Fig. 8-1, where *e* works as an SG emulator with 4th order SG model, $L = 3.8\ mH$, and $R = 0.155\ \Omega$. In the experiment, the fault condition is realized by controlling the three-phase terminal voltage of a converter to be zero. The phase A fault current, as demonstrated in Fig. 8-4, performs distinctly from Fig. 8-3. Besides the DC offset, harmonics of other frequencies also exist in the first few cycles. Similar phenomenon happens when 6th order SG model is adopted. The higher order harmonics in fault currents are actually caused by the omission of transformer voltages. In power system study or simulation environment, the network solution is solved by phasor based methods, where the frequency is assumed to be constant and the state variables of the line inductors and capacitors are ignored. The system solution including SG models can be significantly simplified by neglecting the transformer voltages, which eliminates the fundamental frequency component on *dq*-axis caused by three-phase DC offset. Yet in real analog systems, where the frequency dependent components of the network cannot be neglected, the derived SG models become asymmetrical on *abc*-axis without

transformer voltages, especially without the voltage drop on subtransient reactance $pX_d''i_d$ and $pX_q''i_q$. Fig. 8-5 demonstrates the comparison results between 6th order and the current type fundamental SG model in MATLAB/Simulink. The 6th order model is developed by using control blocks and control voltage sources, while the fundamental model is provided by the SimPowerSystems library with the same parameters. Apparently the current oscillation amplitude and damping ratio are the same in the two models, while oscillation frequency is 60 Hz in the fundamental model versus around 100 Hz in the 6th order model.



(a) Subtransient back EMF (b) SG output current on *dq*-aixs

Fig. 8-5. Simulation comparison between 6th order and current type fundamental SG model.

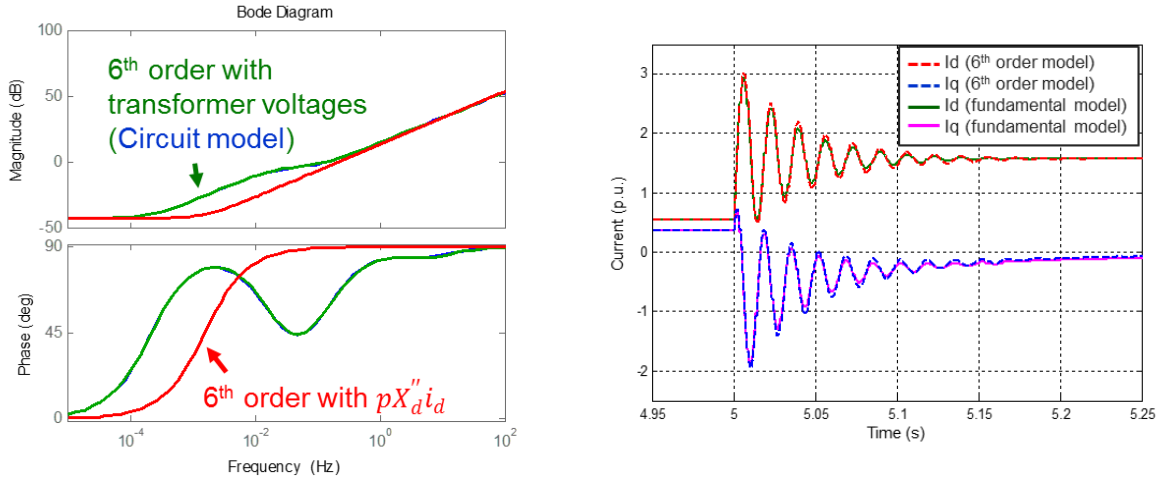
The relationship between the *d*-axis and *q*-axis flux linkages and the subtransient voltages is given by:

$$\begin{aligned} \psi_d &= E_q'' - X_d''i_d \\ \psi_q &= -E_d'' - X_q''i_q \end{aligned} \tag{8-1}$$

Combining (4-2) and (8-4), the SG model on the stator can be rewritten as:

$$u_d = E_d'' - R_a i_d + X_q'' i_q + pE_q'' - X_d'' p i_d$$
$$u_q = E_q'' - R_a i_q - X_d'' i_d - pE_d'' - X_q'' p i_q \quad (8\text{-}2)$$

Different from Fig. 4-1, the 6th order SG model overlaps with the fundamental/circuit model on both Z_{gdd} and Z_{gqq} by adding the transformer voltages. In fact, the 6th order SG model can achieve the same behavior with the fundamental model by only adding $pX_d'' i_d$ and $pX_q'' i_q$. As shown in Fig. 8-6 (a), the amplitudes with different models are the same at medium and high frequency range. In simulation, the 6th order model with $pX_d'' i_d$ and $pX_q'' i_q$ is compared with the circuit model provided by the Simulink library, as demonstrated in Fig. 8-6 (b). The fault currents in the two models match perfectly. Therefore, the 6th order model with $pX_d'' i_d$ and $pX_q'' i_q$ is applied in the following work.



(a) Bode plot of Z_{gdd} SG models

(b) Fault current on dq-axis in simulation

Fig. 8-6. Comparision between 6th order model with transformer voltages and the circuit mode.

In addition, saturation effects are also included in the SG model. The representation of saturation is based on the open-circuit characteristics (OCC) relating its terminal voltage amplitude

(flux linkage) and excitation current [81]. Assume that there is no magnetic coupling between dq-axis, the open-circuit saturation curve used in this work, obtained from Example 3.3 in [81], is demonstrated in Fig. 8-7. Since the SG model is a salient pole machine, saturation only affects the *d*-axis parameters.

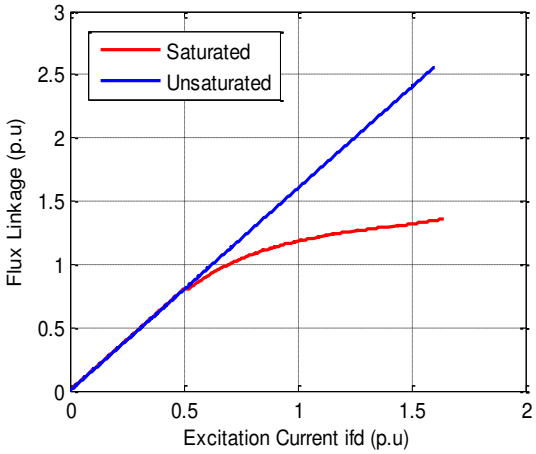


Fig. 8-7. Open-circuit saturation curve.

8.2 Performance Evaluation and Current Feed-forward Parameters

8.2.1 Three-Phase Symmetrical Fault

Assume that the voltage source in Fig. 8-1 $e = E_m \sin(\omega t + \alpha)$, the fault current can be calculated as:

$$i = Ke^{-\frac{R}{L}t} + \frac{E_m}{Z}\sin(\omega t + \alpha - \phi) \tag{8-3}$$

where $Z = \sqrt{R^2 + \omega^2 L^2}$, $\phi = tan^{-1}(\omega L/R)$, $K = i_0 - \frac{E_m}{Z}\sin(\alpha - \phi)$, and i_0 is the current value at $t = 0^-$ [81]. Apparently the current amplitude is related to the network impedance and the

voltage angle if the system is open-circuit before fault. In order to obtain accurate network parameters, experiments with converter open-loop control have been conducted. As demonstrated in Fig. 8-8, the duty cycle of the converter is given as $D_d = 0.735$ and $D_q = 0$, and the DC side voltage is 136 V. Three different cases have been performed to evaluate the line parameters. In each case, the fault happens when the voltage angle of phase A, B, or C is zero, thus creating the largest current on the corresponding phase, as shown in Fig. 8-9 to Fig. 8-11. Since the system is open-circuit before faults happen, assume that the inductance is much larger than the resistance, the fault current in each case on the phase with zero voltage angle becomes:

$$i = \frac{E_m}{Z} e^{-\frac{R}{L}t} - \frac{E_m}{Z} \sin(\omega t) \tag{8-4}$$

The fault currents on the rest two phases with non-zero voltage angle are decided not only by the network parameters, but the corresponding voltage amplitudes when faults happen in each case. Therefore, applying the fault at zero voltage angle can exclude the impact of voltage amplitude on the fault current characteristics. Therefore, the line impedance on each phase can be obtained by curve fitting of the current when the voltage angle is zero, i.e. phase A current in Fig. 8-9, phase B current in Fig. 8-10, and phase C current in Fig. 8-11. The line impedances are then calculated as $L_{T1} = 3.8$ mH and $R_{T1} = 0.14\ \Omega$ in phase A, 3.7 mH and 0.07 Ω in phase B, and 3.8 mH and 0.07 Ω in phase C under 150 μs delay. This set of parameters can perfectly align all the simulated and the experimental currents on the phase with zero voltage angle, as shown in Fig. 8-9 to Fig. 8-11. Even though discrepancies exist for the other two phases in each case, they can still be used for validation of the developed SG emulator.

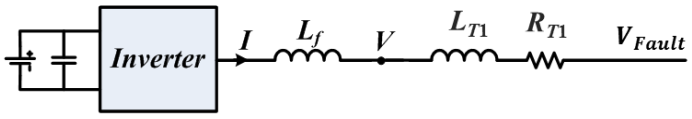
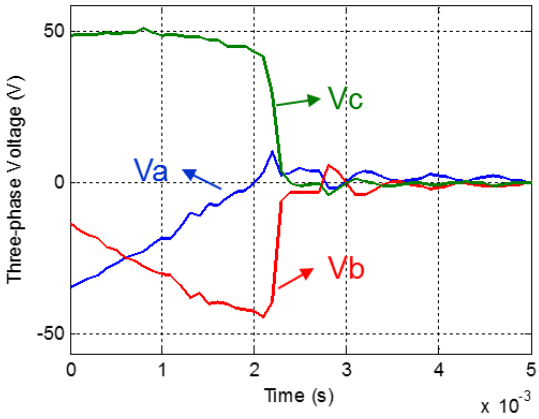
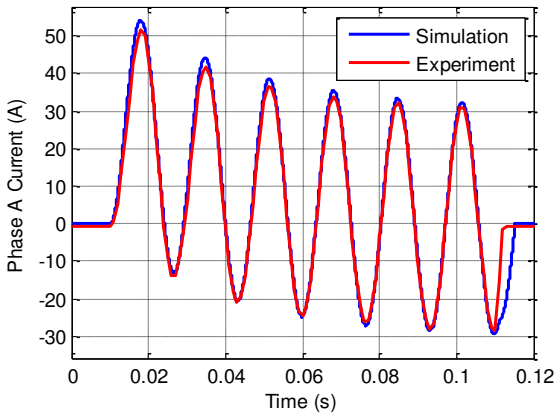


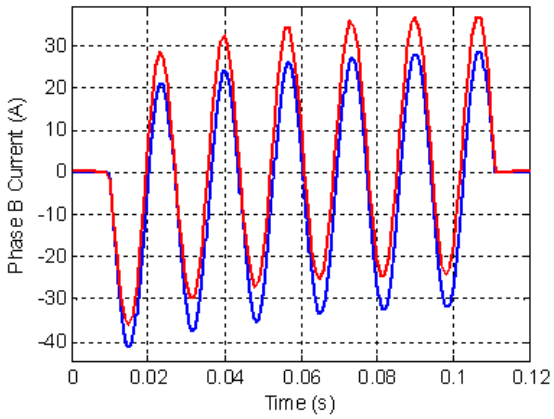
Fig. 8-8. Experiment structure to test network parameters.



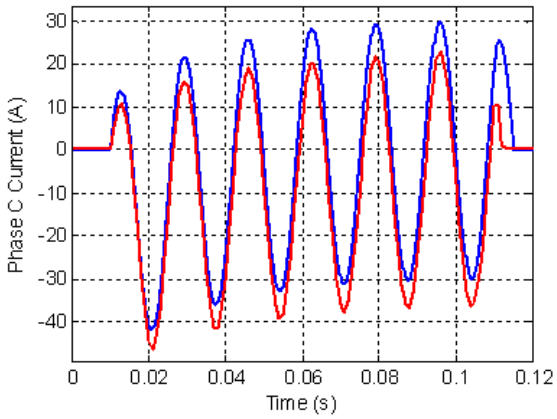
(a) Three-phase fault voltages in experiment



(b) Phase A fault current

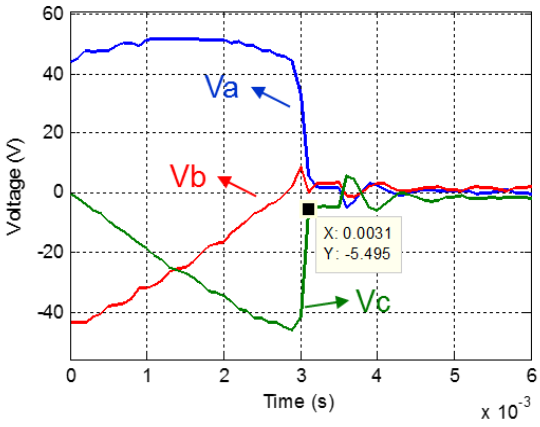


(c) Phase B fault current

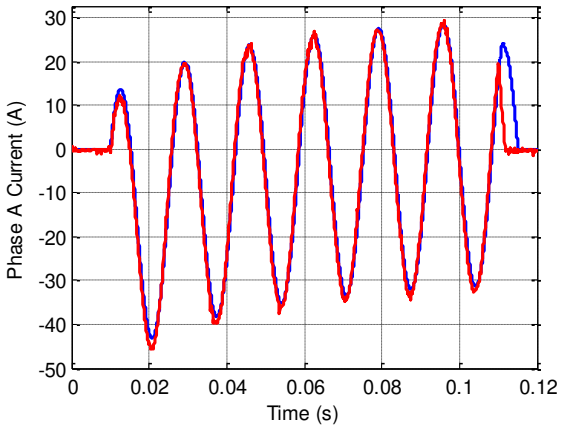


(d) Phase C fault current

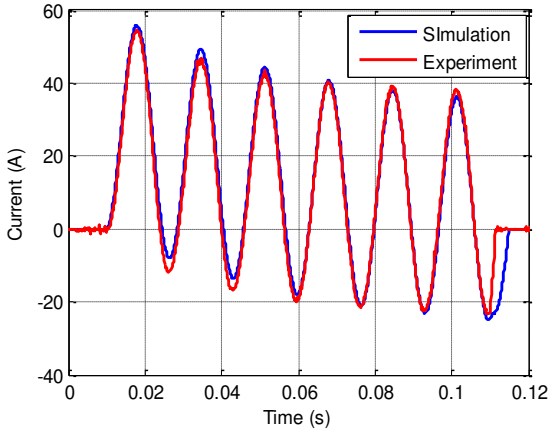
Fig. 8-9. Comparison between experimental and simulated fault data with converter open-loop when phase A voltage angle is zero.



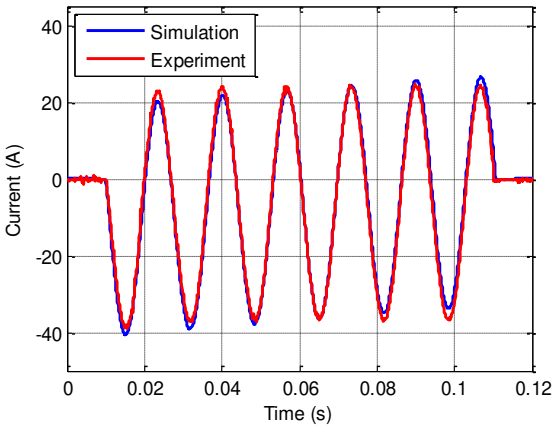
(a) Three-phase fault voltages in experiment



(b) Phase A fault current

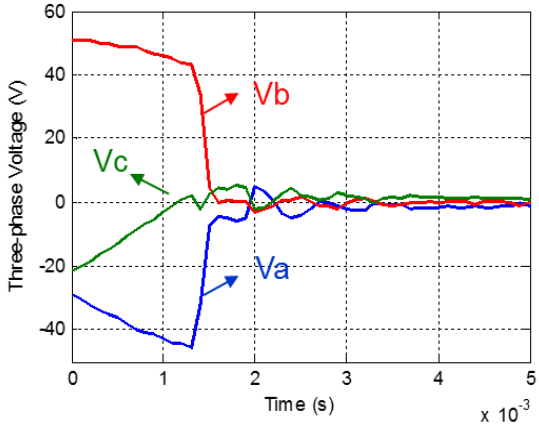


(c) Phase B fault current

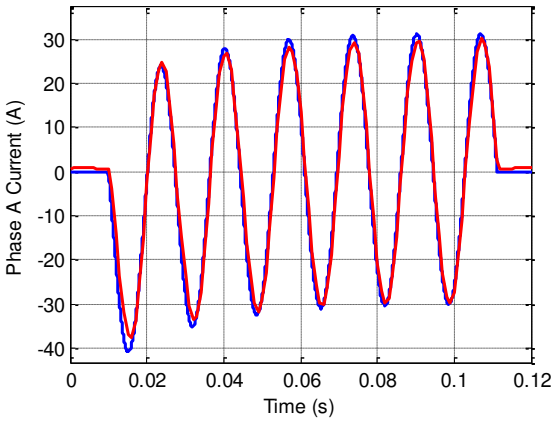


(d) Phase C fault current

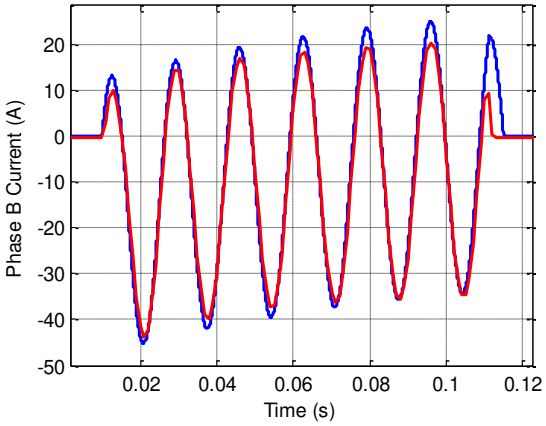
Fig. 8-10. Comparison between experimental and simulated fault data with converter open-loop when phase B voltage angle is zero.



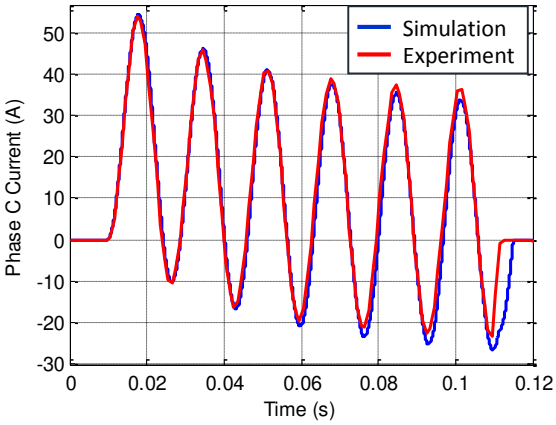
(a) Three-phase fault voltages in experiment



(b) Phase A fault current



(c) Phase B fault current



(d) Phase C fault current

Fig. 8-11. Comparison between experimental and simulated fault data with converter open-loop when phase C voltage angle is zero.

Three-phase symmetrical short-circuit can be seen as an extreme case of overload. As mentioned in chapter 5, errors caused by a PHIL interface will grow with the increasing load power consumption. One reason is that the converter output impedance is comparatively small when the load impedance is large, thus imposing negligible influence on the system response. In overload condition, where the load impedance is now small enough, the converter output impedance cannot be ignored and will significantly impact the system response.

Table 8-1. SG emulation error with different control parameters under fault condition (%).

Control parameters		**Amplitude**		**Phase**	
K_pK_i	K_i	A_{ERd}	A_{ERq}	P_{ERd}	P_{ERq}
0.02	5	6.04	36.46	6.89	11.90
0.02	20	2.51	15.40	2.19	3.68
0.02	30	2.68	16.63	3.18	4.62
0.1	30	4.1	25.36	6.28	9.16

As mentioned in chapter 6, the TFP error can decrease by increasing PI parameters properly. However, the target performance cannot be obtained without current feed-forward. As demonstrated in Table 8-1, the smallest TFP error that can be achieved is 15.4% on magnitude when $K_pK_i = 0.02$ and $K_i = 20$. Two experiments with different control parameters are conducted to demonstrate the errors in time domain. In the first case, $K_pK_i = 0.02$ and $K_i = 5$, while $K_pK_i = 0.02$ and $K_i = 20$ in the second case. The phase A fault currents in the experiments are compared with simulation in Fig. 8-12. As estimated by the TFP based error, parameters in the first case cause a much larger phase error than in the second case.

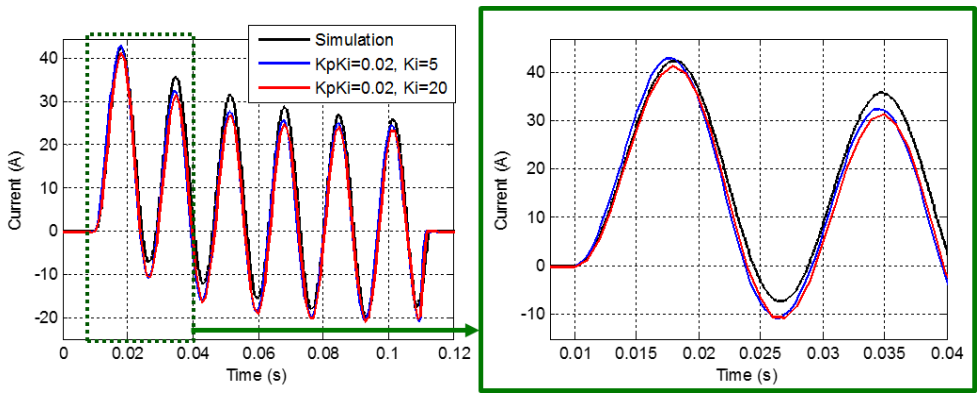
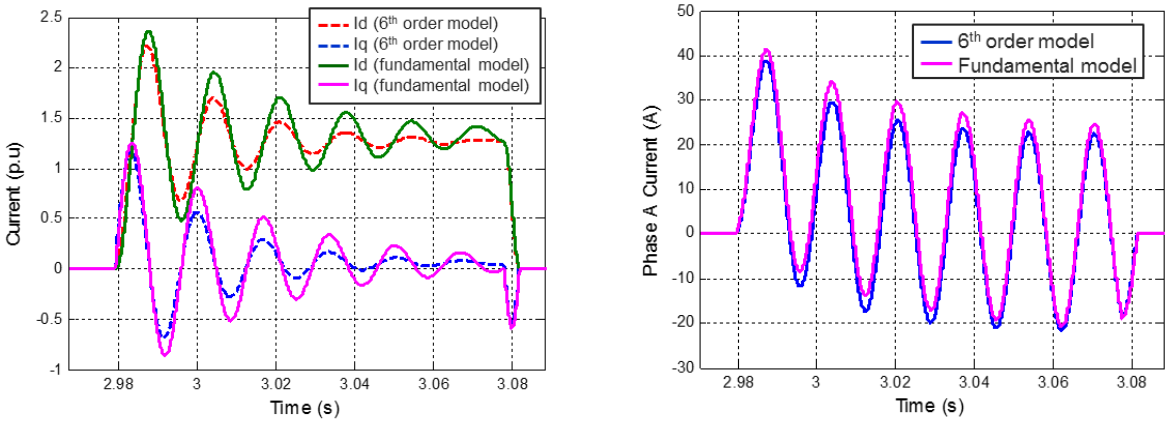


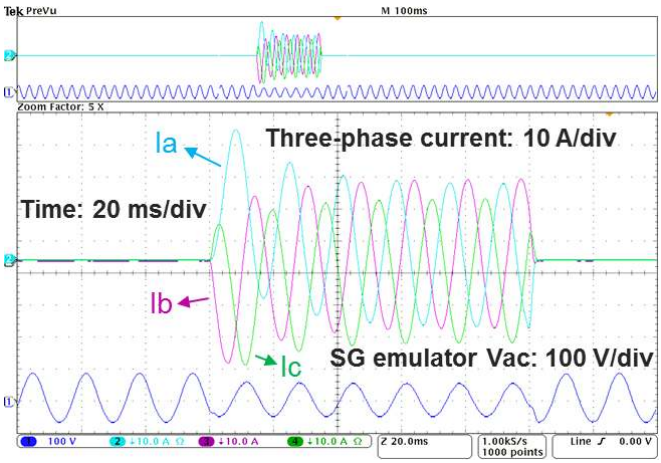
Fig. 8-12. Phase A fault current comparison between simulation and experiments when current feed-forward is not applied.

In addition, another reason that causes large error on emulation is the LPFs applied on $pX_d''i_d$ and $pX_q''i_q$ in the SG model to avoid high frequency noise caused by differentiators. In this work, the cutoff frequency of the LPFs is set as 500 Hz, which alters the frequency response of the original SG model. As shown in Fig. 8-13, the LPF in the 6th order SG model decreases the fault current amplitude.

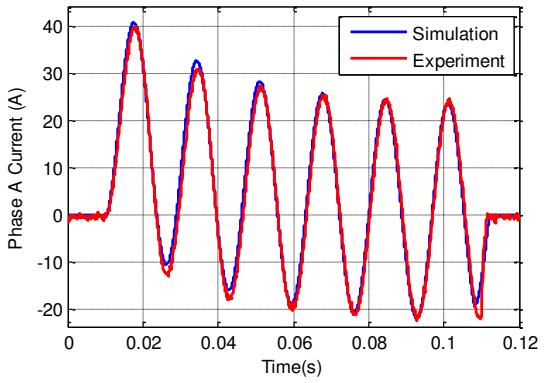


(a) Fault current on *dq*-axis (b) Phase A current

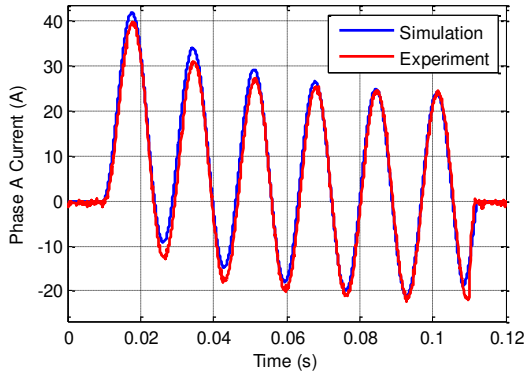
Fig. 8-13. Simulation comparison between the 6th order model with LPF and fundamental model.



(a) Experimental result



(b) Phase A current compared to SG model with LPF



(c) Phase A current compared to SG model without LPF

Fig. 8-14. Comparison between experimental and simulated fault current with SG emulator.

If the emulation target is the SG system with LPFs, the PI controller parameters can be designed as $K_p = 0.001$ and $K_i = 20$, and the current feed-forward parameters can be designed as $L_{fc} =$ 0.6 mH and $R_{fc} = 0.05\ \Omega$ to achieve the performance with 2.18% largest error on amplitude and 1.19% on phase. To verify the design, experiments with the structure shown in Fig. 8-8 have been performed. In both experiment and simulation, the fault happens when phase A voltage angle is zero and lasts for 0.1 s. Simulation data with fundamental SG model and the same network parameters is utilized as benchmark result. As demonstrated in Fig. 8-14, the phase A current of

the developed SG emulator match very well with the simulation when the LPFs are included in the SG model, while with visible discrepancies compared to SG model without LPFs, where the TFP error is 27.61% on magnitude and 4.9% on phase.

When $K_pK_i = 0.02$ and $K_i = 30$, the TFP based error with different current feed-forward parameters are shown in Table 8-2. The performance target can be achieved when $L_{fc} = -0.8$ mH and $R_{fc} = 0.05\ \Omega$. The fault currents with different current feed-forward parameters are shown in Fig. 8-15, and the comparison between the simulation and experiment when $L_{fc} = -0.8$ mH is demonstrated in Fig. 8-16. In accordance with the error estimation, the experimental result matches very well with the benchmark simulation, which validates the accuracy of the estimation.

Table 8-2. SG emulation error with different current feed-forward parameters when $K_pK_i = 0.02$ and $K_i = 30$ under fault condition (%).

Control parameters		**Amplitude**		**Phase**	
L_{fc}	R_{fc}	A_{ERd}	A_{ERq}	P_{ERd}	P_{ERq}
0.6 mH	0.02 Ω	4.21	26.35	5.59	8.04
-0.8 mH	0.05 Ω	0.73	4.62	0.62	1.03
-1.8 mH	0.05 Ω	9.67	60.72	5.92	9.15

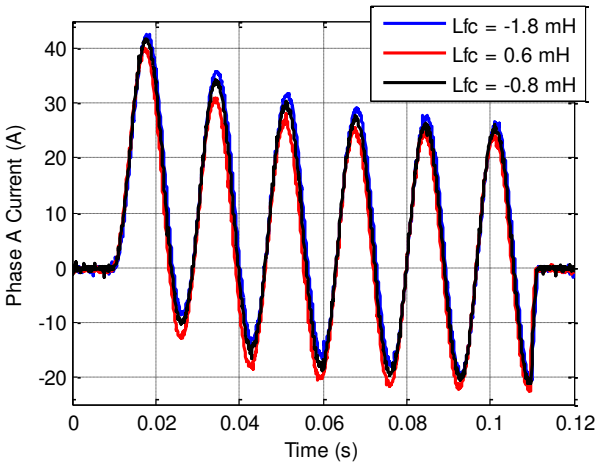
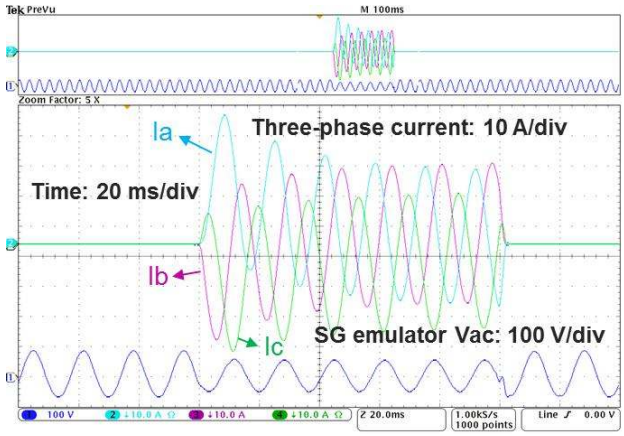
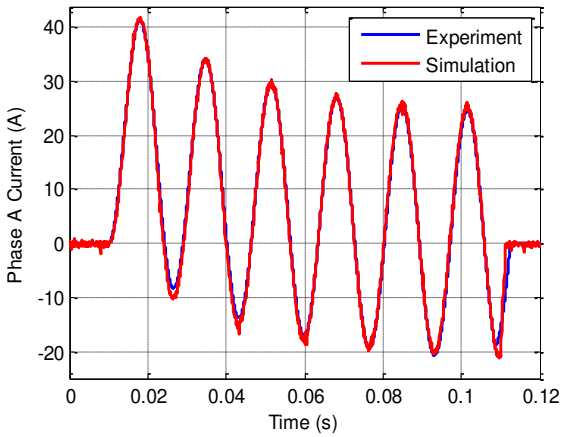


Fig. 8-15. Phase A fault current when $L_{fc} = 0.6$ mH, -0.8 mH and -1.8 mH.



(a) Experimental results.



(b) Comparison between simulated and experimental fault current.

Fig. 8-16. Comparison between simulated and experimental fault current when $L_{fc} = -0.8$ mH and $R_{fc} = 0.05\ \Omega$.

Table 8-3. SG emulation error with different current feed-forward parameters when $K_pK_i = 0.02$ and $K_i = 20$ under fault condition (%).

Control parameters		**Amplitude**		**Phase**	
L_{fc}	R_{fc}	A_{ERd}	A_{ERq}	P_{ERd}	P_{ERq}
-0.2 mH	0.02	1.61	9.8	1.7	2.98
-0.4 mH	0.09	0.74	4.8	1.61	2.60
-0.6 mH	0.09	2.15	13.76	2.86	4.44

The current feed-forward parameters are designed according to different PI controllers, therefore the performance target can be achieved through various combinations. Assume that $K_pK_i = 0.02$ and $K_i = 20$, the TFP based error with different current feed-forward parameters are shown in Table 8-3. In this case, the TFP error difference between the three current feed-forward parameters in Table 8-3 is not very obvious, as verified by the current waveforms demonstrated in Fig. 8-17 and Fig. 8-18.

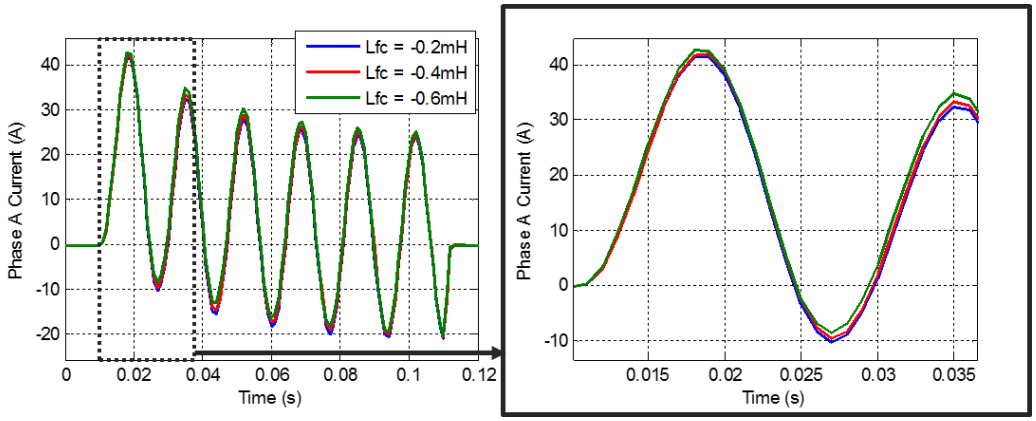


Fig. 8-17. Phase A fault current when $L_{fc} = -0.2$ mH, -0.4 mH and -0.6 mH.

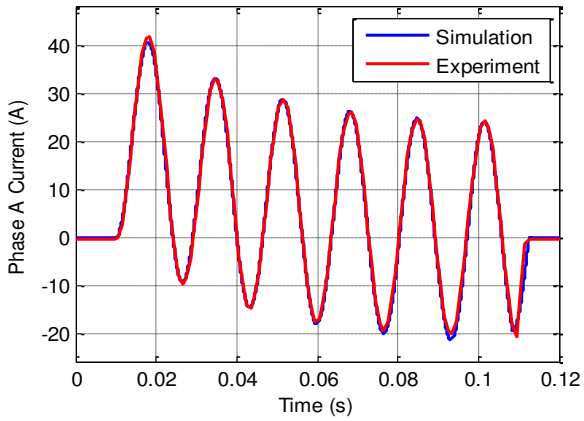


Fig. 8-18. Comparison between simulated and experimental fault current when $L_{fc} = -0.4$ mH and $R_{fc} = 0.09\ \Omega$.

The above experiments are conducted while disabling the mechanical model of the SG emulator, thus resulting in constant rotor speed. With the mechanical model, the experimental results are compared with the simulation in Fig. 8-19 to Fig. 8-21, where the fault happens when phase B voltage angle is zero. Fig. 8-19 shows the line-to-line terminal voltage V_{ac} and three-phase currents of the developed SG emulator in the experiment. The comparison results of the fault currents and the rotor speed in simulation and experiment are satisfactory. At the same time, the converter voltage controller has very good steady-state and dynamic performance, as demonstrated in Fig. 8-21.

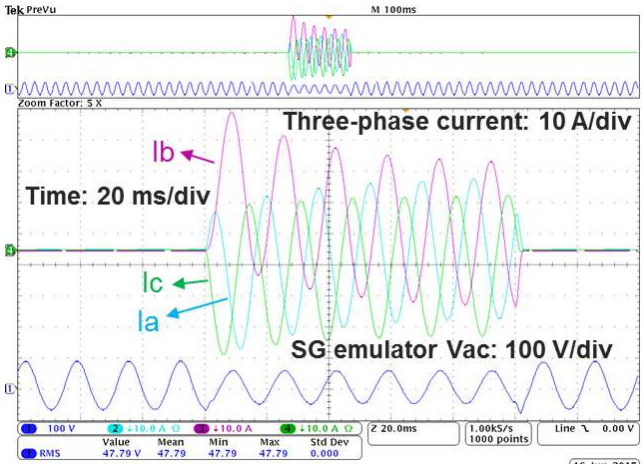
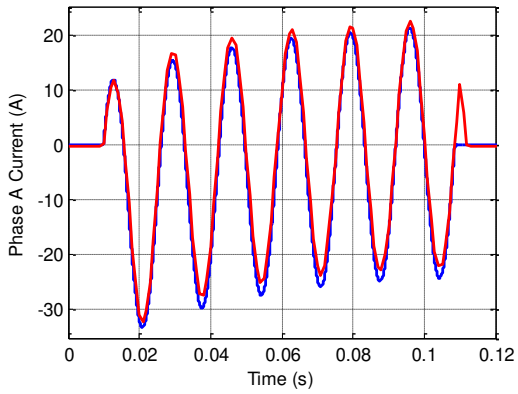
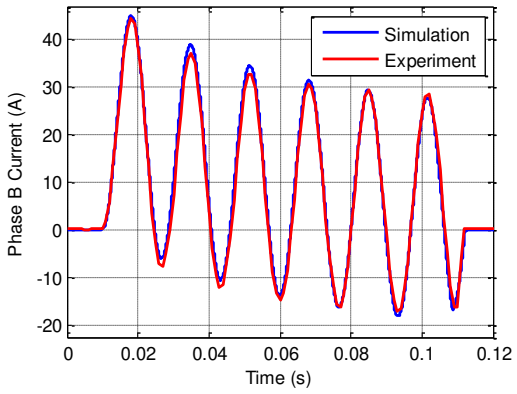


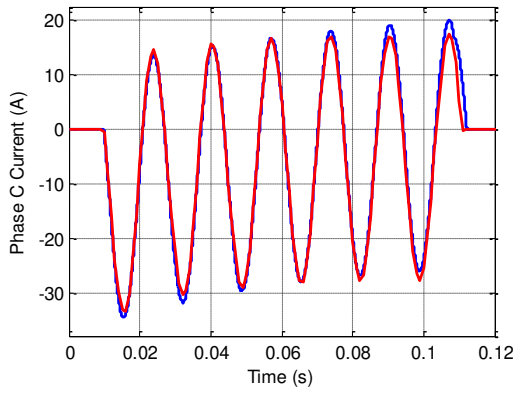
Fig. 8-19. Experimental results with rotor speed variation



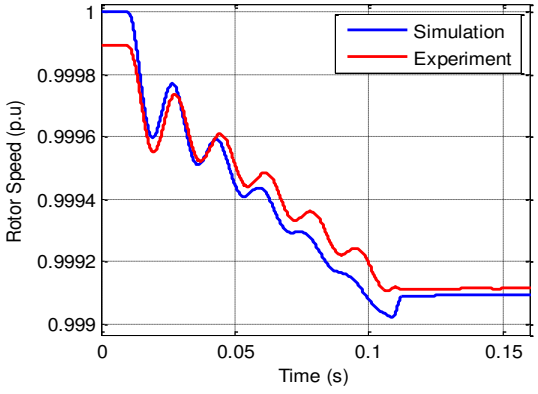
(a) Phase A current during fault



(b) Phase B current during fault

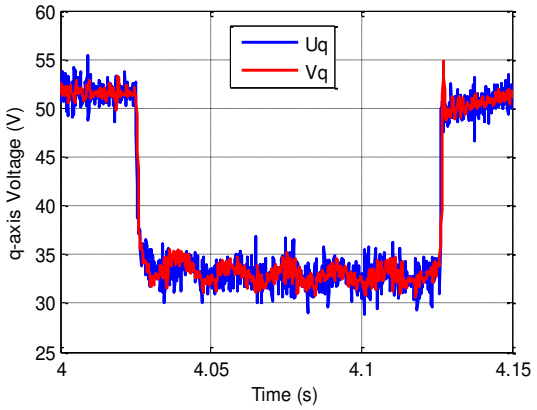


(c) Phase C current during fault

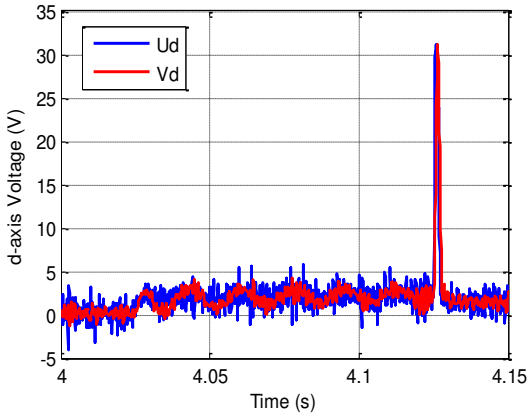


(d) Rotor angle during fault

Fig. 8-20. Verification of the experimental results considering rotor speed variation.



(a) Voltage reference and actual output voltage on *d*-axis



(b) Voltage reference and actual output voltage on *q*-axis

Fig. 8-21. SG model voltage references and acutal emulator ouput voltages on *dq*-axis.

8.2.2 Asymmetrical Fault

Asymmetrical faults are another important part of research in power system transient stability analysis. There are three types of Asymmetrical faults: single-line-to-ground, double-line-to-ground, and the line-to-line fault. In power system study and IEEE Standard 1110-2002, symmetrical components are widely applied to simplify the computation under unbalanced faults [8][81]. The synchronous machine is then represented by positive-, negative-, and zero-sequence impedance.

The classical SG circuit model equations are based on several assumptions about its physical characteristics, such as the symmetry of armature windings, neglect of hysteresis effects and eddy currents, and so on. The unbalanced components do not cause any fundamental impact on these assumptions. Therefore the derivation of the sequence impedances in a synchronous machine is still based on the SG models described in chapter 4 [81]. In EMTP, the SG model on *dq0*-axis is used for both balanced and unbalanced system simulation.

Among the three types of asymmetrical faults, the first two involve additional negative- and zero-sequence components and the last only negative-sequence components. The SG model applied in the previous symmetrical fault emulation, however, does not include the zero sequence impedance, thus it is only suitable for emulating the line-to-line fault.

At the same time, zero sequence current is not allowed in the HTB, as discussed in chapter 2, thus the line-to-ground fault cannot be realized.

Since the impedances on the fault phases are the same with the symmetrical fault, the control parameters can then be designed based on the symmetrical fault. The following line-to-line experiment and simulation are conducted with the same network and control parameters. The fault happens on phase A and B when phase A voltage angle is zero. The zero-sequence current in the line-to-line fault is zero, thus resulting in opposite currents in the two phases, as demonstrated in Fig. 8-23 and Fig. 8-23. The phase currents in the experiment match very well with simulation, thus verifying the developed SG emulation.

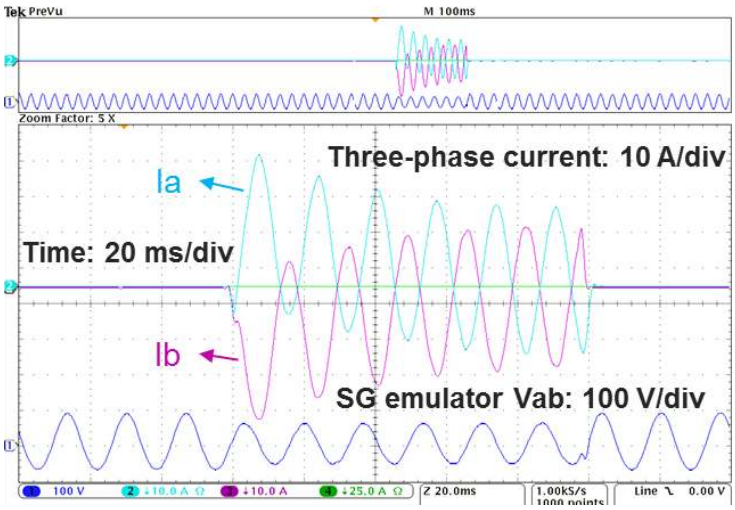
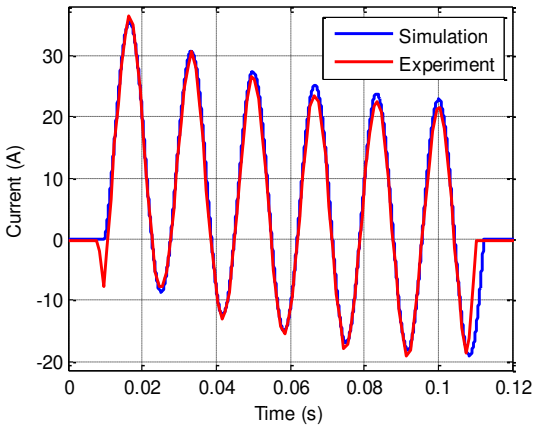
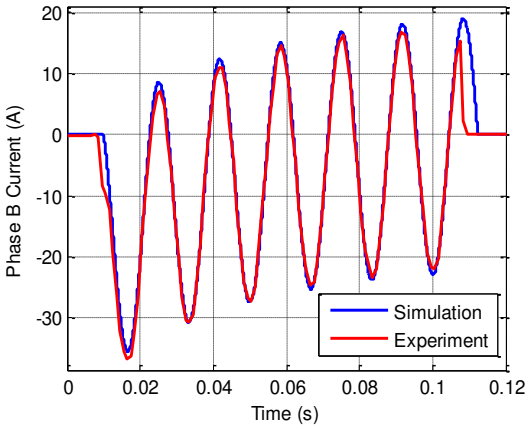


Fig. 8-22. Experimental voltage and currents with line-to-line fault on phase A and B.



(b) Phase A current



(c) Phase B current

Fig. 8-23. Comparison between experimental and simulation results with line-to-line fault on phase A and B.

8.3 Limitation of Converter Based Voltage Type Emulation

For voltage type emulator, a short-circuit fault condition cannot happen directly at the terminals of the emulator, as demonstrated in Fig. 8-24. Even though the large current in a fault condition leads to nearly zero voltage reference calculated in an SG model, the forced zero voltage at the terminals results in no controllability of the closed-loop voltage control implemented in the emulator. Even a small calculated voltage reference, such as 0.2 V, can create conflict between the control reference and target, and thus introduces large oscillating current. Therefore, a short line is required for the fault emulation to allow a certain degree of controllability.

However, the question is how large of a line impedance is needed for the stable emulation of an SG under fault condition. The system model under a three-phase short-circuit condition can be described as (8-5).

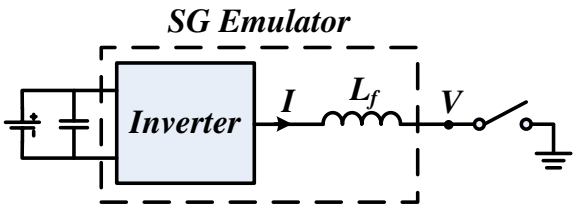


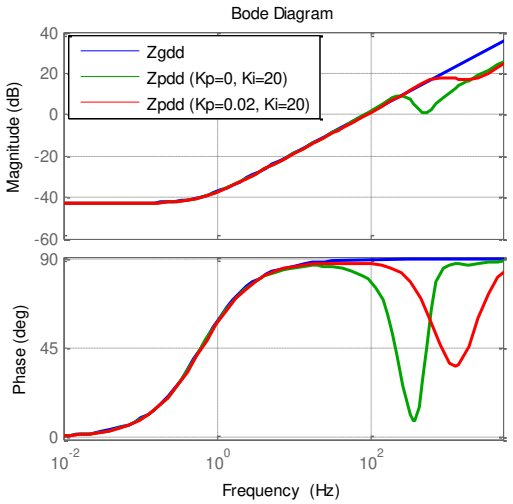
Fig. 8-24. SG emulator with short-circuit fault at the terminals.

$$[\Delta i_{dq}] = \left([Z_p] + [Z_T]\right)^{-1}[G_{vg}]E_{fd} \tag{8-5}$$

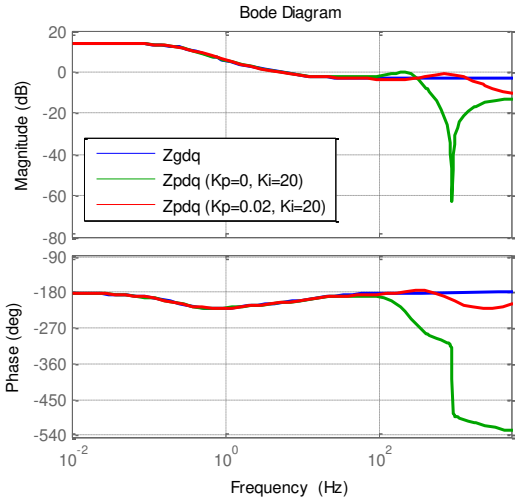
The stability of the system can be then determined by $\left([Z_p] + [Z_T]\right)^{-1}$. Based on the control parameters designed in section 8.2, the smallest impedance needed for stable emulation is around 1.2 mH. However, this critical value is also influenced by the discretization method in use. The same value is obtained when the backward Euler method is applied for the transformer voltages and the current feed-forward, while as low as 0.4 mH will result in a stable emulation when using the trapezoidal method in the simulation with converter switching model. Further study of the discrete system is therefore in need for more precise calculation and prediction.

At the same time, the time delay is another major factor that influences the stability. Larger time delay not only introduces larger error, as discussed in 6.2, but also results in larger line impedance needed in stable fault emulation. Theoretically, a converter with the switching frequency large enough to cover the control bandwidth is adequate for emulation purpose. But, a lower switching frequency also indicates larger time delay. With the same control parameters and bandwidth as mentioned above, the largest time delay that can ensure the stable fault emulation with 1.2 mH line impedance is around 430 μs (as low as 3-4 kHz switching frequency considering 1.5 cycles delay) in continuous model calculation.

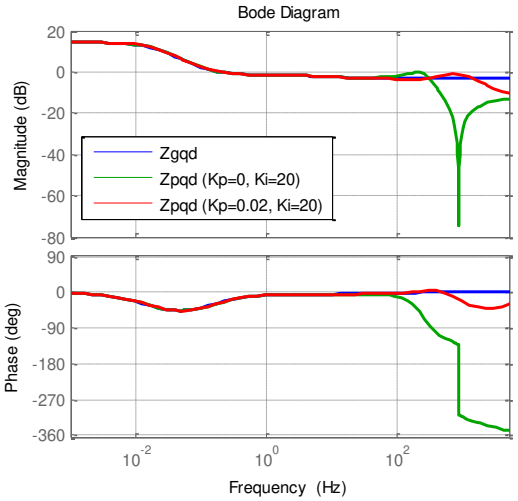
8.4 Stability of a Two-Generation System



(a) Bode plot of Z_{pdd} with varying PI parameters and Z_{gdd}



(b) Bode plot of Z_{pdq} with varying PI parameters and Z_{gdq}



(c) Bode plot of Z_{pqd} with varying PI parameters and Z_{gqd}

Fig. 8-25. Bode plot of Z_p and Z_g with transformer voltages.

As discussed in chapter 7, the stability issues in the interconnection of SG emulators are caused by the combination of the 4th-order SG model and the converter voltage control. Especially the converter output impedance Z_{cdd} and Z_{cqq} are much larger than the SG model impedance Z_{gdd} and Z_{gqq} (stator resistance R_a), and the phase response of the resulting emulator output impedance Z_{pdd} and Z_{pqq} is out of the passive range (-90° to 90°) at the medium and high frequency range. When the transformer voltages $p\psi_d$ and $p\psi_q$ are taken into consideration, the SG model impedance Z_{gdd} and Z_{gqq} become inductive at medium and high frequency range, thus creating positive incremental amplitude response on the frequency domain, as demonstrated in Fig. 8-6. This inductive output impedance will shape the emulator characteristics and decrease the emulation error. As shown in Fig. 8-25, the SG emulator output impedance Z_{pdd} has much less deviation from the SG model than the previous study where the 4th-order SG model is adopted. Even when $K_p = 0$, with which the two-generation system has RHP poles in chapter 7, the phase response of Z_{pdd} is still within the passive range, which is beneficial to the overall system stability.

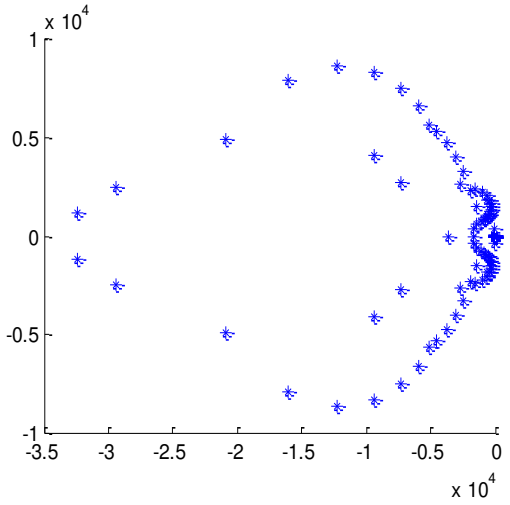


Fig. 8-26. Plot of Y_{sdd} poles with SG 6th-order model including transformer voltages.

The stability of the two-generation system with the same power stage and network parameters as described in 7.2.1 is evaluated again here, incorporated with the 6th-order SG model applied in the three-phase fault. With the control parameters $K_p = 0$ and $K_i = 20$, the poles of the characteristic admittance Y_{sdd} are plotted in Fig. 8-26.

Clearly, Y_{sdd} does not have any RHP poles, neither do the rest of the components in $[Y_s]$. As a conclusion, the stability of the interconnected SG emulator system can be largely improved by including the transformer voltages.

8.5 Conclusion

The transformer voltages in the SG model are needed in the fault conditions to ensure correct performance. Higher frequency harmonics will appear when the transformer voltages are not included. The emulator cannot be faulted at its terminal. First, it is voltage controlled and the controller will fight with the forced zero voltage at its terminal. Second, when the filter inductance is very small, fault current can easily exceed the device ratings and trigger protection even if the emulator is current type. Since LPFs are added on the transformer voltages to avoid high frequency noises, the SG model itself in the emulator creates error. This error can be compensated by choosing proper feed-forward parameters. In this case, the parameters of the differential current feed-forward are negative, instead of positive like in chapter 5. In addition, the stability of a two-generation system with transformer voltages is improved significantly, because the transformer voltages can shape the emulator output impedance and constrain the frequency response with the passive region, even though the amplitude of Z_{gdd} and Z_{gqq} is much larger than with 4th-order SG model.

9 Conclusion and Future Work

9.1 Conclusion

In this paper, an SG emulator with high accuracy is developed in a hardware testbed for various testing scenarios. The interface algorithm is selected, converter control is designed, stability issues with interconnected SG emulators are studied, and the emulator is verified through fault conditions as well as a two-area system. The key points included in this dissertation could be summarized as follows:

1. Improved IAs are needed only when time delay is very large and open loop control is used. Voltage type ITM is selected for SG emulation since the generator is the only voltage source in the HTB system. Closed-loop voltage control is applied to compensate the phase lag caused by time delay in low frequency.

2. The control design targets of an SG emulator is to have large enough bandwidth and small converter output impedance. A single voltage controller is adequate for the converter topology with only inductor filter, since the inductance is small enough and its voltage drop can be ignored compared with the load. A current feed-forward can further decrease the difference between the emulator and the target SG. This feed-forward can reduce the amplitude of the converter output impedance Z_{cdd} and Z_{cqq} without increasing PI parameters, especially when the load impedance is small.

3. The TFP method compares the transfer function of the original system without the converter interface and the PHIL system on the frequency domain. Since a frequency domain response includes not only magnitude but phase characteristics, the TFP error should inspect both aspects. The calculation results verify that the current feed-forwad can decrease the error in the

frequency range of interest. At the same time, the error is also related to the amount of time delay as well as loading conditions. With the increase of the load power consumption, the error will increase under the same control parameters. To gurantee the performance target under various conditions, the control parameters should be designed for the worst case scenario such as faults. In addition, the converter influence on the closed-loop control, AVR, is very small as long as the emulator performance target is achieved.

4. The instability in a two-generation system is mainly caused by the combination of the 4th-order SG model and the voltage controller in the converter. Especially when a single integral controlled is applied, the converter output impedance is much larger compared with PI controller. The current feed-forward is beneficial to the system stability since it decreases the emulator output impedance. The small signal model with three different output variables are established for the system with constant impedance load. When the load impedance amplitude is from zero to infinite, it can provide some level of damping to the system. Therefore, the control design of the SG emulators with passive loads has to guarantee the stability of with constant current load, assuming that each emulator is stable with the load.

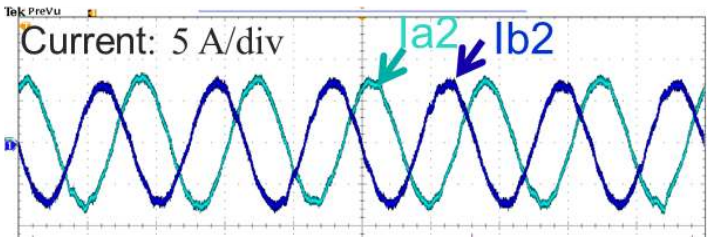
5. The transformer voltages in the SG model are needed in the fault conditions to ensure correct performance. Higher frequency harmonics will appear when the transformer voltages are not included. Since LPFs are added on the transformer voltages to avoid high frequency noise, the SG model itself in the emulator creates error. This error can be compensated by choosing proper feed-forward parameters. In addition, the stability of a two-generation system with transformer voltages is improved significantly, because the transformer voltages can shape the emulator output impedance and constrain the frequency response with the passive region, even though the amplitude of Z_{gdd} and Z_{gqq} is much larger than with 4th-order SG model.

9.2 Future Work

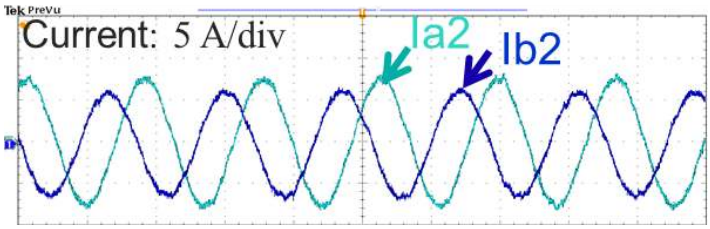
Based on the research conducted for this dissertation, the following future works are recommended:

1. Current Type SG Emulator.

Even though the voltage type SG emulator has many benefits as discussed in chapter 3, it also introduces problems. When multiple SG emulators are interconnected, unbalanced current can be easily created. This unbalanced current is caused by voltage sensor calibration error and the network inductors with unbalanced inductances. Experiments with the structure shown in Fig. 7-1 are conducted to demonstrate the idea. In Fig. 9-1 (a), the SG emulator 1 output current are balanced when the voltage sensing is correctly calibrated, while obvious unbalance can be observed in Fig. 9-1 (b) with 2% voltage sensing error.



(a) Correct sampling



(b) 2% error on voltage sampling of phase A to B

Fig. 9-1. SG emulator 1 current on phase A and B with different voltage sensing calibration.

Since a single voltage control loop is applied, the converters are not capable of regulating their output current, and thus unable to eliminate the unbalance problem. At the same time, the unbalanced current will result in unbalanced voltage reference, thus forming a positive feedback. In addition, since the load emulator regulates its output current, the unbalanced current only flows between the SG emulators. However, adding a current inner-loop to the voltage type emulator is not feasible, because the voltage loop control plant will then be absolutely determined by the varying load model.

One way to solve this problem is to develop current type SG emulators and use both the voltage and current type together within an area. Since the current type can regulate its output current, the unbalanced components can be removed between the SG emulators. The AVR now becomes the outer voltage loop to regulate the emulator terminal voltages, and the phase angle is obtained through the rotor model instead of nonlinear PLL. Fundamentally, the current type SG emulator can still be seen as a voltage source because of AVR, but its influence to the overall system stability needs to be further investigated.

2. Voltage Feedback before the Filter Inductor

As discussed in chapter 5, the major sources of the error in an SG emulator come from the voltage drop on the filter inductor and the time delay. Even though current feed-forward is proposed to compensate the voltage drop, the time delay coupled in the compensation loop can cause stability problems under certain capacitive loads. If the voltage feedback is extracted before the filter inductor instead of after, the voltage drop will not cause error anymore. However, this does not mean that an open-loop control can be applied. When the SG impedance is large enough, unstable cases can be created because of the time delay. Therefore, the closed voltage loop is only applied for compensating the phase lag caused by the time delay within the controller bandwidth,

and its performance is totally independent from the load model. In addition, the output filter can be used to represent a part of the stator inductance, but it also means that there is a limit on how small the SG parameters can be. By releasing part of the SG output impedance, the stability of the voltage type emulators can be further improved.

3. A Simpler Stability Criteria

In chapter 7, the stability problem with interconnected SG emulators are investigated by calculating the poles of the small signal models. This work is tedious and difficult with increasing number of branches, or with more complicated networks. Therefore, a simpler stability criteria is in the need.

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