Three-Phase PWM Boost–Buck Rectifiers With Power-Regenerating Capability

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***Abstract*—Three-phase pulsewidth-modulated (PWM) boost–buck rectifiers with power-regenerating capability are investigated. The converters under consideration are capable of: 1) both voltage step-up and step-down; 2) bidirectional power processing; and 3) almost unity-power-factor operation with nearly sinusoidal ac current. Expected advantages are: 1) applicability to lower voltage applications, e.g., direct retrofit to replace diode or thyristor rectifiers; 2) switching loss reduction in the inverter load; 3) low-order harmonic control in the inverter load output voltage; 4) blanking time effect mitigation in the inverter load; and 5) a modest level of voltage sag/swell compensation. In this paper, firstly, a step-by-step power stage derivation process is described. Then, taking the Ćuk–Ćuk realization as an example, its operating principle and modulation scheme are described. A steady-state model and dynamic model for controller design are also described. Representative results of circuit simulations and hardware experiments are presented. Through these procedures, the feasibility of the presented three-phase PWM boost–buck rectifier with power-regenerating capability is demonstrated.**

***Index Terms*—Boost–buck converter, power regeneration, pulsewidth-modulated rectifier.**

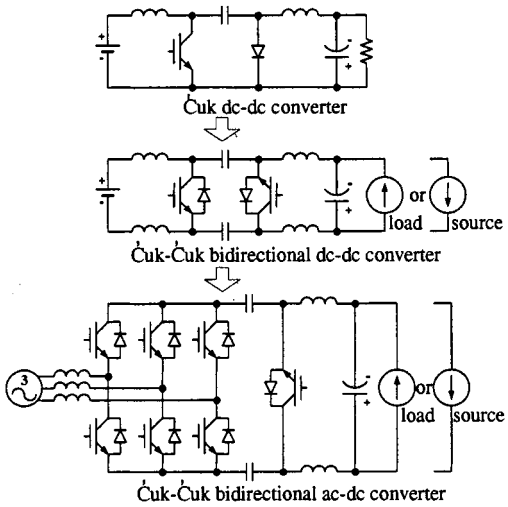

Fig. 1. Derivation of Ćuk–Ćuk bidirectional ac–dc converter.

I. Introduction

THE active rectifier front end of a pulsewidth-modulated (PWM) inverter drive has been attracting increased attention due to incessantly growing power quality concerns [1], [2]. A great amount of work has already been done concerning the three-phase PWM boost rectifier [3]–[7], and the buck rectifier [8]–[12]. The boost–buck-based active rectifier has, however, not yet been fully investigated. Although several three-phase boost–buck rectifiers have been reported thus far [13]–[15], none of these offers power-regenerating capability. Although [16] has shown a possible topology, no specific description of its operation has been presented.

In this paper, three-phase PWM boost–buck rectifiers with power-regenerating capability are discussed. The converters under focus are capable of: 1) both voltage step-up and step-down; 2) bidirectional power processing; and 3) almost unity-power-factor operation with nearly sinusoidal ac current. Expected advantages coming from these capabilities are: 1) applicability to lower voltage applications, e.g., direct retrofit to replace diode or thyristor rectifiers; 2) switching loss reduction in the inverter load; 3) low-order harmonic control in the inverter load output voltage; 4) blanking time effect mitigation in the inverter load, by decreasing the dc-link voltage depending on the operating condition. In addition, 5) a modest level of voltage sag/swell compensation is possible.

In the following sections, a power stage topology derivation, operating principle and modulation scheme, steady-state and dynamic modeling for controller design, and representative results of circuit simulations and hardware experiments are presented.

II. Power Stage Topologies

Figs. 1 and 2 illustrate power stage derivation of two three-phase ac–dc boost–buck bidirectional power converters. Their building blocks are three-phase voltage stiff converter (VSC) and boost–buck-based bidirectional dc–dc converters.

There exist two boost–buck-based dc–dc converters, namely, the so-called Ćuk [17] and the single-ended primary inductor converter (SEPIC) [18]. These two dc–dc converters are shown at the top of Figs. 1 and 2. They can be made bidirectional dc–dc converters by adding an antiparallel diode to the active switch and an antiparallel active switch to the freewheeling diode. This modification is shown in the middle of these figures, where the reactive components originally only on the upper rail are split into the upper and lower rails. Although the splitting of the reactive components does not make any change from the differential-mode behavior viewpoint, it is

Paper IPCSD 02–038, presented at the 2001 Industry Applications Society Annual Meeting, Chicago, IL, September 30–October 5, and approved for publication in the IEEE Transactions on Industry Applications by the Industrial Power Converter Committee of the IEEE Industry Applications Society. Manuscript submitted for review October 15, 2001 and released for publication June 11, 2002.

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Publisher Item Identifier 10.1109/TIA.2002.802910.

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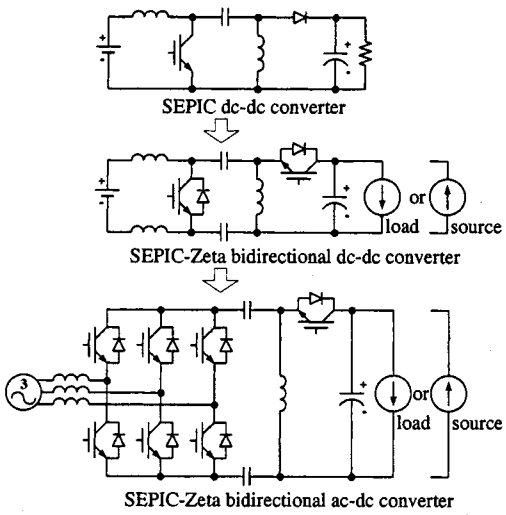


Fig. 2. Derivation of SEPIC–Zeta bidirectional ac–dc converter.

expected to have a common-mode electromagnetic interference (EMI) suppression effect because of their symmetrical structure. It may be noted that the Ćuk-based bidirectional dc–dc converter appears to be a Ćuk converter from both sides but the SEPIC-based bidirectional dc–dc converter is seen to be a SEPIC only from the left side and appears as a Zeta [19] from the right side. These bidirectional dc–dc converters can be made ac–dc converters by replacing their active switch/diode pair on the left side with a three-phase VSC bridge as shown at the bottom of the figures. In the following, the Ćuk–Ćuk realization will exclusively be discussed due to the limitation of space.

A similar power stage derivation is possible from a three-phase current stiff converter and buck–boost-based bidirectional dc–dc converters. This alternative is currently under investigation by the authors.

III. Operating Principle and Modulation Scheme

Whether during rectification or inversion, sinusoidal current shaping can be reduced to a voltage control in which the controlled voltage source (rectifier/inverter) is connected to an ac source through an inductance as shown in Fig. 3(a). The fundamental component phasor diagrams for unity-power-factor rectification and inversion are shown in Fig. 3(b). The desired converter ac terminal voltage can be defined as the hypotenuse of the right triangle composed of three voltage phasors. The modulation scheme is then discussed from the ac terminal voltage synthesis and power transfer viewpoint.

A. Rectifier Operation

Fig. 4 shows the power stage schematic for the purpose of rectifier operation analysis. The following discussions are based on the notation in Fig. 4. The operating principle of the boost–buck-based rectification has been presented in [14] and [15]. It has been made clear in these references the necessity of bridge-leg-short realized as unconventional zero-voltage space vectors to make power transfer happen. A variety of such zero-voltage space vectors can be classified into three groups, *viz.* the one-leg-short, two-leg-short, and three-leg-short zero-voltage space vectors [14]. In this paper, taking into account a tradeoff between average switching frequency and current-carrying capability required in the switching devices, the two-leg-short zero-voltage space vectors are selected as a reasonable compromise [20].

Fig. 5 illustrates the modulation scheme and the power transfer from the ac source to dc load during one triangle carrier period, where $v^*_{\mathrm{aca}} > v^*_{\mathrm{acb}} > v^*_{\mathrm{acc}}$ is assumed in the rectifier ac terminal voltage command and $i_a > 0 > i_b > i_c$ is assumed in the three-phase ac current. Once the operating principle in this particular condition is understood, all the other possible operating conditions can readily be derived in the same manner. Immediately below the triangle carrier waveform v_{carrier} are shown the well-known boost rectifier switching functions for reference purposes.

In Fig. 5(a), switching functions H_a–H_c and gate pulses g_1–g_6 are the same between the conventional boost rectifier and the boost–buck rectifier during the intervals in which active voltage space vectors are used as denoted as intervals x and y.

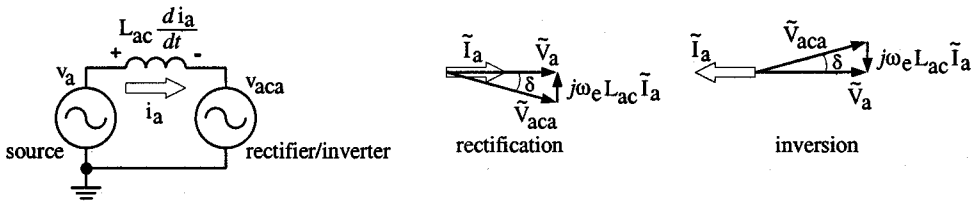
The most significant difference from the conventional boost rectifier is in interval z during which zero-voltage space vectors are applied. By turning on both the upper and lower switches in a phase leg, a coupling capacitor discharging current path is established, whereby power transfer from the coupling capacitors to the dc load is realized. Since diode D_7 is naturally turned off, shoot-through failure does not occur in the phase leg. The corresponding current paths are depicted at the bottom illustration of Fig. 5(b). Since the two-leg-short zero-voltage space vector is chosen here, two phases carrying negative currents, phases b and c, are the leg-short phases. If the ac current relation is $i_a > i_b > 0 > i_c$, phases a and b are the leg-short phases and $g_5 = \overline{g}_2 = 0$ in phase c. That is, two phases sharing the same ac current sign are the leg-short phases for the zero-voltage space-vector interval and the upper switch in the remaining phase leg stays on (off) and the lower switch stays off (on) throughout the carrier period if its ac current is positive (negative).

B. Inverter Operation

In inverter operation, the necessary phase-leg-short is naturally realized through antiparallel diodes in the three-phase bridge. Accordingly, the same gate pulses as in the conventional VSC can be applied. On the other hand, the switch on the dc link, S_7, must actively operate. Fig. 6 illustrates the modulation scheme and power transfer from the dc source to ac load during one triangle carrier period, where $v^*_{\mathrm{aca}} > v^*_{\mathrm{acb}} > v^*_{\mathrm{acc}}$ is assumed in the three-phase bridge ac terminal voltage command and $i_a < i_b < 0 < i_c$ is assumed in the three-phase ac current. In addition, $|i_{L\mathrm{dc}}| > |i_c| = |i_a| + |i_b|$ is assumed.

During the intervals in which active voltage space vectors are used, as in intervals x and y in Fig. 6, the situation is basically the same as in the rectifier operation except the directions of the load current, dc inductor current, and power transfer. During these intervals, the energy stored in the coupling capacitor is discharged through the three-phase bridge to the ac load.

During the intervals in which zero-voltage space vectors are used, as in intervals z_o and z_7 in Fig. 6, the active switch on



(a) (b)

Fig. 3. Simplified per-phase equivalent circuit and phasor diagrams for unity-power-factor operation. (a) Per-phase fundamental component equivalent circuit for steady state. (b) Per-phase phasor diagrams for unity-power-factor operation (δ is power angle and ω_e is ac source angular frequency.

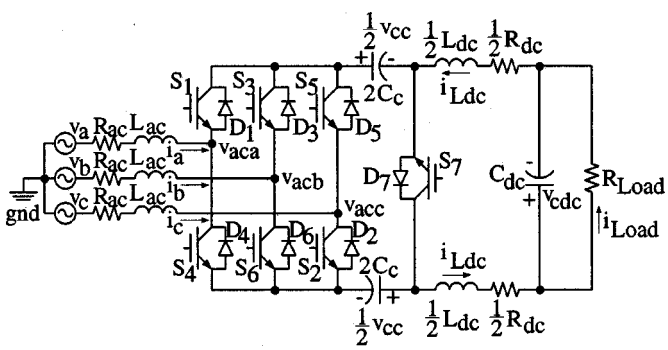


Fig. 4. Ćuk–Ćuk bidirectional ac–dc converter for analysis of rectifier operation.

the dc link is turned off, and the coupling capacitor is charged with $i_{L\mathrm{dc}}$. Since $|i_{L\mathrm{dc}}| > |i_c| = |i_a| + |i_b|$ is assumed, the amount of $|i_c|$ in $i_{L\mathrm{dc}}$ flows through the ac load and the extra amount, $|i_{L\mathrm{dc}}| - |i_c|$, flows through naturally shorted phase legs via their antiparallel diodes as illustrated at the top and bottom of Fig. 6(b). If $|i_{L\mathrm{dc}}|$ is less than the current flowing through the ac load, the extra amount of ac current flows through an active device in the bridge and the continuity of current flow is maintained. Such an active device is one of the lower devices for interval z_0 or of the upper devices for interval z_7.

It may be noted that, although the gate pulses in the three-phase bridge are the same as those of the conventional VSC, the zero-voltage space vector realized here are again unconventional ones because of the phase-leg-short through antiparallel diodes.

IV. Modeling and Analysis for Controller Design

The analytical model derivation is based on the power stage schematic shown in Fig. 4 where the ideal switches and zero equivalent series resistance (ESR) in the capacitors are assumed. The following matrix–vector form of equation can be derived from a set of differential equations with the assumption of the balanced three phase set of ac source and three-wire system, and applying the synchronous frame d–q transformation

$$\frac{dx}{dt} = Ax + Bu \tag{1}$$

$$x = [\, i_q \quad i_d \quad v_{cc} \quad i_{L\mathrm{dc}} \quad v_{\mathrm{dc}} \,]^T$$
$$u = v_q \tag{2}$$

$$A = \begin{bmatrix} -\dfrac{R_{\mathrm{ac}}}{L_{\mathrm{ac}}} & -\omega_e & -\dfrac{d_q}{L_{\mathrm{ac}}} & 0 & 0 \\ \omega_e & -\dfrac{R_{\mathrm{ac}}}{L_{\mathrm{ac}}} & -\dfrac{d_d}{L_{\mathrm{ac}}} & 0 & 0 \\ \dfrac{3}{2}\dfrac{d_q}{C_c} & \dfrac{3}{2}\dfrac{d_d}{C_c} & 0 & -\dfrac{d_z}{C_c} & 0 \\ 0 & 0 & \dfrac{d_z}{L_{\mathrm{dc}}} & -\dfrac{R_{\mathrm{dc}}}{L_{\mathrm{dc}}} & -\dfrac{1}{L_{\mathrm{dc}}} \\ 0 & 0 & 0 & \dfrac{1}{C_{\mathrm{dc}}} & -\dfrac{1}{C_{\mathrm{dc}} R_{\mathrm{Load}}} \end{bmatrix} \tag{3}$$

$$B = \begin{bmatrix} \dfrac{1}{L_{\mathrm{ac}}} & 0 & 0 & 0 & 0 \end{bmatrix}^T \tag{4}$$

where the arbitrary coefficient and the axes direction in the synchronous frame d–q transformation used here are following those in [21] and $v_d = 0$ due to the assumption that a axis and q axis coincide. In addition, by taking the local time average, the switching functions are replaced with the corresponding duty ratio. As in Fig. 5, when the rectifier is in the operating sector of $v^*_{\mathrm{aca}} > v^*_{\mathrm{acb}} > v^*_{\mathrm{acc}}$, the duty ratio in the synchronous d–q frame can be expressed as

$$d_q = \tfrac{1}{2}\, m \cos\delta$$
$$d_d = \tfrac{1}{2}\, m \sin\delta \tag{5}$$

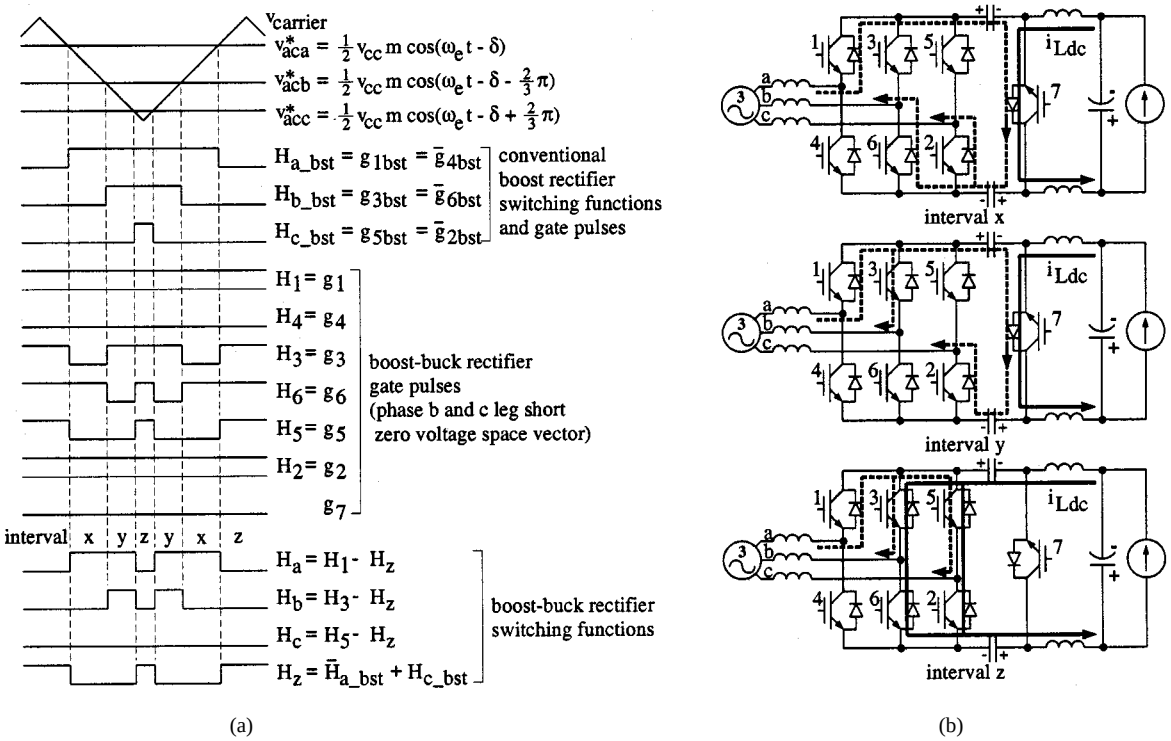
$$d_z = \langle (1 - H_{a_bst}) - H_{c_bst} \rangle = 1 - \frac{\sqrt{3}}{2}\, m \sin(\omega_e t - \delta) \tag{6}$$

where m and δ are the modulation index and modulation displacement angle, or power angle, respectively.

The same treatment can be applied to all the other operating sectors over a full fundamental frequency period. Fig. 7 shows duty ratio, d_q, d_d, and d_z over $0 \le \omega_e t \le 2\pi$ for a representative value of m and δ. Unlike the well-known boost or buck rectifier, even after the synchronous frame d–q transformation and local time averaging, the system is still time dependent for a fixed value of m and δ because of d_z, which contains integer multiples of the sixth harmonic. The Fourier series expansion of d_z is

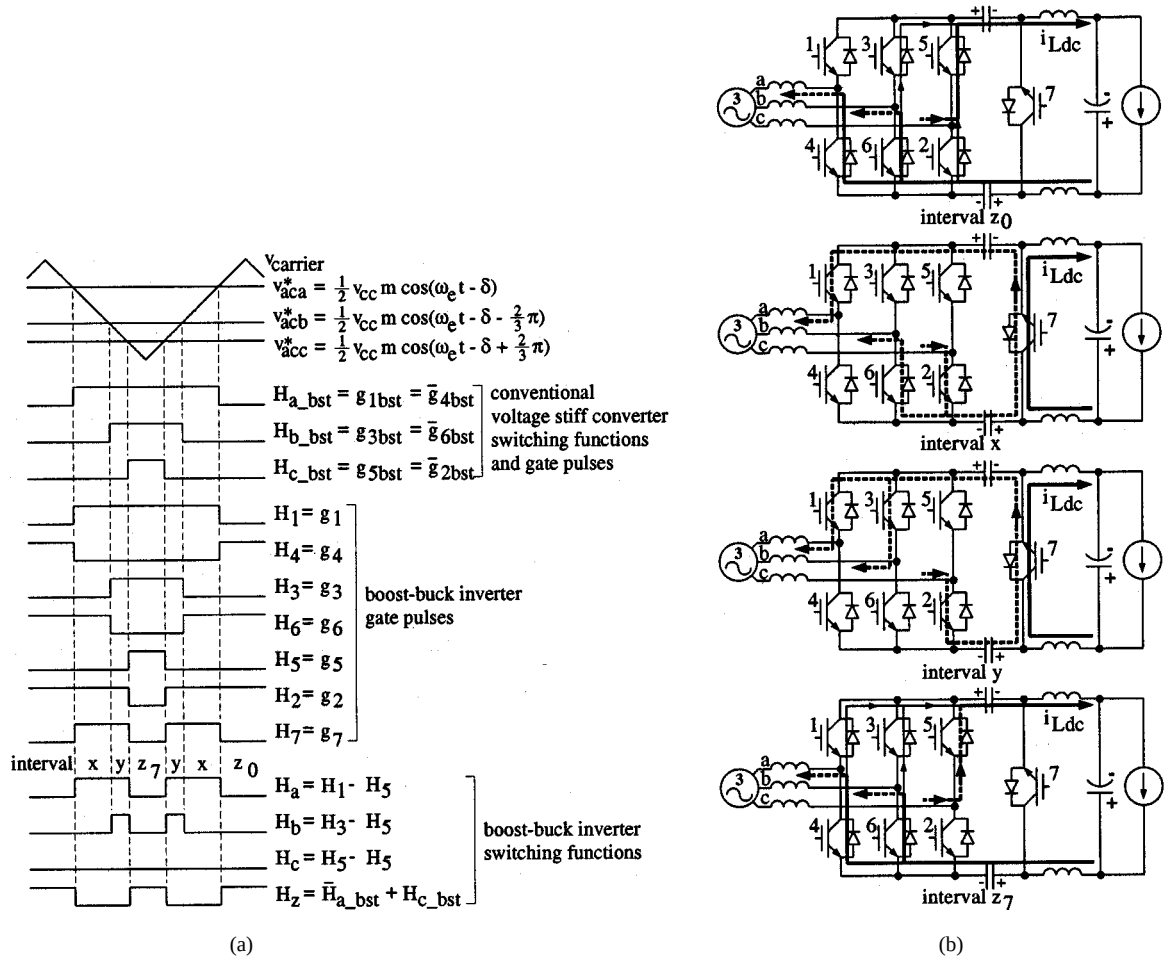
$$d_z = 1 - \frac{3\sqrt{3}}{2\pi}\, m + \frac{3\sqrt{3}}{2\pi}\, m \sum_{n=1}^{\infty} \left(\frac{1}{6n-1} - \frac{1}{6n+1} \right) \cdot \cos(6n\omega_e t - 6n\delta). \tag{7}$$

Because of the time-varying property of d_z, the steady-state operation can not be analyzed by simply solving the algebraic equation of the right-hand side of (1) $= 0$. By using the same



(a) (b)

Fig. 5. PWM scheme and power transfer illustration of Ćuk–Ćuk ac–dc converter for rectification. (a) PWM scheme for rectification. (b) Power transfer illustration.



(a) (b)

Fig. 6. PWM scheme and power transfer illustration of Ćuk–Ćuk ac–dc converter for inversion. (a) PWM scheme for inversion. (b) Power transfer illustration.

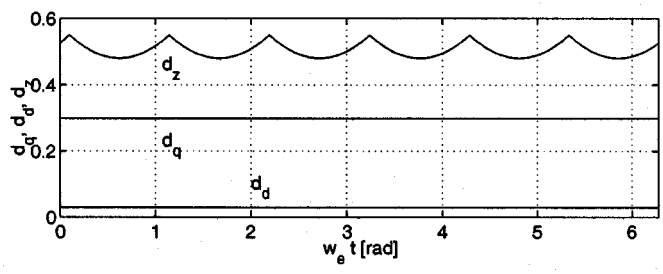


Fig. 7. Duty ratio over one fundamental frequency period ($m = 0.6$, $\delta = 5.6°$).

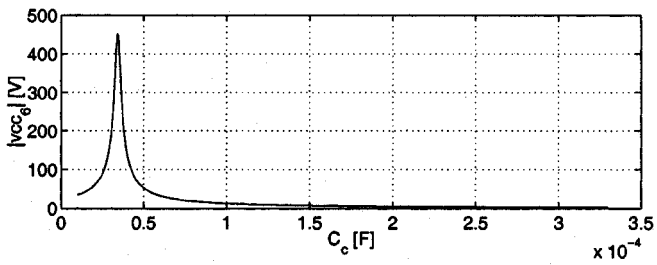


Fig. 8. Steady-state solution example for $|v_{cc6}|$ as a function of C_c [$m = 0.6$, $\delta = 5.6°$, $L_{\rm ac} = 2.5$ mH, $R_{\rm ac} = 0.33\ \Omega$, $L_{\rm dc} = 2.2$ mH, $R_{\rm dc} = 0.24\ \Omega$, $C_{\rm dc} = 2300\ \mu$F, $R_{\rm Load} = 18\ \Omega$, $I_q = 18.9$ A, $I_d = 0.0$ A, $V_{cc} = 610$ V, $I_{L\rm dc} = 16.8$ A, $V_{\rm dc} = 303$ V, and $V_q = 188$ V (230 Vrms line to line)].

approach as in the small-signal analysis, (1) is separated into the dc part and the sextuplen harmonic part as follows:

$$[0 \quad 0 \quad 0 \quad 0 \quad 0]^T = A_o X + BU \tag{8}$$

$$\frac{dx_{6n}}{dt} = A_o x_{6n} + B_o d_{z6n} \tag{9}$$

$$A_o = A|_{d_q = D_q,\, d_d = D_d,\, d_z = D_z}$$

$$B_o = \left[0 \quad 0 \quad -\frac{I_{L\rm dc}}{C_c} \quad \frac{V_{cc}}{L_{\rm dc}} \quad 0\right]^T \tag{10}$$

where the capital letters of the state variables and duty ratio denote their dc component and subscript $6n$ denotes their sextuplen harmonic components. It may be seen that the steady-state circuit behavior in (9) looks like that of a linear time-invariant system excited with sextuplen frequencies. This implies that the reactive component selection must be done such that the resonance with sextuplen frequencies is avoided. This is possible by solving (8) and (9). Once the circuit parameters and the operating point are set up, dc algebraic equation (8) can readily be solved and ac equation (9) can be solved with the phasor computation for each sextuplen frequency as

$$x_{6n} = [j6n\omega_e I - A_o]^{-1} B_o d_{z6n}. \tag{11}$$

Fig. 8 shows a solution example of $|v_{cc6n}|$ for 360 Hz ($n = 1$) as a function of C_c. All the other parameters are presented in the caption. It can be seen from the figure that 30–40 μF of C_c must be avoided. Taking into account higher frequency excitation ($n = 2, 3, \ldots$) and operating point dependent property, it is reasonable to take a larger side of capacitance for C_c with a certain margin.

The time-varying property of the system due to d_z may lead to a more complex treatment for a dynamic model. The well-separated poles between the ac side and the dc side, however,

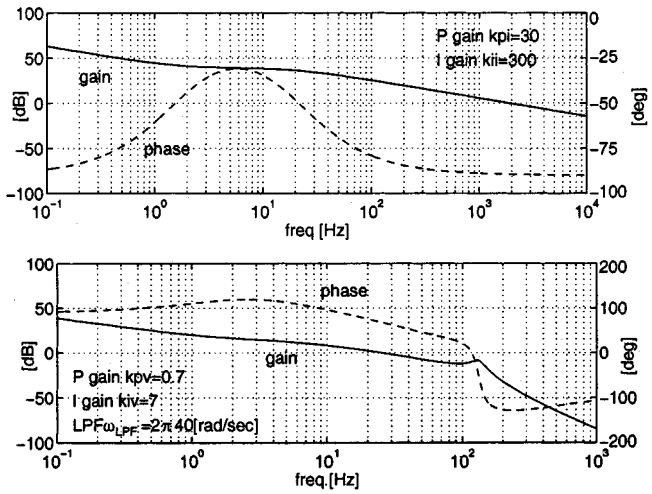


Fig. 9. Representative Bode plots of ac current control (upper trace) and dc voltage control (lower trace) open-loop transfer functions (circuit parameters and operating point are given in Fig. 8 and $C_c = 470\ \mu$F).

make a quasi-static dynamic analysis approximation applicable, namely, the upper two and the lower three differential equations expressed in (1)–(4) can be dealt with separately, provided a proper choice of the reactive components based on the steady-state analysis presented in the above. Therefore, the well-developed ac current control techniques for VSC can directly be applied because the dc-link voltage seen by the three-phase bridge, v_{cc}, can be treated as a constant, V_{cc}. The synchronous frame current controller [22], [23] with d–q decoupling [7] is used here as will be shown later in a control block diagram.

The dc output voltage control bandwidth must be even lower than the sixth harmonic frequency in order to avoid input current waveform degradation in steady state. Noting this requirement, it becomes reasonable to neglect the sextuplen harmonic terms in d_z which express the time dependency, even with a fixed operating point. The usual small-signal analysis is now applicable to the dc-side modeling and the following equations are obtained:

$$\frac{d\Delta x_{\rm dc}}{dt} = A_{\rm dc}\Delta x_{\rm dc} + B_{\rm dc}\Delta u_{dq} \tag{12}$$

$$\Delta x_{\rm dc} = [\Delta v_{cc} \quad \Delta i_{L\rm dc} \quad \Delta v_{\rm dc}]^T$$

$$\Delta u_{dq} = [\Delta i_q \quad \Delta i_d]^T \tag{13}$$

where $A_{\rm dc}$ and $B_{\rm dc}$ are shown in (14) and (15) at the bottom of the next page. The complexity in $A_{\rm dc}$ and $B_{\rm dc}$ comes from the nonlinearity between d_q, d_d, and d_z expressed in (5) and (6), and that in d_q and d_d as functions of i_q and v_{cc} embedded in (1)–(3). Although this dc-side model is not quite physically insightful, it can be utilized to obtain the dc voltage control loop transfer function with a numerical tool such as Matlab.

Fig. 9 shows representative open-loop transfer functions of the ac current and dc voltage control for the control structure shown in Fig. 10 without *Load ff*. They are obtained with (1)–(15) and Matlab. Proportional-integral (PI) controllers are assumed for both the ac current and the dc voltage control and their controller gains are given along with the plots. Since the cross coupling between d and q axes in the ac side is decoupled, the Bode plots of ac current control is a typical one of those

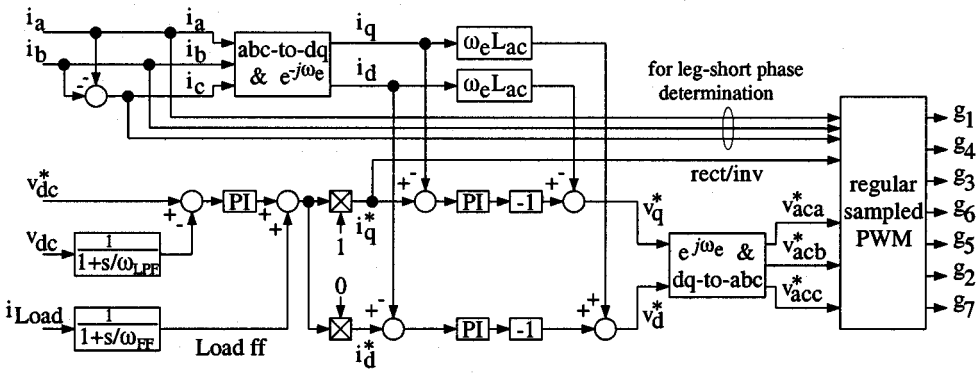


Fig. 10. Control block diagram for circuit simulation.

composed of PI and a first-order physical system. A low-pass filter (LPF) is assumed to be on the dc voltage feedback path, whose cutoff frequency is 40 Hz. The voltage control bandwidth is about 20 Hz. This low bandwidth is necessary to avoid unwanted ac current amplitude modulation in steady state.

V. Circuit Simulations

A series of circuit simulations has been carried out with the Saber simulation package. The power stage component parameters and controller gains are the same as those in Figs. 8 and 9. A rated operation of 5-kW output power and 300 V of dc output voltage with 230 V of ac line-to-line voltage in rms are assumed.

Fig. 10 shows a control block diagram for the simulation. Two phase currents and dc voltage are sensed for the feedback control purposes. In addition, in order to improve dynamic response in the dc voltage control, load current i_{Load} is also sensed and added to the ac current amplitude reference as load feedforward. The corner frequency of the LPF on the load feedforward path is 180 Hz. Changeover of rectifier/inverter operation is determined by the sign of i_q^*. In order to choose proper two-leg-short phases for zero-voltage space vectors in its rectifier operation, three-phase current information is provided to the regular-sampled PWM block. The triangle carrier frequency for the regular-sampled PWM is 9 kHz.

Strictly speaking, the triangle carrier amplitude should be adjusted depending on the coupling capacitor voltage v_{cc}, which is the dc-bus voltage seen by the three-phase VSC bridge. This would, however, introduce extra complexity into the control block, therefore, a fixed triangle carrier amplitude for the rated operating point, i.e., 610 V, is used here.

Figs. 11 and 12 show steady-state simulation results of four different operating conditions, namely, step-up and step-down for each rectification and inversion. It can be seen from these figures that almost unity-power-factor and nearly sinusoidal ac current operation is possible. It may be noted that the ac current waveform quality under the lightly loaded condition of Fig. 12 is degraded. This is because switching frequency ripple component and the low-order nontriplen harmonic components are increased with respect to the fundamental component. The latter is caused by the sextuplen excitation described in the previous section.

$$A_{\mathrm{dc}}=\begin{bmatrix} \frac{R_{\mathrm{ac}}I_q-V_q}{V_{cc}^2}\left(\frac{3\sqrt{3}}{\pi}\frac{D_q}{\sqrt{D_q^2+D_d^2}}\frac{I_{L\mathrm{dc}}}{C_c}+\frac{3}{2}\frac{I_q}{C_c}\right)-\frac{\omega_e L_{\mathrm{ac}}I_q}{V_{cc}^2}\left(\frac{3\sqrt{3}}{\pi}\frac{D_d}{\sqrt{D_q^2+D_d^2}}\frac{I_{L\mathrm{dc}}}{C_c}+\frac{3}{2}\frac{I_d}{C_c}\right)-\frac{1}{C_c}D_z & 0 \\ \frac{1}{L_{\mathrm{dc}}}D_z-\frac{3\sqrt{3}}{\pi}\frac{D_q}{\sqrt{D_q^2+D_d^2}}\frac{R_{\mathrm{ac}}I_q-V_q}{V_{cc}L_{\mathrm{dc}}}+\frac{3\sqrt{3}}{\pi}\frac{D_d}{\sqrt{D_q^2+D_d^2}}\frac{\omega_e L_{\mathrm{ac}}I_q}{V_{cc}L_{\mathrm{dc}}} & -\frac{R_{\mathrm{dc}}}{L_{\mathrm{dc}}} \quad -\frac{1}{L_{\mathrm{dc}}} \\ 0 & \frac{1}{C_{\mathrm{dc}}} \quad -\frac{1}{C_{\mathrm{dc}}R_{\mathrm{Load}}} \end{bmatrix} \tag{14}$$

$$B_{\mathrm{dc}}=\begin{bmatrix} \frac{3}{2}\frac{1}{C_c}D_q-\frac{R_{\mathrm{ac}}}{V_{cc}}\left(\frac{3\sqrt{3}}{\pi}\frac{D_q}{\sqrt{D_q^2+D_d^2}}\frac{I_{L\mathrm{dc}}}{C_c}+\frac{3}{2}\frac{I_q}{C_c}\right)+\frac{\omega_e L_{\mathrm{ac}}}{V_{cc}}\left(\frac{3\sqrt{3}}{\pi}\frac{D_d}{\sqrt{D_q^2+D_d^2}}\frac{I_{L\mathrm{dc}}}{C_c}+\frac{3}{2}\frac{I_d}{C_c}\right) & \frac{2}{2}\frac{1}{C_c}D_d \\ \frac{3\sqrt{3}}{\pi}\frac{D_q}{\sqrt{D_q^2+D_d^2}}\frac{R_{\mathrm{ac}}}{L_{\mathrm{dc}}}-\frac{3\sqrt{3}}{\pi}\frac{D_d}{\sqrt{D_q^2+D_d^2}}\frac{\omega_e L_{\mathrm{ac}}}{L_{\mathrm{dc}}} & 0 \\ 0 & 0 \end{bmatrix} \tag{15}$$

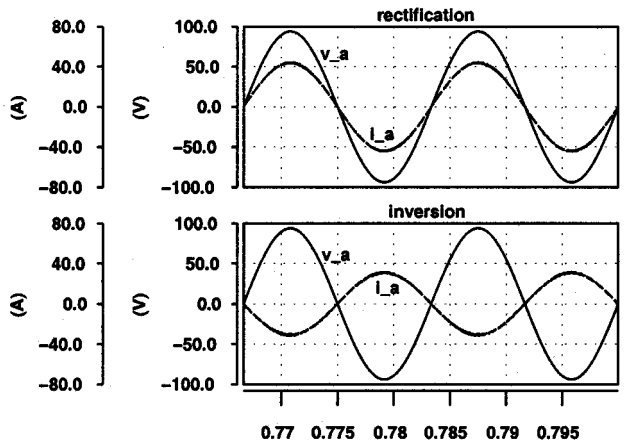


Fig. 11. Simulation results for step-up rectification (upper trace) and step-down inversion (lower trace) with ac 115 V line to line in rms, dc 300 V, and $i_{\mathrm{Load}} = 16.7$ A, phase-a voltage and current.

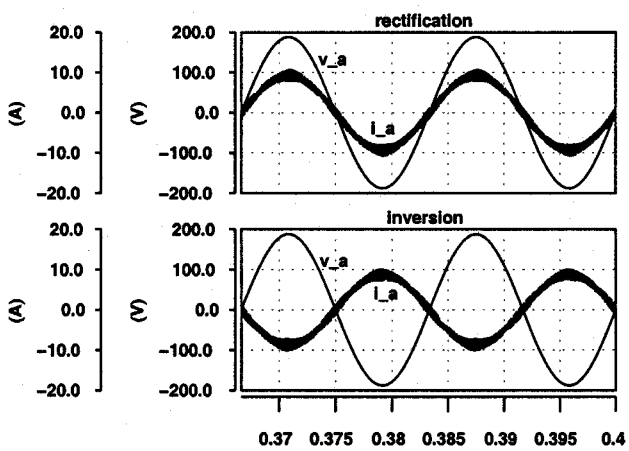


Fig. 12. Simulation results for step-down rectification (upper trace) and step-up inversion (lower trace) with ac 230 V line to line in rms, dc 150 V, and $i_{\mathrm{Load}} = 8.4$ A, phase-a voltage and current.

As a dynamic response example, Fig. 13 shows simulation results of a sudden load change requiring changing over from full-rated rectification to full-rated inversion. The load current direction is reversed at about 0.3 s. By utilizing load feedfoward, the low bandwidth of the voltage control loop is well compensated and the dc-link voltage is hardly disturbed. Along with the waveforms are shown the gate pulses for switches of the phase-a leg and the dc link. It can be seen in the figure that the active switch on the dc link operates only for inverter operation.

VI. Hardware Experiments

A hardware prototype of the Ćuk–Ćuk converter has been built with the same component values as shown in Figs. 8 and 9. The PI compensator gains are also the same as those in the analysis and simulations except that the current controller P gain has been decreased to a quarter of the original values obtained from the analysis to reduce noise susceptibility in the fine-tuning process.

Figs. 14 and 15 show steady-state ac current waveform i_b in four different operating conditions, namely, step-up and

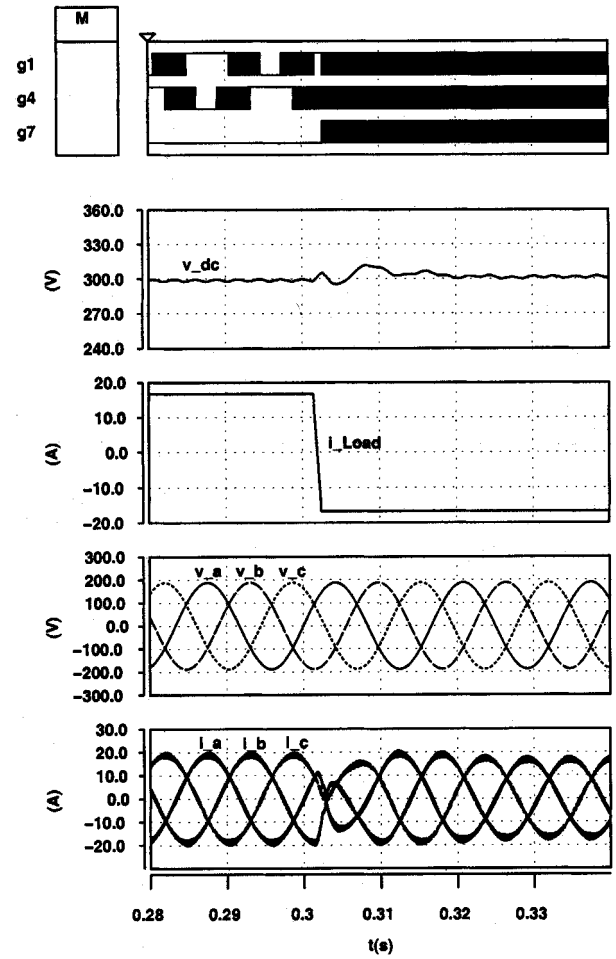


Fig. 13. Simulation results for sudden change from full rectification to full inversion.

step-down for each rectification and inversion. Since the neutral point is not accessible, line-to-line voltage v_{ac} is overlaid. The maximum point of v_{ac} corresponds to 0° of v_b and it is the center of time axis. It can then be seen from the figures that almost unity-power-factor operation has been realized in all four cases. As predicted from the preceding sections, the ac current waveform is relatively degraded in lightly loaded operations, i.e., the lower traces in Figs. 14 and 15.

Fig. 16 shows dynamic response in a sudden change from rectification to inversion. Although the operating point is not the same as that in Fig. 13, a similar dynamic response is observed. In particular, dc output voltage v_{cdc} is barely disturbed in spite of the low bandwidth of the dc voltage control loop thanks to the load feedforward.

VII. Conclusions

Three-phase PWM boost–buck rectifiers with power-regenerating capability have been investigated in this paper. The converters of interest are capable of: 1) both voltage step-up and step-down; 2) bidirectional power processing; and 3) almost unity-power-factor operation with nearly sinusoidal ac current.

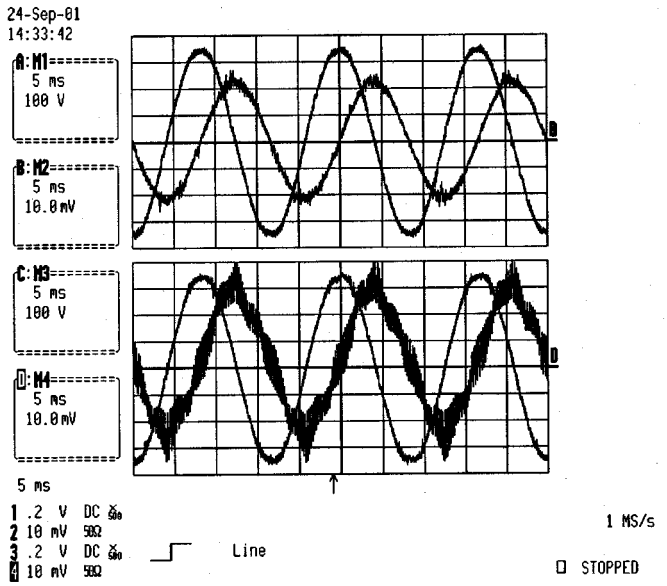


Fig. 14. Hardware experimental results of steady-state rectifier operation (upper trace: step-up rectification, *A:* line-to-line voltage $v_{\rm ac}$ 100 V/div; *B:* phase-b current i_b 20 A/div with $v_{\rm cdc} = 300$ V, ac source voltage 115 V line to line in rms and approximately 5 kW of output power, lower trace: step-down rectification; *:C* line-to-line voltage $v_{\rm ac}$ (phase angle reference purpose only); *D*: phase-b current i_b 2 A/div with $v_{\rm cdc} = 150$ V, ac source voltage 230 V line to line in rms and approximately 1.4 kW of output power).

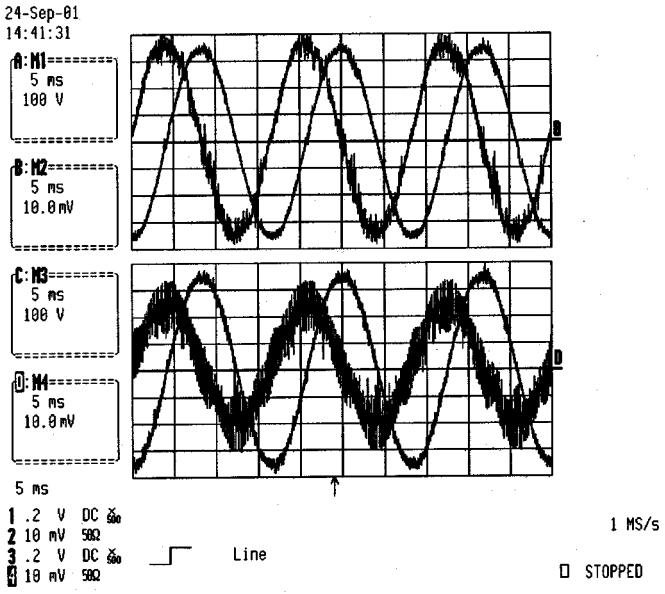


Fig. 15. Hardware experimental results of steady-state inverter operation (upper trace: step-down inversion, *A:* line-to-line voltage $v_{\rm ac}$ 100 V/div; *B:* phase-b current i_b 10 A/div with $v_{\rm cdc} = 300$ V, ac source voltage 115 V line to line in rms and approximately 5 kW of power regeneration; lower trace: step-up inversion *C:* line-to-line voltage $v_{\rm ac}$ (phase angle reference purpose only); *D:* phase-b current i_b 2 A/div] with $v_{\rm cdc} = 150$ V, ac source voltage 230 V line to line in rms and approximately 1.4 kW of power regeneration).

A systematic power stage topology derivation has been presented. Taking the Ćuk–Ćuk realization as an example, operating principle, modulation scheme, steady-state, and dynamic analyses have been discussed. In particular, differences between the boost–buck rectifier under focus and the well-known VSC have been made clear from an analytical viewpoint. Representative results of circuit simulations and hardware experiments have been presented. The feasibility of the presented three-phase PWM boost–buck rectifier with power-regenerating capability has been demonstrated through these procedures.

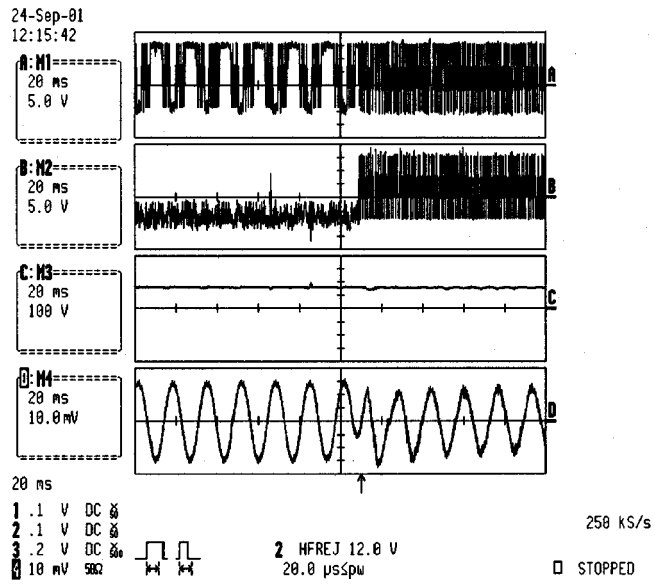


Fig. 16. Hardware experimental results of sudden change over from rectification to power regeneration (trace *A:* gate pulse for S_6 5 [V/div]; trace *B:* gate pulse for S_7 5 V/div; trace *C:* dc output voltage $v_{\rm cdc}$ 100 V/div; trace *D:* phase-b current i_b 5 A/div with ac source voltage 117 V line to line in rms and change from approximately 1.8 kW of rectification to 1.8 kW of regeneration).

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