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Three-Port Series-Resonant Converter DC Transformer with Integrated Magnetics for High Efficiency Operation

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Abstract—The series-resonant converter has become a very attractive topology for solid-state transformers due to its fixed voltage gain and soft-switching conditions when operating at the resonance frequency. This paper presents an open-loop three-port series-resonant converter (TP-SRC) capable of interconnecting three dc microgrids. High efficiency power electronics is a key enabler for the future dc distribution systems. In this paper, efficiency optimization and rms current reduction of the TP-SRC is achieved by a detailed analysis of the resonance frequency and dead-time selection. The analysis is supported by a losses modelling of the main components of the converter. In addition, Gallium Nitride (GaN) MOSFETs are used to reduce semiconductors' losses. Furthermore, the resonance inductance of the distributed resonant tank has been integrated into the leakage inductance of the transformer and the PCB parasitic inductances. In order to ensure a fixed resonance frequency, an experimental resonance frequency matching methodology for the resonant tank has been presented. Experimental results were obtained for a $1.4\,\mathrm{kW}$ featuring a peak efficiency of $98.8\,\%$.

I. Introduction

State-of-the-art in electrical power conversion shows a tendency towards the utilization of Solid-State transformers (SST) as interlinking converters between dc grids [1]. Technological advances in SST that enhance the system scalability and dc grids flexibility in combination with improvements in energy conversion efficiency, are key enablers to motivate the penetration of SST into dc distribution systems. Among the different power converter topologies implemented as SST , the Series-Resonant converter (SRC) has been extensively used [2–5] because of its load regulation characteristics in open-loop together with its soft-switching conditions for wide power ranges. Many optimization methods focusing on the efficiency improvement of the SRC have been discussed in the literature. Authors in [6] proposed a computer aided algorithm with the calculated efficiency as the objective function. The loss model was carried out for a LLC SRC with phase-shifted modulation and results were verified on a $300\,\mathrm{W}$ $400\,\mathrm{V}$ prototype with a peak efficiency of $97.07\,\%$. In [7] an efficiency analysis for a two port open-loop SRC was presented. The efficiency was optimized by utilizaing silicon-carbide MOSFETs and a detailed design procedure based on an accurate losses modelling, where the losses were analysed for a fixed resonance frequency of $20\,\mathrm{kHz}$. The losses model was verified on a $10\,\mathrm{kW}$ SRC with a peak efficiency of
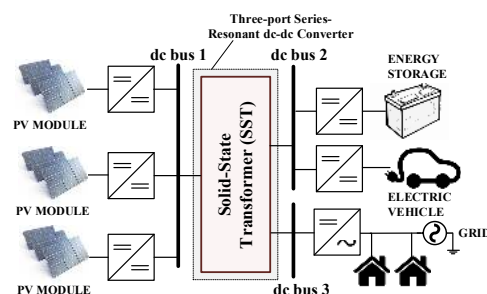

Fig. 1. Example of application for the Three-Port Series-Resonant Converter operating as a Solid-State Transformer to interconnect multiple dc grids.

$98.61\,\%$. In [8] losses optimization were performed for a current-fed SRC based on $15\,\mathrm{kV}$ SiC MOSFETs. A fixed dead-time strategy was adopted, incurring in partial soft-switching conditions, so the converter design parameter was carried out based on a trade-off between conduction losses and switching losses. Reported efficiency on a $12\,\mathrm{kW}$ prototype was $97.8\,\%$.

In this paper, an efficiency optimization for a Three-Port Series-Resonant converter (TP-SRC) with a distributed resonant tank is presented. The TP-SRC aims at interconnecting three dc-bus, which are utilized to integrate RES, LES and the ac grid. The system architecture diagram is presented in Fig.1. The TP-SRC operates in open-loop at the sub-resonance region, at a fixed switching frequency and duty cycle. The design methodology of the TP-SRC is based on the design equations proposed in [4], [5], where the resonant tank parameters are selected to ensure soft-switching under all operation conditions. On the other hand, the SRC generally incurs into high root-square-mean (rms) currents due to the sinusoidal shape of the resonant current together with the magnetizing current flowing through the inputs ports. Therefore, while the switching losses are almost negligible, the SRC suffers from higher conduction losses. The design procedure given in [4], [5] have two degrees of freedom which are the switching frequency and dead-time. The effect of these two parameters into the converter rms currents and losses is analyzed in this paper. To further improve the efficiency, Gallium-Nitride (GaN) MOSFETs with very low on-state resistance are used, decreasing dramatically the conduction losses. Furthermore,
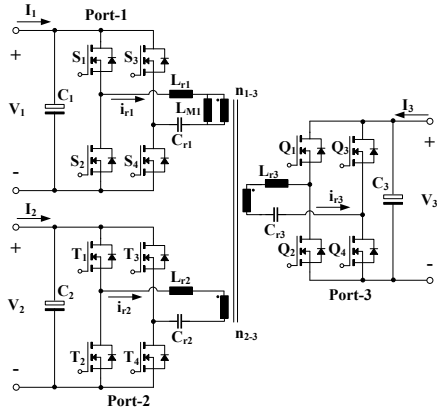
Fig. 2. Topology of the Three-Port Series Resonant Converter.

the leakage inductance of the resonant tank is solely implemented by the leakage inductance of the transformer and the PCB parasitics. In that way, external resonant inductors are avoided and the converter losses are further minimized. Since the resonant inductance is solely composed by the leakage inductance of the transformer and the parasitic inductances, the resonance frequency matching of the distributed resonant tank becomes challenging. An experimental methodology for tuning the resonant tanks at each side of the transformer at the same resonance frequency id also presented in this study.

This paper is organized as follows: section II describes the operation principle of the TP-SRC, where the main design equations are provided. In section III the extended rms equations of the resonant currents are given and the losses analysis methodology in all components is presented. In section IV, the influence of the dead-time and switching frequency to the rms currents and the efficiency is analyzed. In section V, the resonance frequency matching methodology is explained. Section VI presents the implementation procedure and the experimental results on a $1.4\,\mathrm{kW}$ prototype, where a peak efficiency of $98.8\,\%$ is demonstrated.

II. THREE-PORT SERIES-RESONANT CONVERTER

The circuit diagram of the bidirectional TP-SRC is shown in Fig.2 and Fig.3 illustrates the main waveforms of the converter. The SRC achieves the highest efficiency when the switching frequency is equal or slightly below the resonance frequency [7], which is given by the resonant inductors L_r and resonant capacitors C_r. At this operation region the MOSFETs at the input bridges operate with zero-voltage switching (ZVS) at the turn-on, while the turn-off is carried out at low current and the MOSFETs at the output bridges operate with zero-current switching (ZCS). An additional advantage is that the SRC has a fixed input-to-output voltage gain when is operating at the vicinity of the resonance frequency. Due to the fixed voltage gain and soft-switching conditions, open-loop operation of the TP-SRC results in a very attractive solution for applications where only load regulation is required and the dc bus voltages are constant.
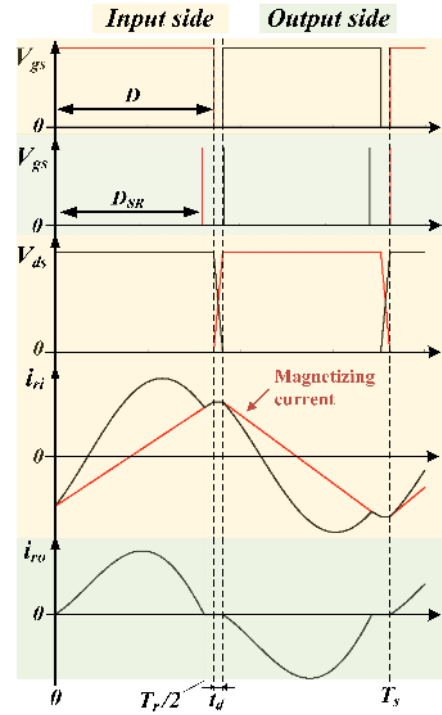

Fig. 3. Main waveforms of the Three-Port Series Resonant Converter.

The TP-SRC operates at a fixed switching frequency f_{sw} and MOSFETs at input ports are actively switched with a $50\,\%$ duty cycle with a dead-time. Synchronous rectification is used in the output ports to reduce conduction losses. In order to prevent hindering soft-switching, synchronous rectification is implemented at the switching frequency and with an on-time equal to half the resonant period.

The design of the resonant tank is based on the methodology proposed in [5], where the main requirements are (I) to provide the minimum energy to charge/discharge the MOSFTETs' output capacitance C_{oss} and (II) to operate with an inductive impedance of the resonant tank under any load condition. The first conditions is fullfiled by selecting a magnetizing inductance L_{M1} that provides enough peak current during the dead-time to charge and discharge the MOSFETs' C_{oss}. According to [5], to ensure ZVS the magnetizing inductance L_{M1} should be lower than the maximum magnetizing inductance $L_{M1,max}$ given by (1). Then, the magnetizing inductance is chosen according to (2) to ensure that ZVS will be achieve in all ports. As explained by the authors in [5], the minimum inductance ratio to ensure operation with an inductive impedance, and thereby achieve ZVS under all operating conditions, can be calculated with (3), and therefore the condition in (4) has to be fulfilled. Finally, the resonant capacitors are chosen with (5).

Utilizing the design equations (1)-(5) and the design specifications from Table I, the resonant tank parameters can be calculated. As can be observed, the design procedure contains two main degrees of freedom, which are the resonance fre-

quency and the dead-time. These parameters will be selected in order to achieve the highest efficiency.

$$L_{M1,max,S} = \frac{t_d}{8C_{oss,S}f_{sw}}$$

$$L_{M1,max,T} = n_{1-2}^2 \frac{t_d}{8C_{oss,T}f_{sw}} \quad (1)$$

$$L_{M1,max,Q} = n_{1-3}^2 \frac{t_d}{8C_{oss,Q}f_{sw}}$$

$$L_{M1} = min\{L_{M1,S}, L_{M1,T}, L_{M1,Q}\} \quad (2)$$

$$k_{min} = \frac{3}{2} \left(\frac{\pi^2 \omega_r L_{M1} P_{max}}{8V_1^2} \right)^2 \quad (3)$$

$$k_{min} \leqslant \frac{L_{M1}}{L_{r1}} \quad k_{min} \leqslant \frac{L_{M1}}{n_{1-2}^2 L_{r2}} \quad k_{min} \leqslant \frac{L_{M1}}{n_{1-3}^2 L_{r3}} \quad (4)$$

$$C_{r1} = \frac{1}{\omega_r^2 L_{r1}} \quad C_{r2} = \frac{1}{\omega_r^2 L_{r2}} C_{r3} = \frac{1}{\omega_r^2 L_{r3}} \quad (5)$$

where

$C_{oss,S}$: Output capacitances of MOSFETs S_1-S_1.
$C_{oss,T}$: Output capacitances of MOSFETs T_1-T_4.
$C_{oss,Q}$: Output capacitances of MOSFETs Q_1-Q_4.
f_{sw}: Switching frequency.
f_r: Resonance frequency.
ω_r: angular resonance frequency given by $\omega_r = 2\pi f_r$.
n_{1-2}: Turns ratio from Port-1 to Port-2 given by n_{1-3}/n_{2-3}.
k_{min}: Minimum inductance ratio.
P_{max}: Maximum rated power.

III. LOSSES ANALYSIS METHODOLOGY

In order to analyse the effect of the switching frequency and dead-time to the converter efficiency, a careful analysis of the losses in the main components of the TP-SRC is computed for the given specifications. To support the losses analysis the equations to calculate the rms currents flowing through the resonant tanks are given by (6) and (7) and the magnetizing current at the beginning of the dead-time is given by (8).

$$I_{ri,rms} = n_{i-o}^2 V_o \frac{\sqrt{2}}{8} \sqrt{\frac{(T_{sw} - 2t_d)^2(T_{sw} + 2t_d)}{T_{sw}L_{Mi}^2}}$$
$$+ \sqrt{\frac{T_{sw}4\pi^2 P_i^2}{(T_{sw} - 2t_d)n_{i-o}^4 V_o^4}} \quad (6)$$

$$I_{ro,rms} = \frac{\sqrt{2}}{4}V_o \sqrt{\frac{n_{i-o}^4}{L_{Mi}^2} \frac{(T_{sw} - 2t_d)^3}{T_{sw}} \frac{5\pi^2 - 48}{12\pi^2}}$$
$$+ \sqrt{\pi^2 \frac{T_{sw}}{T_{sw} - 2t_d} \frac{P_o^2}{V_o^4}} \quad (7)$$

$$I_M = \frac{1}{4} \frac{V_1(T_s - 2t_d)}{L_{M1}} \quad (8)$$

where i refers to the input port, o to the output port, t_d to the dead-time, T_{sw} to the switching period $1/f_{sw}$ and L_{Mi} to the magnetizing inductance referred to the input port.

A. Semiconductors losses

In order to achieve highest efficiency performance of the semiconductors, GaN MOSFETs are selected. GaN transistors are characterized by low on resistance $R_{ds,on}$ and low output capacitance C_{oss}. The combination of low energy losses with ZVS results in very low switching losses. In reverse conduction, GaN MOSFETs have larger voltage drop across the body diode than Silicon MOSFETs. But when using synchronous rectification, the current flows through the MOSFET channel, and therefore the losses in reverse conduction are given by the $R_{ds,on}$. The MOSFETs selected are given in Table II.

The main losses of a MOSFET are divided in conduction losses and switching losses. The conduction losses for the input side MOSFETs $P_{cond,in}$ can be calculated with (9), where $I_{ri,rms}$ is calculated with (6). As the converter operates under ZVS on the input side, turn-on losses can be neglected. However, at the turn-off event, the current flowing through the MOSFETs channel hardly commutates to the body diodes of the complementary switches incurring in turn-off losses $P_{off,in}$. The turn-off losses when switching at the vicinity of the resonance frequency can be calculated with (10) [9], where I_M is the magnetizing current at the turn-off event.

Synchronous rectification is used at the output side MOSFETs. Because of the fixed switching frequency and fixed duty cycle operation, the output MOSFETs turn-on and turn-off events can be adjusted to avoid current circulation through the body diode by fixing the on-time below half the resonance period. Therefore, the conduction losses of a MOSFET at the output side $P_{cond,out}$ can be calculated with (11). As the converter operates in the vicinity of the resonance frequency ZCS on the output side is always achieved, and thus, the switching losses can be neglected.

$$P_{cond,in} = \frac{R_{ds,on}I_{ri,rms}^2}{2} \quad (9)$$

$$P_{off,in} = \frac{1}{6}\left(V_{ds}I_M - C_{oss}\frac{V_{ds}}{t_{off}}\right)t_{off}f_s \tag{10}$$

$$P_{cond,out} = \frac{R_{ds,on}I_{ro,rms}^2}{2} \tag{11}$$

B. Transformer losses

The transformer design has been carried out to optimize its losses through the design methodology explained below. The design procedure have two degrees of freedom, which are the core size and the flux density. The cores considered for the design are (I) ETD 49/25/16, (II) ETD 54/28/19 and (III) ETD 59/31/22. The transformer has been designed through a loop where the peak flux density β_{max} has been swept from $50\,\mathrm{mT}$ to $300\,\mathrm{mT}$. To reduce the complexity of the comparative analysis single wire gauge has been considered and an interleaved arrangement of the transformer windings is assumed. The wire gauge is selected at the skin depth δ as given by (12) to reduce the skin effect, and the number of strands is calculated to meet the power requirements. Then, the number of turns is calculated for the flux density selected. Based on the design specifications, the maximum flux linkage occurs at Port-3, where $V_3 = 600\,\mathrm{V}$ and thus, the number of turns is calculated according to (13). To adjust the inductance of the transformer to the desired magnetizing inductance, given by (2), the air-gap length is calculated with (14). Subsequently the implementation viability is verified by comparing the window area of the core with the required area by the design. If the design is successful the winding and core losses are calculated, otherwise the peak flux density is increased and the transformer is redesigned. When the peak density reaches the maximum, a larger core size is chosen.

$$\delta = \frac{7.5}{\sqrt{f_{sw}}}(cm) \tag{12}$$

$$N_3 = \frac{V_3}{4f_{sw}A_c\beta_{max}} \tag{13}$$

$$l_g = \frac{\eta_0 N_3^2 A_c}{n_{1-3}^2 L_{M1}} \tag{14}$$

where

N_3: Number of turns of the transformer at Port-3.
A_c: Cross-sectional area of the transformer core.
η_0: Permeability of free space $\eta_0 = 4\pi \cdot 10^{-7}Hm^{-1}$.

The dc winding resistance is calculated with (15) and Dowell's equations [10] are used to estimate the ac resistance (16). The copper loss of the transformer can be calculated with (17), where the rms currents at the transformer windings are calculated with (6) or (7) whether the port behaves as an input or an output. Finally, the core losses are estimated using Steinmetz equation (18).

$$R_{dc} = \frac{\rho_{cu}N_{tr}MLT}{A_{AWG}} \tag{15}$$

$$\frac{R_{ac}}{R_{dc}} = \frac{\Delta}{2}\left[\frac{\sinh\Delta + \sin\Delta}{\cosh\Delta - \cos\Delta} + (2m-1)^2\frac{\sinh\Delta - \sin\Delta}{\cosh\Delta + \cos\Delta}\right] \tag{16}$$

$$P_{TR,W} = R_{ac1}I_{r1,rms}^2 + R_{ac2}I_{r2,rms}^2 + R_{ac3}I_{r3,rms}^2 \tag{17}$$

$$P_{TR,C} = Kf_{sw}^\alpha \beta_c^\beta \tag{18}$$

Δ: h/δ.
h: Conductor height
m: Number of layers. $m = 1$ for interleaved multilayer windings.
ρ_{cu}: Resistivity of the copper. $\rho_{cu} = 1.72 \times 10^{-8}\Omega m$ @ $20\,°C$.
MLT: Core mean-length-turn.
A_{AWG}: Wire cross-sectional area.
K, α, β: Core material parameters provided by the manufacturer. For N87 material $K = 3.73 \cdot 10^{-7}$, $\alpha = 2.1$ and $\beta = 2.48$.

The total transformer losses are calculated with (19) and to ensure transformer operation under a safe temperature range, the condition in (20) should be satisfied.

$$P_{TR} = P_{TR,W} + P_{TR,C} \tag{19}$$

$$P_{TR} \leqslant \frac{T_{max} - T_{amb}}{Tr_c} \tag{20}$$

where T_{max} is the maximum safe-operating temperature of the transformer core, T_{amb} is the ambient temperature and Tr_c the core thermal resistance given by the manufacturer.

C. Resonant capacitor

The losses at the capacitor are due to the equivalent series resistance (ESR) which is given by the resonance frequency, the capacitance and the dissipation factor $\tan\delta$ as shown in (21). To optimize the losses at the resonance capacitor, Polyphenylene sulfide (PPS) and Polypropylene (PP) film capacitors have been utilized due to their low dissipation factor. In addition, the temperature and frequency dependence of the electrical parameters in PP and PPS film capacitors are also low compared to their counterparts. To have a more accurate estimation of the losses at the resonant capacitor, a database containing a linearised function of $\tan\delta$ in terms of frequency for different capacitors have been included in the calculation. Once the ESR has been estimated, the losses at the resonant capacitors are calculated with (22), where the rms currents are calculated with (6) or (7) whether the port behaves as input or output.

$$ESR = \frac{\tan\delta}{2\pi f_r C_r} \tag{21}$$

$$P_{C_r} = ESR_1 I_{r1,rms}^2 + ESR_2 I_{r2,rms}^2 + ESR_3 I_{r3,rms}^2 \tag{22}$$

IV. RMS CURRENTS AND EFFICIENCY ANALYSIS

A. Switching frequency analysis

By following the design procedure given in Section II, with equations (1)-(4) soft-switching conditions are always achieved and thus, MOSFETs' turn-on losses are almost negligible. This indicates that potentially higher switching frequency is achievable. The rms currents in terms of switching frequency have been calculated for different dead-times using (1)-(8). Results are depicted in Fig.4. The rms currents are given in per-unit, where the base unit is the dc current at the input or output port. The base relationships at the input port are not the same for different power levels due to the magnetizing current, which is not load-dependent. Conversely, at the output side the per-unit rms current do not differ for different power levels. It can be observed that for a fixed t_d, increasing the switching frequency can lead to an increase of the rms current, and thus, the MOSFETs' conduction losses can increase accordingly.

On the other hand, increasing the switching frequency allows the use of smaller passive components, including the resonant tank parameters. The maximum resonant inductance allowed to operate the TP-SRC with an inductive impedance and the corresponding resonance capacitance have been calculated using (1)-(5) for different t_d and f_{sw}. Results are given in Fig.5. As expected, by increasing the switching frequency the maximum resonant inductance L_r decreases. This can increase the design complexity of the converter, since the maximum L_r allowed by the design might drop down below the total series inductance, which is mainly composed by the leakage inductance of the transformer together with the parasitic inductances of the PCB. Consequently, the resonant converter would fall into the capacitive operating region and soft-switching would be hindered [4], [5].

B. Dead-time analysis

For a given switching frequency the rms currents have been calculated with different combinations of t_d and L_M at different power levels using (1)- (8). Results obtained are given in Fig. 9. Small t_d implies smaller L_M which results in larger circulating current hence larger conduction losses. At the same time, large t_d causes a reduction of the effective duty cycle, and thus larger rms currents are required to transfer the same power from input side to output side.

For different power levels the optimal combination of t_d and L_M1 that gives the lowest rms currents differs, and therefore the optimal design for the entire power range can not be accomplished. For a design where the rms current should be minimized for all load conditions, a normal distribution of the optimal t_d for each power level can be utilized as illustrated in Fig.7.

C. Efficiency analysis

First, the overall efficiency of the TP-SRC has been calculated in terms of switching frequency and resonant components size. The efficiency calculation has been carried out following the losses analysis depicted in Section II. At this stage, the
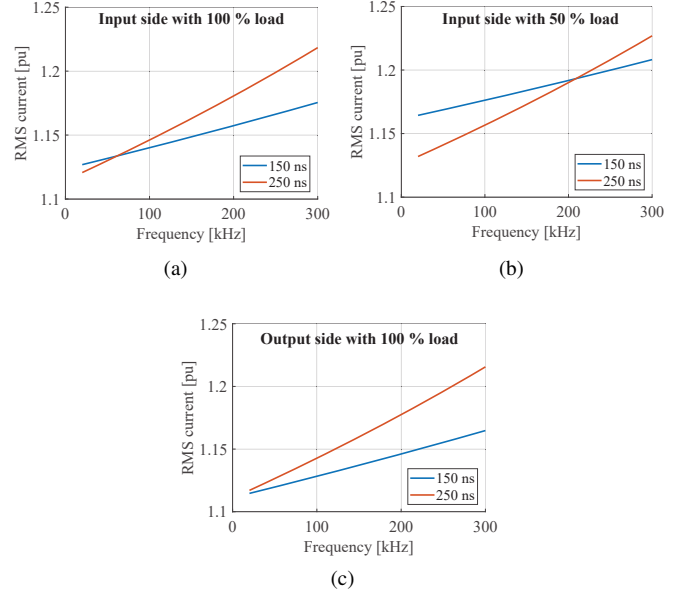
(a)

(b)

(c)

Fig. 4. Resonant rms current in per-unit at input and output side in terms of frequency with fixed dead-time and different power transfer. The rms current is converted to the per-unit system with the dc current at the input or output port I as the base value and is calculated with $Ir, rms(pu) = Ir, rms/I$. The per-unit rms current at the input side is load-dependent due to the magnetizing current, which is not load-dependent.
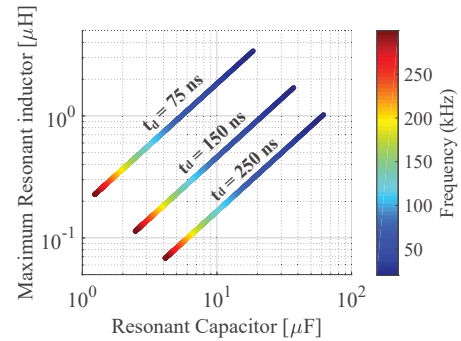
Fig. 5. Resonant tank components at the LV side $L_{r,HV}$ and $C_{r,HV}$ for different switching frequencies f_{sw} and dead-times t_d. For each switching frequency and dead-time the result gives the maximum resonant inductance allowed according to (3).

resonant inductance is an unknown parameter, since it is composed by the leakage inductance of the transformer and the parasitic inductances of the PCB. For that reason, the resonant inductor parameter has been swept from a minimum to maximum value of $L_{r,HV} = 100\,\text{nH}..30\,\mu\text{H}$ in the computational algorithm. The efficiency has been calculated for the lowest conduction losses by selecting the dead-time that results in the lowest rms current for each switching frequency. Results obtained are given in Fig.10. Taking into account the results obtained for $50\,\%$ load and rated load, a potential switching frequency between $100\,\text{kHz}$ to $150\,\text{kHz}$ would give the highest efficiency with the smallest resonant capacitor.

As previously discussed, the optimal combination of t_d

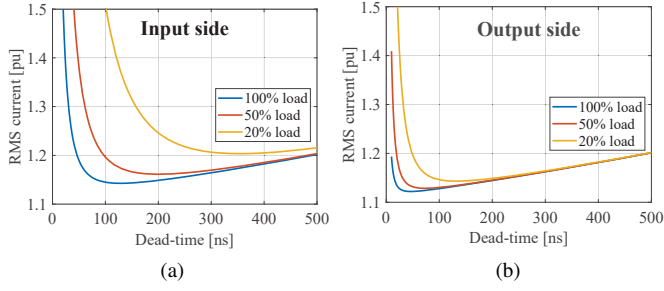Fig. 6. Resonant rms current in per-unit at input and output side in terms of dead-time with a $f_{sw} = 150\,\text{kHz}$ and different power transfer. The rms current is converted to the per-unit system with the dc current at the input or output port I as the base value and is calculated with $Ir, rms(pu) = Ir, rms/I$. The per-unit rms current at the input side is load-dependent due to the magnetizing current, which is not load-dependent.
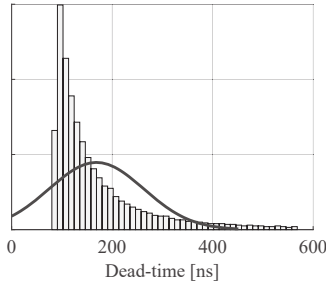

Fig. 7. Normal distribution of the optimal dead-time for each power level.

and L_M that incurs in the smallest rms current changes for different power levels. For that reason, the effect of t_d to the overall efficiency is also analysed. Fig.9 shows the theoretical efficiency in terms of t_d and input power for a given switching frequency.

V. RESONANCE FREQUENCY MATCHING

The TP-SRC presented in this paper utilizes the leakage inductance of the transformer and the PCB parasitic inductances as the inductive component of the resonant tank. Consequently, the total resonant inductance seen from each port is unpredictable, which complicates the resonance frequency matching. The TP-SRC can still operate at a fixed switching frequency, even if the resonant frequency at each port is not the same. However, in some operating modes, the resonance frequency would be further away from the switching frequency and thus, the converter would not be operating at its optimal operating region from the efficiency point of view. The process implemented to carry out the resonance frequency matching is described below.

From the transformer leakage inductance, the theoretical values of the resonant capacitors at each port are calculated with (5) for the selected resonance frequency. Once the resonant capacitors are mounted on the PCB, the resonance frequency has to be retuned to compensate for the parasitic inductances. Firstly, the resonance frequency at one side of the transformer is found by short-circuiting the resonant capacitors at the other two sides and measuring the voltage gain after
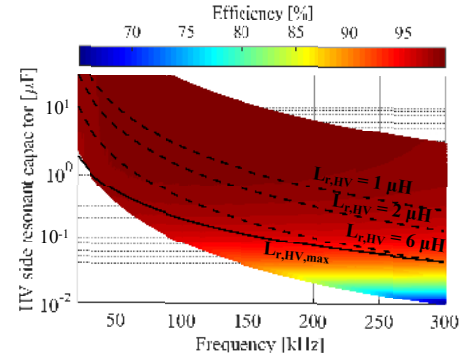
(a)
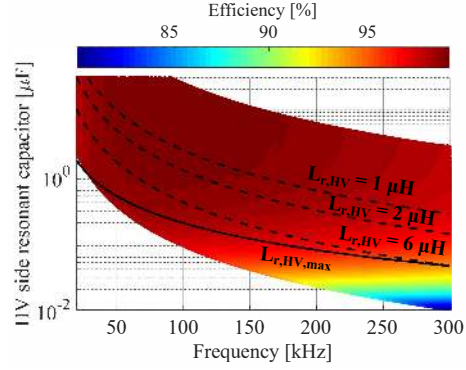
(b)

Fig. 8. Analysis of the TP-SRC efficiency in terms of switching frequency and resonant components size. Efficiency is calculated for dual-output mode with LV side as input at maximum output power with equal power sharing among ports. The dead-time has been selected to achieve the lowest rms current in each efficiency measurement.
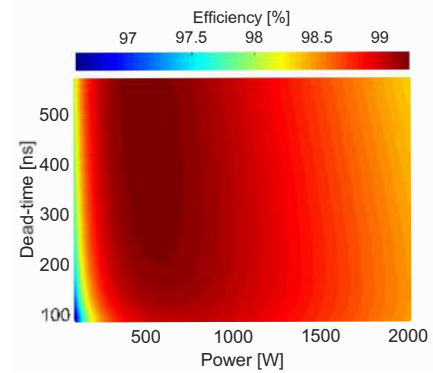

Fig. 9. Analysis of the TP-SRC efficiency in terms of t_d and power level. Efficiency is calculated for dual-output mode with LV side as input at $f_{sw} = 150\,\text{kHz}$ with $L_{r,HV} = 1.5\,\mu\text{H}$.

the resonance capacitor, as shown in Fig.10a. In that way, the resonance frequency obtained f_{req1} from the gain measured is only due to the capacitor at the input side and the overall resonance inductance of the resonant tank L_{eq1} as shown in Fig.10b. Then, from $f_{r,eq1}$ and C_{r1}, the equivalent resonance inductance L_{eq1} can be calculated as given in (23). The measurement is repeated for the other two ports to calculate the equivalent inductances L_{eq2} and L_{eq3}. Subsequently, the
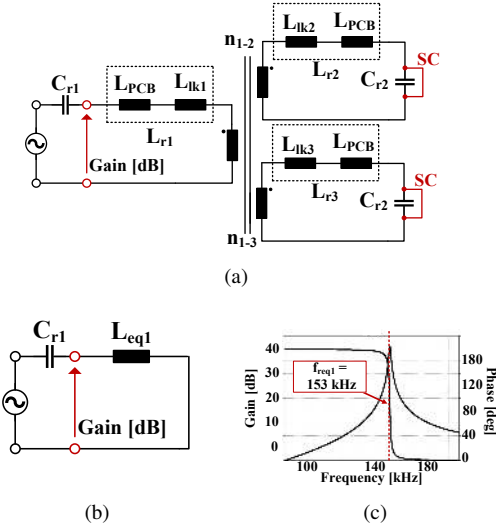
Fig. 10. Resonance frequency matching methodology. (a) Measurement set-up for Port-1: the gain after the resonant capacitor is measured with a Bode analyser. (b) Equivalent circuit of the measurement set-up, where L_{eq1} is the overall resonant inductance seen from Port-1. (c) Measured bode plot and equivalent resonance frequency due to C_{r1} and L_{eq1}.

resonance inductances L_{r1}, L_{r2} and L_{r3} can be calculated by solving the system given in (24). Finally, the resonant capacitors are recalculated to match the desired resonance frequency using (5).

$$L_{eq1} = \frac{1}{(2\pi f_{r,eq1})^2 C_{r1}} \quad L_{eq2} = \frac{1}{(2\pi f_{r,eq2})^2 C_{r2}}$$
$$L_{eq3} = \frac{1}{(2\pi f_{r,eq3})^2 C_{r3}} \tag{23}$$

$$L_{eq1} = L_{r1} + \left(\frac{1}{n_{12}^2 L_{r2}} + \frac{1}{n_{13}^2 L_{r3}}\right)^{-1}$$
$$L_{eq2} = L_{r2} + \left(\frac{n_{12}^2}{L_{r1}} + \frac{1}{n_{23}^2 L_{r3}}\right)^{-1} \tag{24}$$
$$L_{eq1} = L_{r1} + \left(\frac{n_{13}^2}{L_{r1}} + \frac{n_{23}^2}{L_{r2}}\right)^{-1}$$

VI. IMPLEMENTATION OF THE CONVERTER PROTOTYPE AND EXPERIMENTAL RESULTS

The TP-SRC prototype was designed for the specifications given in Table I with the GaN MOSFETs specified in Table II. A picture of the prototype is shown in Fig.11. According to the efficiency analysis, the ideal resonance frequency was selected at $140\,\text{kHz}$ and the three-winding transformer was constructed following the design analysis presented in section II.B for the selected frequency. The transformer was evaluated with an impedance analyser and the main parameters were extracted. The physical implementation of the transformer and the measured parameters are given in Table III. The resonant capacitors were calculated with the resonance frequency matching methodology given in section V. The resonant tank parameters are given in Table IV. The switching frequency
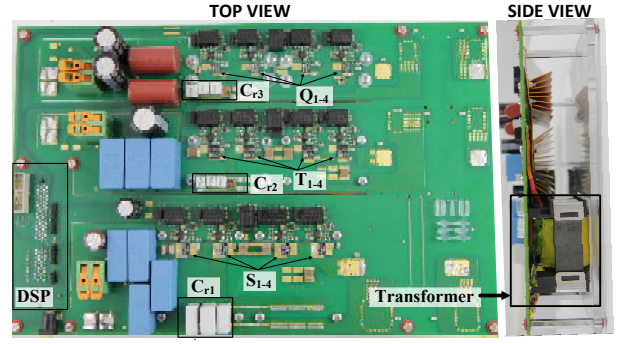

Fig. 11. Picture of the prototype.

TABLE III
TRANSFORMER SPECIFICATIONS

Core	No. of turns	Wire	R_{dc}	L_M
ETD	$N_1 = 6$	120 x AWG26	$2\,\text{m}\Omega$	$32.9\,\mu\text{H}$
59/31/22	$N_2 = 26$	20 x AWG26	$38\,\text{m}\Omega$	$817\,\mu\text{H}$
	$N_3 = 39$	20 x AWG26	$65\,\text{m}\Omega$	$1.88\,\text{mH}$

was selected at $133\,\text{kHz}$, which is $7\,\text{kHz}$ below the resonance frequency, in order to add some safety margin and ensure soft-switching operation. The dead-time utilized was $220\,\text{ns}$, which gives a high efficiency performance for the entire power range according to the analysis carried out in Section V.
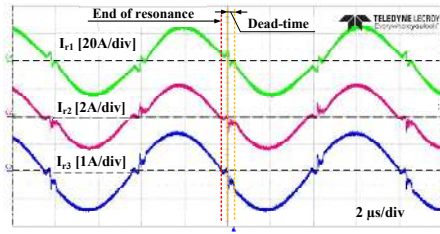
A. Experimental results

The experimental results were obtained with the converter operating in stead-state in dual-output mode with Port-1 ($V_1 = 80\,\text{V}$) as the input port. The main waveforms obtained are shown in Fig.12. In Fig.12a the resonant currents at the input side (I_{r1}) and output side (I_{r2} and I_{r3}) are presented. It can be observed that the resonance cycle ends before the switching event, where the input side switches turn-off and the dead-time interval begins. The output side currents I_{r2} and I_{r3} become zero before the turn-off event, and therefore the MOSFETs at the output sides operate in ZCS. Fig.12b shows the drain-source voltage and gate source voltage on the MOSFET S_4 at the input side and the resonant current I_{r1}. In Fig.12b ZVS operation and turn-off event with low current I_M can be verified.

The efficiency curve in function of the output power is shown in Fig.13, while the theoretical losses distribution is presented in Fig.14. The efficiency was measured in dual-output operation with an equal power sharing among output ports. A peak efficiency of $98.8\,\%$ was measured at $800\,\text{W}$, while at rated load an efficiency of $98.15\,\%$ was measured. From the losses distribution given in Fig.14, it can be observed

TABLE IV
RESONANT TANK PARAMETERS

C_{r1}	C_{r2}	C_{r3}	L_{r1}	L_{r2}	L_{r3}
$8\,\mu\text{F}$	$1.88\,\mu\text{F}$	$910\,\text{nF}$	$161.5\,\text{nH}$	$687.4\,\text{nH}$	$1.42\,\mu\text{H}$

(a)
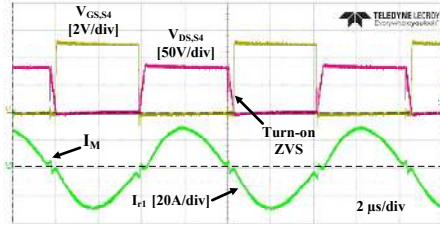
(b)

Fig. 12. Experimental results obtained in steady-state at $1.2\,\mathrm{kW}$ in dual-output mode with Port-1 ($V_1 = 80\,\mathrm{V}$) operating as input. (a) Tank circuit currents, (b) Tank current at input side, drain-source voltage and gate-source voltage of MOSFET S_4.
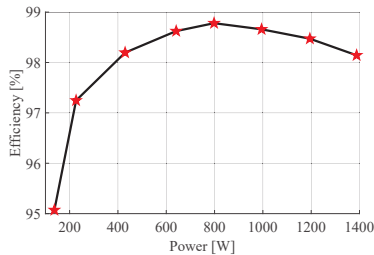

Fig. 13. Efficiency results in dual-output mode with Port-1 ($V_1 = 80\,\mathrm{V}$) operating as input.

that the MOSFETs at the input side are responsible of $65\,\%$ of the total losses, while the MOSFETs at both output sides are responsible for only $5\,\%$ of the losses. Such a large difference between the losses at the input side and the output side is due to the relatively large on-resistance of the MOSFETs at Port-1 compared to the other two MOSFETs. In order to decrease the conduction losses at Port-1, GaN MOSFETs with larger current rating should be selected.

VII. Conclusion

The multi port series resonant converter in open-loop operation is a promising topology to be used as a dc-dc statge of SST to interconnect multiple dc grids. In dc distribution systems for distributed energy sources, high efficiency power electronics are highly desired. In this paper, the losses analysis of the main components of TP-SRC has been presented. Then, the effect of the dead-time and resonance frequency to the rms currents and converter losses have been analysed and discussed. To further improve the converter efficiency, GaN MOSFETs with very low output capacitance and on-resistance were used. The resonance inductances of the resonant tank
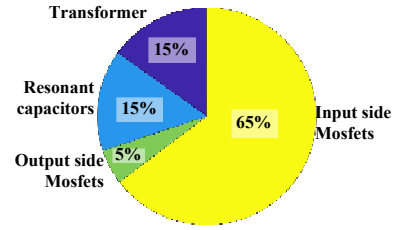

Fig. 14. Losses distribution on the main components of the converter at $1.4\,\mathrm{kW}$.

were integrated into the leakage inductance of the transformer and the PCB parasitic inductances. Because of the fixed switching frequency operation, a resonance frequency matching among the resonant tanks at each side of the transformer is required to operate the TP-SRC at its efficiency-wise optimal operating region. Therefore, a resonance frequency matching methodology was also presented in this paper. Finally, experimental results were provided for a $1.4\,\mathrm{kW}$ prototype. The proposed TP-SRC obtained a peak efficiency of $98.8\,\%$.

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