Through-Silicon-Via Inductor: Is it Real or Just A Fantasy?

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Outline

- Background and Motivation
- Micro-Channel Shield Technique
- Experimental Results
- Conclusions

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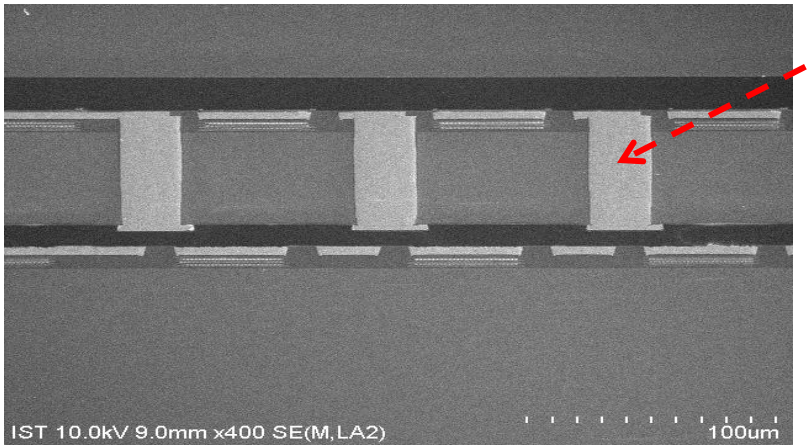
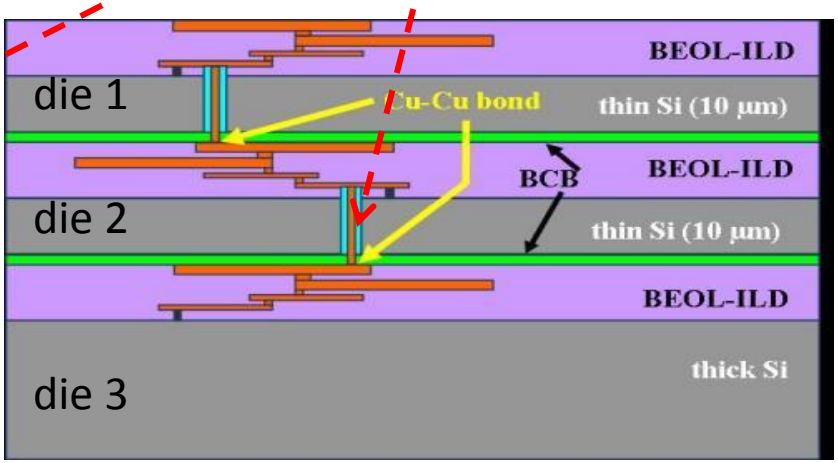
3D Integrated Circuits

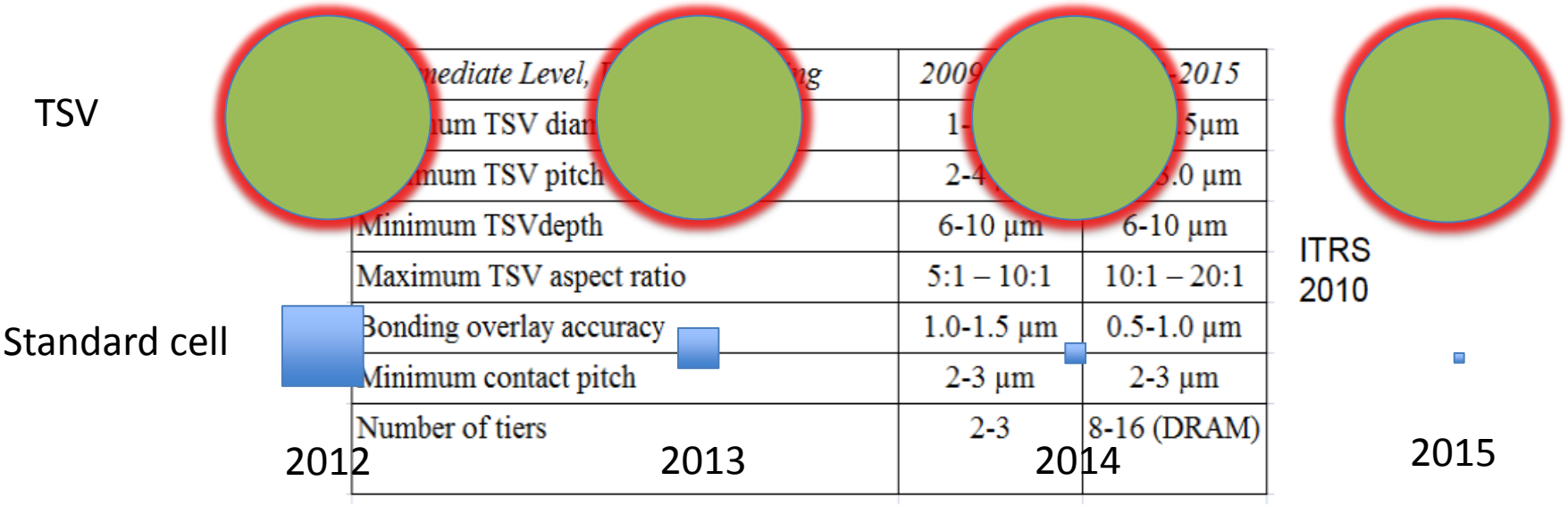
- 3D IC is considered one of the most promising alternatives at the limit of device scaling
  - *Reduced* form factor
  - *Reduced* interconnect length
  - *Compatible* with current technology
  - *Heterogeneous* integration

through-silicon vias (TSVs) for vertical links





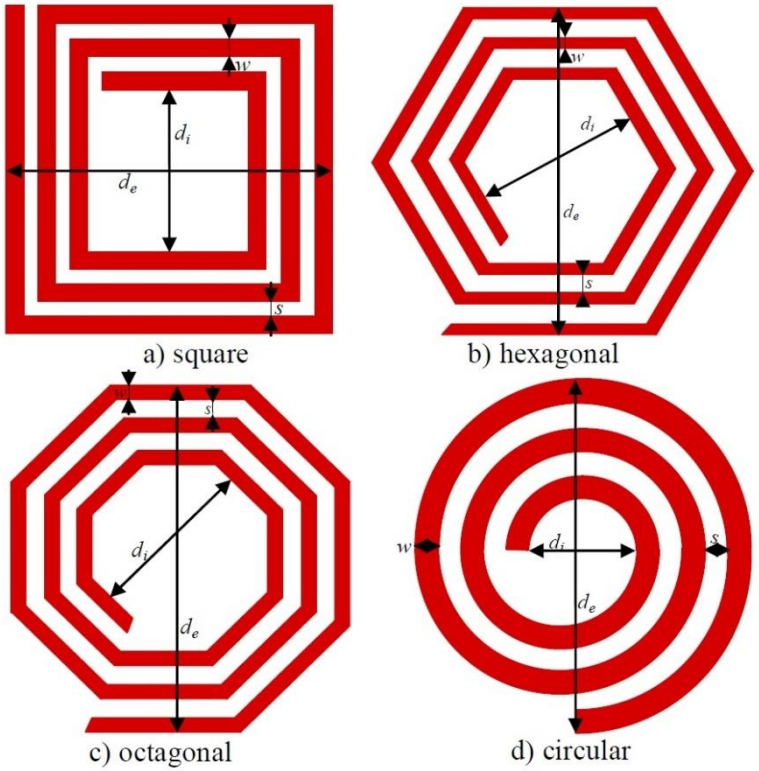
The Curse of TSV Scaling



…mediate Level, …ng	*2009*	*…2015*
…um TSV dia…	1-…	…5µm
…mum TSV pitch	2-4…	….0 µm
Minimum TSVdepth	6-10 µm	6-10 µm
Maximum TSV aspect ratio	5:1 – 10:1	10:1 – 20:1
Bonding overlay accuracy	1.0-1.5 µm	0.5-1.0 µm
Minimum contact pitch	2-3 µm	2-3 µm
Number of tiers	2-3	8-16 (DRAM)

- ✓ TSV scaling limited by the wafer handling and alignment accuracy
- ✓ TSV diameter will not scale with logic gates
  - → 50X diameter ratio, 2500X area ratio by 2015!

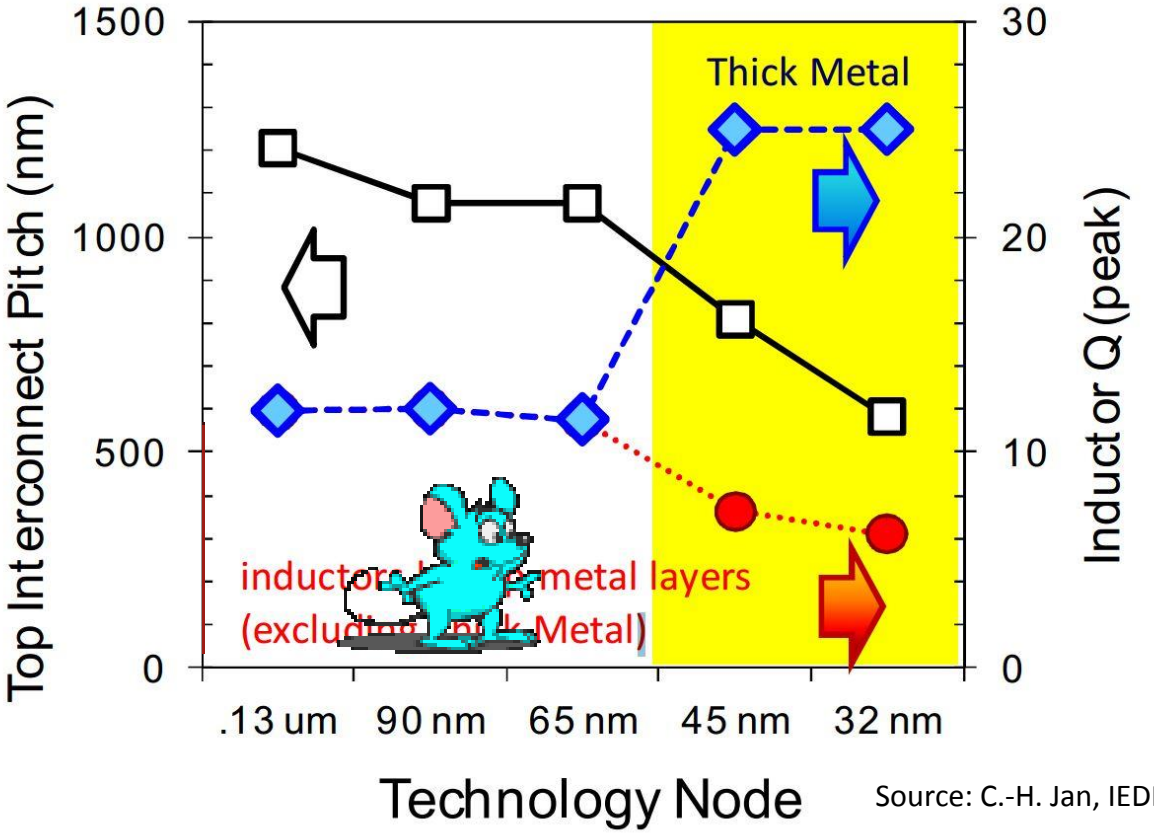
On-Chip Spiral Inductor



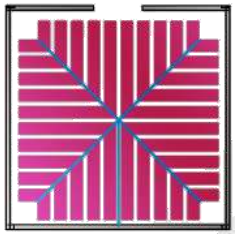
- Low-noise amplifiers, power amplifiers
- voltage control oscillators
- voltage regulators
- DC-DC converters

- Substrate loss
- Large die area (78,400 um^2) for practical purposes
- Consumes high routing area

The Curse of CMOS Scaling



Source: C.-H. Jan, IEDM'10

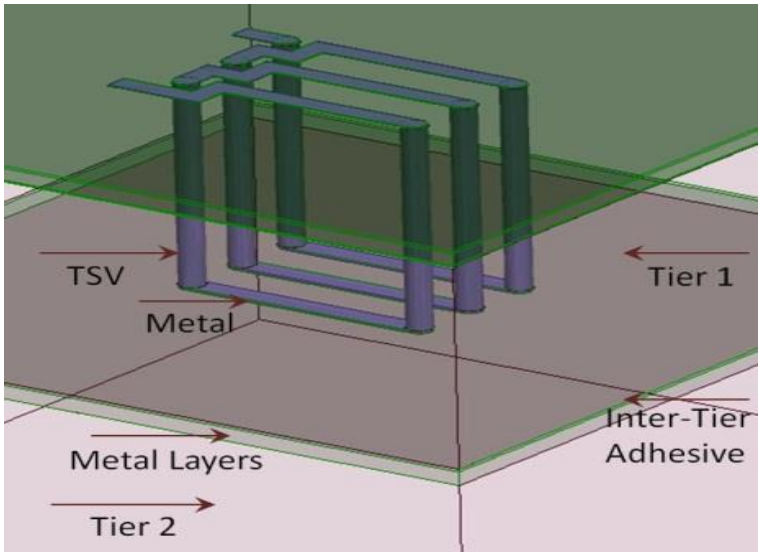


Patterned ground shield

Brought by scaling of the interconnect pitch and metal thickness

How about 3D RF SOC?

- Subject to both curses? 
  - Not necessarily!
- Use dummy TSVs to make inductors
  - Minimum footprint
  - No special RF process
  - Sounds fancy, but…
- Is it real or just a fantasy?
  - New loss mechanism?
  - New design freedom?



Prior Art and Motivation

- The quality factor of the TSV inductor is significantly less than its 2D spiral counterpart, mainly due to the losses from the substrate.
- The entire TSV inductors is buried in the silicon substrate, which is lossy at high frequencies.
- Bontzios et al suggested that for 50 µm substrate thickness and below, TSV inductor should be used when area is the only concern.
- Is there any way that we can reduce substrate losses for TSV inductors?

Contributions

- Novel shield technique using micro-channel.
- Experimental results states 21x and 17x increase of Q and L respectively.
- With this technique, TSV inductors can achieve up to 38x smaller area and 33% higher Q compared with spiral inductors.

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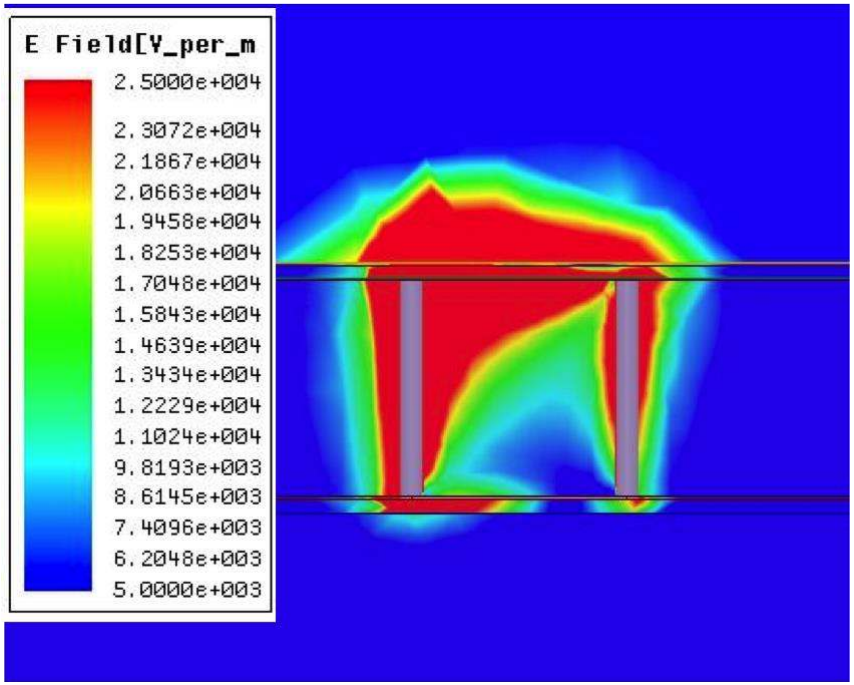
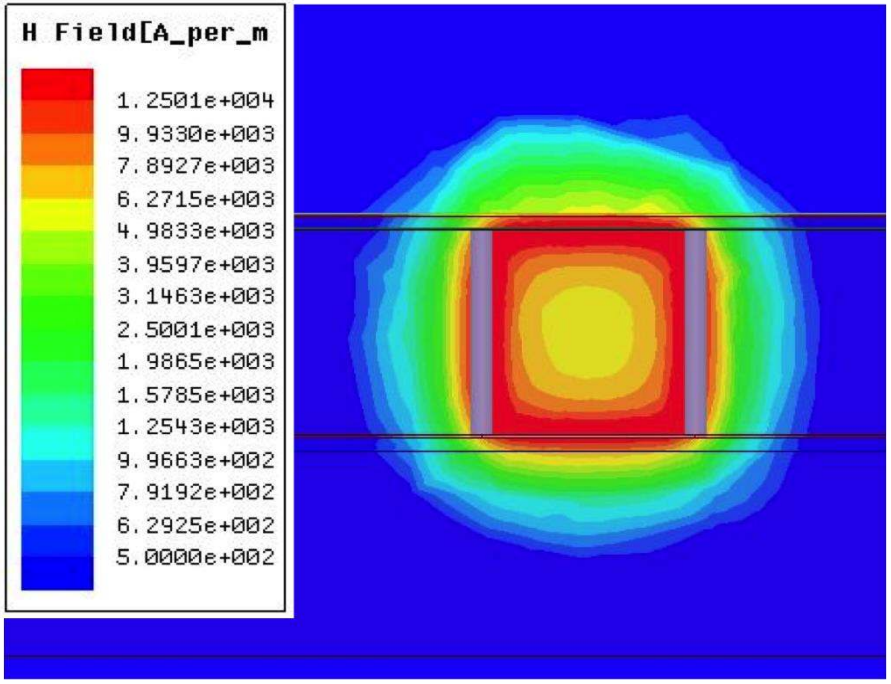
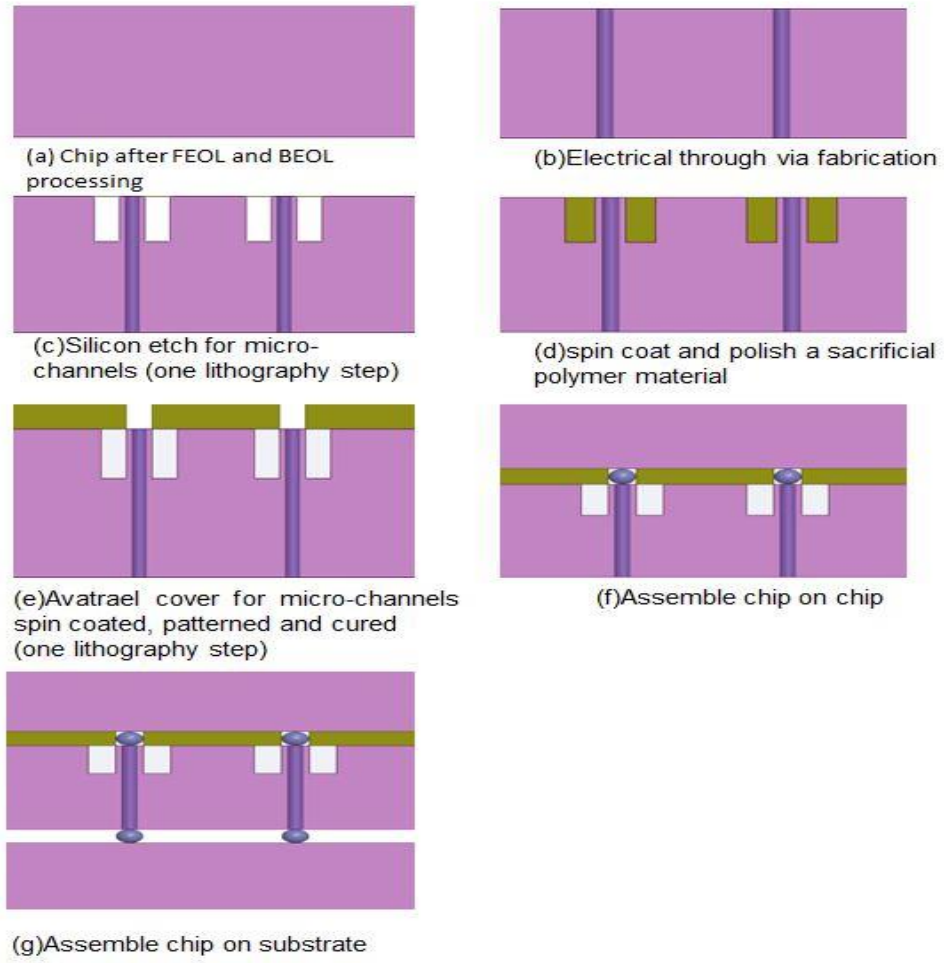
E Field and H Field without Shield





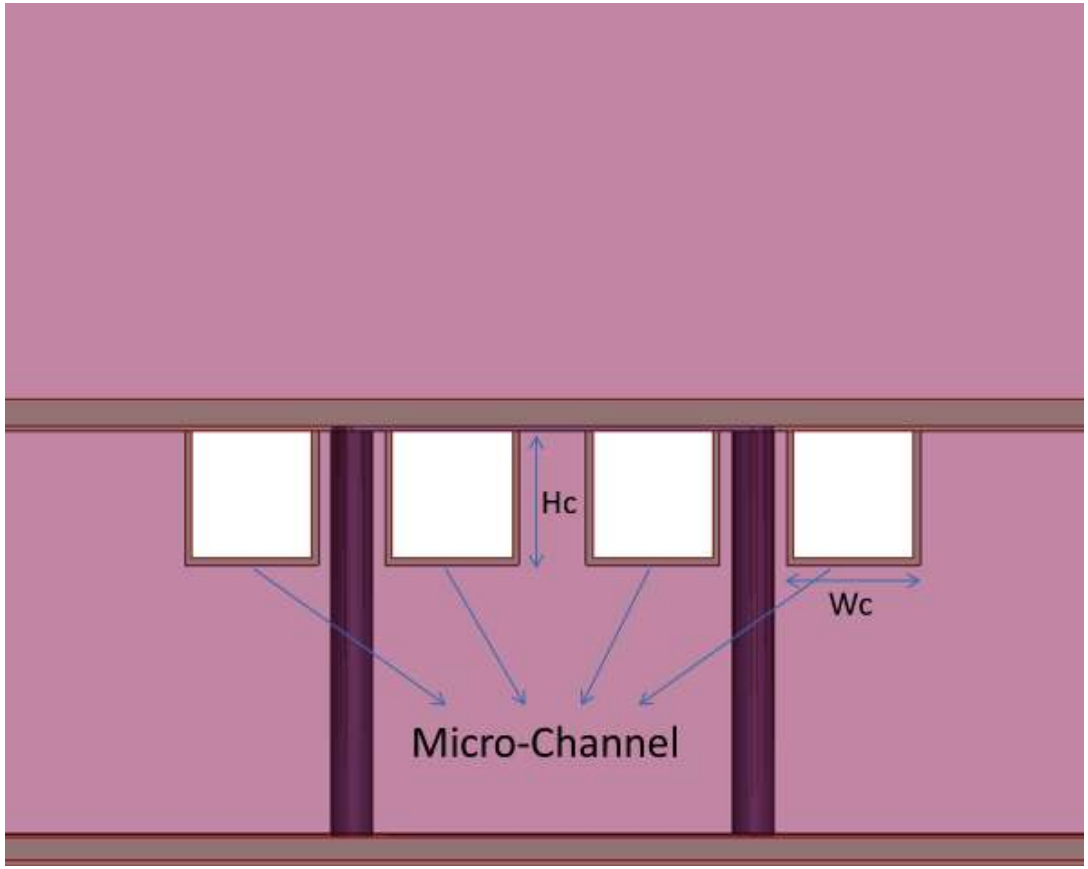
- Much of the losses are near the inductor.
- Losses can be reduced if substrate near inductor is removed.
- Substrate is removed by using micro-channel technique.

Micro-Channel Fabrication Steps



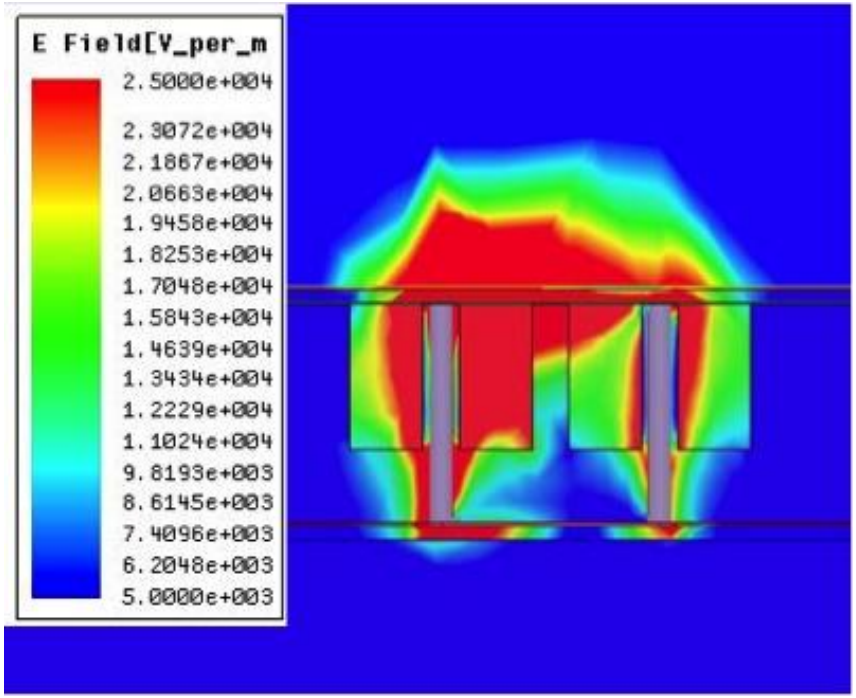
Adds little amount of cost due to two extra lithography steps.

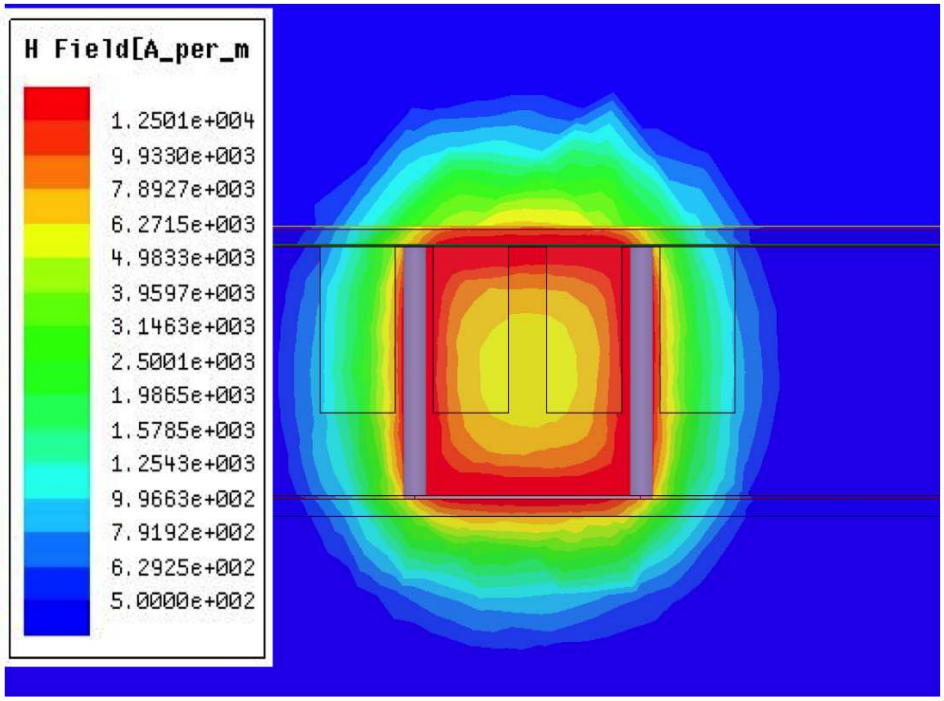
Micro-Channel Shields



- 4 Micro-channels are placed 5um away from the TSV.
- When the TSV inductor is used as antenna, the micro-channels can help to cool it as well.

E and H Field with Shield





- Losses are reduced due to the reduction of E-field in the substrate.
- Less effect on Inductance since no change in magnetic flux.

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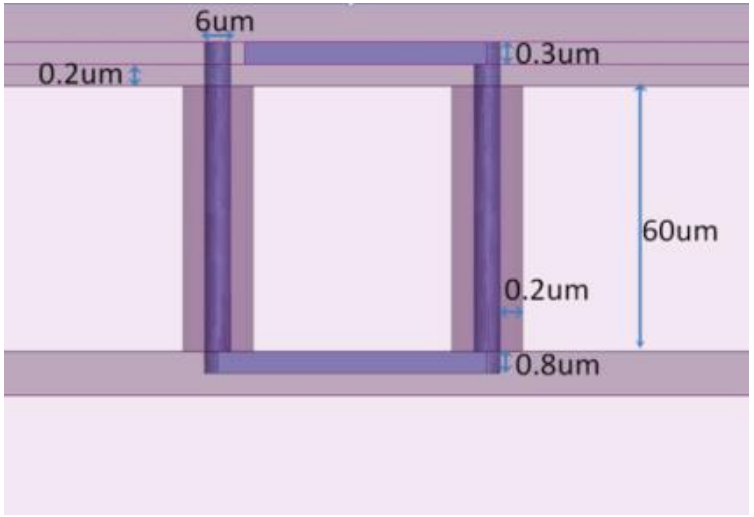
Experimental Setup

Notation	Meaning	Range
N	Number of turns	1-6
T	Number of tiers	2-4
P(μm)	Loop pitch	13-23
W(μm)	Width of metal strip	3-12
f(GHz)	Operating frequency	0.15, 1,5, 10



Nominal Settings

P=18um, W=6um,
f=0.15, 1, 5, 10 GHz

voltage regulators

RF applications

Improvement Using Micro-channel at Various Channel Dimensions

		W_c (um)					
		Quality Factor			Inductance (nH)		
		10	20	25	10	20	25
H_c (um)	10	6.71 (4.5%)	6.92 (8.1%)	7.03 (9.6%)	1.396 0.0%	1.395 0.0%	1.394 0.0%
	20	7.02 (9.6%)	7.29 (13.8%)	7.46 (16.3%)	1.393 0.0%	1.390 0.0%	1.390 0.0%
	30	7.34 (14.6%)	7.76 (21.1%)	7.94 (23.9%)	1.391 0.0%	1.386 0.0%	1.384 0.0%
	40	7.73 (20.5%)	8.28 (29.2%)	8.59 (34%)	1.388 0.0%	1.386 0.0%	1.382 0.0%
	50	8.25 (28.8%)	8.98 (40.1%)	9.41 (46.1%)	1.388 0.0%	1.380 0.0%	1.376 0.0%
	60	9.12 (42.2%)	10.34 (61.4%)	10.96 (71.0%)	1.386 0.0%	1.374 0.0%	1.377 0.0%

- N=6, T=2, P=18um, W=6um and f=10 GHz
- Improvement over no shield case are shown in parenthesis.

Maximum Q Improvement at 10 GHz

Q		T			
		2	3	4	5
N	1	10.96 (5.88%)	13.12 (14.5%)	14.53 (38.9%)	14.90 (70.3%)
	2	11.36 (11.7%)	11.31 (78.52%)	7.59 (168%)	6.14 (359%)
	3	11.89 (26.3%)	9.15 (167%)	4.65 (406%)	2.00 (2034%)
	4	11.89 (42.4%)	7.46 (269%)	2.93 (1007%)	1.03 N/A
	5	11.37 (55.3%)	5.97 (371%)	1.87 N/A	0.19 N/A
	6	10.98 (71%)	4.74 (483%)	1.01 N/A	-2.08 N/A

- P=18um, W=6um, Wc and Hc are max
- An average of 2.5x improvement in Q

Maximum Q Improvement at 1 GHz

Q		T			
		2	3	4	5
N	1	4.29 (0.0%)	3.74 (0.5%)	4.15 (1.0%)	4.44 (2.0%)
	2	3.36 (0.0%)	4.72 (3.2%)	5.37 (4.8%)	5.90 (9.9%)
	3	3.76 (0.2%)	5.28 (1.7%)	6.39 (15.8%)	6.83 (36.4%)
	4	4.02 (0.8%)	6.04 (11.1%)	7.11 (37.4%)	7.57 (88.3%)
	5	4.13 (0.1%)	6.49 (17.8%)	7.65 (67.0%)	7.78 (153.0%)
	6	4.29 (2.7%)	6.81 (26.5%)	7.92 (98.5%)	8.01 (235.1%)

- P=18um, W=6um, Wc and Hc are max

Maximum L Improvement at 10 GHz

L (nH)		T			
		2	3	4	5
N	1	0.135 (0.0%)	0.344 (0.0%)	0.577 (0.0%)	0.828 (1.2%)
	2	0.344 (0.0%)	0.958 (0.0%)	1.729 (0.0%)	2.708 (11.9%)
	3	0.594 (0.0%)	1.700 (0.0%)	3.523 (39.9%)	5.882 (1615%)
	4	0.843 (0.0%)	2.741 (1.0%)	5.959 (424%)	8.855 N/A
	5	1.093 (0.0%)	3.390 (2.2%)	8.577 N/A	3.055 N/A
	6	1.376 (0.0%)	5.206 (58.5%)	10.634 N/A	-3.518 N/A

- P=18um, W=6um, Wc and Hc are max
- Increased fSR brought by the shield.

Q Factor and Area Comparison Between 2D Spiral Inductors and 3D TSV inductors

Design Specs			Spiral Inductor						TSV Inductor						
#	f (GHz)	L (nH)	Geometry				Q	A (um^2)	Geometry				Q		A (um^2)
			T (um)	D (um)	d (um)	W (um)			N	T	W (um)	P (um)	w/o Shield	w/ Shield	
1	1	6.5	2	560	535	10	5.7	313,600 (1)	6	2	7	20	4.6	7.6	8,255 (1/37.9x)
2	5	2.50	2	400	355	20	6.9	160,000 (1)	4	3	6	18	4.3	10.3	9,358 (1/17.1x)
3	10	0.95	1	330	320	10	10.0	108,900 (1)	2	3	6	18	5.8	10.1	4,679 (1/23.3x)

- 38x area reduction.
- 33% Q improvement

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Conclusions

- A micro-channel shield technique to drastically improve the quality factor and the inductance is proposed.
- 21x and 17x increase of Q and L respectively are observed using the technique.
- 38x smaller area and 33% higher Q compared with spiral inductors can be achieved with this technique for TSV inductors.

Thank you!