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Through silicon vias filled with planarized carbon nanotube bundles**

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Abstract

The feasibility of using carbon nanotube (CNT) bundles as the fillers of through silicon vias (TSVs) has been demonstrated. CNT bundles are synthesized directly inside TSVs by thermal chemical vapor deposition (TCVD). The growth of CNTs in vias is found to be highly dependent on the geometric dimensions and arrangement patterns of the vias. The CNT-Si structure is planarized by a combined lapping and polishing process to achieve both a high removal rate and a fine surface finish. Electrical tests of the CNT TSVs have been performed and their electrical resistance was found to be in the kΩ range. The reasons for the high electrical resistance have been discussed and possible methods to decrease the electrical resistance have been proposed.

1. Introduction

While shrinking the transistor size on silicon chips appears to be slowing down due to various physical and technological limits, the continuous downscaling of electronics in the future is expected to be driven mainly by the integration of components within packages at the system level, especially by stacking chips in a 3-dimensional (3D) manner [1, 2]. The short interconnection paths in such 3D structures can also improve the electrical performance of the systems [2]. One key enabling technology for 3D chip stacking is the formation of through silicon vias (TSVs), which have been realized in various ways [3-5]. The most common method to fill the TSVs and make them conductive is by deposition or plating of metals, such as copper [5, 6], tungsten [7], and zinc [8]. Despite the high integration density and performance improvement, stacking chips and connecting them by TSVs have raised concerns over the reliability [9-11] and thermal management issues [12-13]. The reliable fabrication of systems with 3D-stacked chips and the efficient heat dissipation from such structures with very high power density still remain as big challenges.

Due to their unique mechanical, thermal, and electrical properties, carbon nanotubes (CNTs) have been proposed as a promising candidate material to make interconnects for electronics [14], among many other applications [15]. The attractive mechanical properties CNTs offer, including a high Young's modulus [16], good flexibility and resilience [17], and a low coefficient of thermal expansion [18], offer great advantages in making strong and reliable interconnects. The high thermal conductivity of CNTs [19] may make interconnects good heat removal paths in densely packed electronics systems. Their high current density carrying capacity and stability against electromigration [20] are also beneficial for interconnection technology.

The research work performed on developing CNT interconnects falls into two categories, namely on-chip and off-chip interconnects. CNT on-chip interconnects have been realized by various technical routes. The majority of the work is focusing on vertically aligned CNTs in via interconnects [21-25]. CNT interconnects in the form of horizontal wires have also been demonstrated [26, 27]. Attempts at making CNT off-chip

interconnects bridging chips with substrates or other chips have also been made. Iwai *et al.* and Soga *et al.* developed CNT flip chip bumps which are highly thermal conductive and mechanically flexible [28, 29]. Recently, CNTs have also been proposed to be used in TSV interconnects. In contrast to on-chip via interconnects with a typical depth smaller than 0.5 μm [21-25], TSVs are normally several tens to several hundreds of micrometers deep. This big difference in scale requires the growth of much longer CNTs and consequently modified planarization processes compared to the on-chip cases. Xu *et al.* have demonstrated the growth of CNT bundles in 100 μm deep TSVs but haven't performed any planarization processes [30].

In the present study, CNT-filled TSVs have been developed by using a new process as opposed to the previous method of Xu *et al.*'s [30], avoiding any wafer bonding steps. Furthermore, we employed a unique post-growth lapping and polishing process to planarize the tall CNT bundles that grow out of the vias. This process is needed as a preparation for the potential subsequent processes such as metallization and chip-to-chip or wafer-to-wafer bonding. The current-voltage responses of the CNT-TSVs have also been measured.

2. Experimental details

The fabrication process of the CNT-filled TSVs is shown in figure 1. The process starts by photolithography on a 3-inch Si wafer. The Si wafer is then etched by a deep reactive ion etching (DRIE) process to create vias with different depths. A 10 nm thick Al_2O_3 layer followed by a 1 nm thick Fe layer are then evaporated onto the wafer as the catalyst for CNT growth. After that the photoresist is stripped off and then the wafer is cleaned by isopropanol and deionized water. This step also serves as a lift-off process and leaves the catalyst layer only at the bottom of the Si vias. The wafer is diced into small chips before being taken into the CNT growth process. These preparation steps for CNT growth are illustrated in figure 1 (a)-(d).

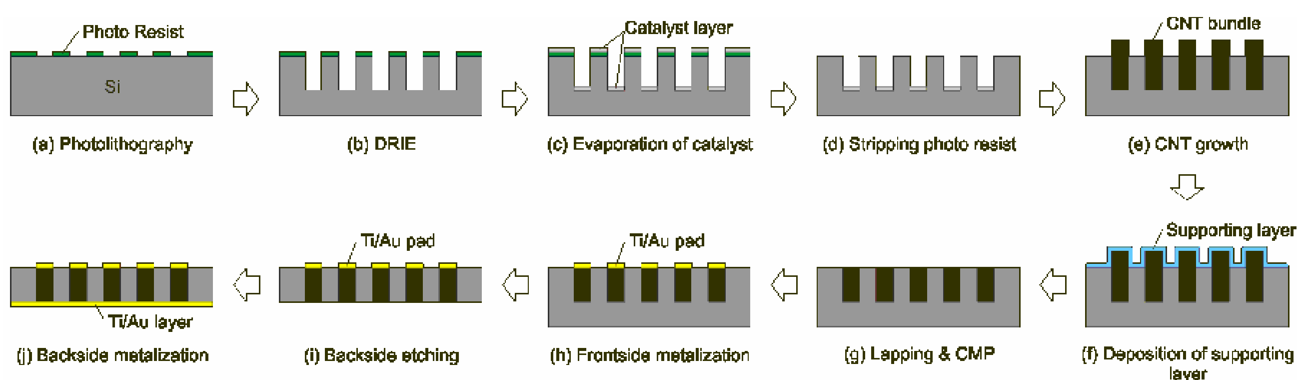

Figure 1. Fabrication process of the CNT-filled TSVs. (a) Photolithography to define the shapes and patterns of the vias. (b) DIRE to etch deep vias into Si. (c) E-beam evaporation of the catalyst layer. (d) Stripping the photo resist to remove the catalyst deposited on the top of the Si, leaving catalyst only at the bottom of the

vias. (e) TCVD to grow CNT bundles from the bottom of the vias. (f) Deposition of supporting layer to mechanically hold the CNTs during the following planarization process. (g) Lapping and CMP to planarize the Si-CNT structure. (h) Photolithography, evaporation and lift-off to form metal pads on the frontside. (i) Dry etching of Si from the backside to expose the bottom of the vias. (j) Sputtering of conduction layer onto the backside.

The CNTs are grown by thermal chemical vapor deposition (TCVD) using two different growth systems in this study. The first set up is a home-made TCVD system operatied under atmospheric pressure. The chip is inserted into rge middle of a quartz tube of 4cm diameter inside a furnace of 50cm length. The chip is first heated up to 700 °C in a flow of 900 standard cubic centimeters per minute (sccm) argon and 100 sccm H_2 at atmospheric pressure. The sample is kept at 700 °C for 15 minutes before adding acetylene (C_2H_2) into the reactor to start the growth of CNTs. 3 to 6 sccm C_2H_2 is applied for the CNT growth in a mixed flow of 500 sccm Ar and 500 sccm H_2. The flow of C_2H_2 is turned off after 5 to 20 minutes to terminate the CNT growth. The sample is then cooled down to room temperature in 900 sccm Ar and 100 sccm H_2 flow before being taken out of the growth reactor. We also used a commercial growth system (Black Magic II. Aixtron) to grow CNTs under low pressure. The chip is placed onto a graphite heater, above which a showerhead is used to deliver well-mixed gases in the vertical direction. The catalyst is annealed at 500°C in a flow of 692 sccm H_2 for 3 min. After that, the temperature is elevated to 700°C and 200 sccm C_2H_2 is added to start the CNT growth, which lasts for 90-120 s for chips with different via depth. The pressure is kept at around 10 mbar during the growth process. The growth step is illustrated in figure 1(e).

One major part of the present study is the development of a planarization process of the as-grown CNT-Si structure (figure 1 (f) and (g)). This planarization process is necessary due to the difficulty of controlling the length of the CNTs to be exactly equal to the depth of the Si vias. The flat surface created by this planarization process will enable the subsequent processing steps on the CNTs, such as metallization and bonding. Horibe *et al.* [24] and Yokoyama *et al.* [25] also claim that polishing of multiwalled carbon nanotubes (MWNTs) may make their inner shells contribute to the electrical conductions. The conduction of the MWNT bundles can thus be improved. Prior to the planarization of this structure, a supporting layer is deposited to hold the CNT bundles. Otherwise the CNT bundles are easily deformed or pulled out of the vias during the planarization process. Both the work of Horibe *et al.* [24] and the work of Yokoyama *et al.* [25] focused on the development of an on-chip vertical CNT via interconnects, the depth of which is below 0.5 μm. The top of the as-grown CNT bundles in their work is only about a half to a few micrometers higher than the surface of the chip. Therefore they could deposit a thin supporting layer and employ chemical mechanical polishing (CMP) afterwards to flatten the structures. Horibe *et al.* [24] used a spin coated thin photoresist (S1813) and Yokoyama *et al.* [25] used a spin-on glass (SOG) layer for this purpose. In our case, the length of the CNTs is on the order of a few hundred micrometers and they stick out from the chip surface for more than tens of

micrometers. Therefore a thick supporting layer has to be used in our study. A thick negative photoresist SU-8 10 (Microchem) is thus chosen as the supporting layer. However directly applying photoresist on CNT bundles can cause deformation and densification of the bundles, a phenomenon also observed by Futaba *et al.* [31] and Garcia *et al.* [32]. To prevent CNT bundles being wetted by the photoresist, a 800 nm thick Si layer is sputtered onto the chip with CNTs grown from the vias. The SU-8 10 photoresist is then spin coated onto the chip at a rotating speed of 2000 revolutions per minute (rpm), resulting in a final film thickness of approximately 15 µm. The SU-8 10 is exposed to 400 nm wavelength ultraviolet (UV) light for 30 seconds after being soft baked at 65 °C for 2 minutes and at 95 °C for 5 minutes. Post-exposure bake is performed at 65 °C for 1 minute and at 95 °C for 2 minutes. Hard bake at 180 °C for 45 minutes is finally done to finish this step.

The planarization of the CNT-Si structure is performed on a lapping and polishing machine (Logitech PM5). It begins with a lapping step which quickly removes the materials, followed by a CMP step to fine polish the surface. The lapping is done on a glass lapping plate rotating at a speed of 25 rpm, assisted by a suspension containing 3 µm Al_2O_3 powders (Logitech). After the whole supporting SU-8 layer is removed, the sample is further polished on a polishing cloth (Logitech Chemcloths) rotating at a speed of 30 rpm for 15 to 20 minutes. This CMP step is done with SF1 polishing fluid (Logitech). Both lapping and CMP are performed under a low pressure of 15 kPa. After CMP the sample is rinsed in acetone and deionized water and then undergoes a post-CMP cleaning process similar to the standard cleaning (SC) of Si wafers. At room temperature, the sample is immersed sequentially in SC1 solution for 5 minutes, in 2% HF solution for 30 seconds, and in SC2 solution for 5 minutes.

A series of processes is executed after the planarization to finalize the fabrication of the CNT-TSVs and facilitate the electrical measurement (figure 1 (h)-(j)). First, 20/80 nm thick Ti/Au pads are made on the top of the planarized CNT bundles by photolithography, evaporation and lift-off processes. A dry etching process is then done to remove the Si from the backside of the chip until the bottom of the vias is revealed. A 30/400 nm thick Ti/Au layer is sputtered on the etched backside to form a conducting surface.

The characterization procedures are performed during and after the fabrication processes. The depth of the Si vias is measured by an optical surface profiler. The chips after CNT growth and planarization are observed by a scanning electron microscope (SEM). Some chips with CNTs grown in vias are etched in SF_6 and O_2 plasma to remove the surrounding Si and expose the CNT bundles for easy SEM observation. To characterise the structure of the CNTs, chips with CNTs grown in vias are immersed into methanol and then sonicated for 30 min to detach and disperse the CNTs. One drop of methanol containing CNTs is put onto a copper grid and dried in air for transmission electron microscope (TEM) observation. The current-voltage (I-V) response of the CNT-filled vias is measured by a two point method on a probe station connected to a multimeter. One probe is put on the top of a CNT via and the other probe is connected to the conductive holder of the probe

station which touches the backside of the chips. To ease the positioning of the probe on the top of the CNT via, about 5 µm thick Si is etched from the frontside to make the CNT bundles extend out of the Si surface.

3. Results and discussions

We have shown that CNTs can be successfully grown from the bottom of the vias deeper than 100 µm using both TCVD growth systems mentioned above. However, the growth results from the two systems differ in terms of uniformity and controllability. Using the homemade system, the growth of CNTs at atmospheric pressure from deep Si vias is found to behave differently from that on a flat surface, possibly due to the differences of gas diffusion to the catalyst at the bottom of the vias giving different conditions of growth [33]. First, a relatively high flow rate of C_2H_2 needs to be applied to achieve long and uniform CNT bundles. In the present study, a narrow process window of 5-6 sccm flow rate of C_2H_2 is found to generate reasonably good growth results. Furthermore, the growth of CNTs in deep Si vias is highly dependent on the arrangements and geometric dimensions of the vias. For example, two chips cut from the same wafer, carrying vias with the same diameter and depth but in different arrangements (figure 2 (a) and (b)), undergo the same growth conditions but produce different results. It can be clearly observed that CNTs grown from vias in an array arrangement (figure 2 (a)) are quite uniform while those grown from vias in a peripheral arrangement (figure 2 (b)) are not uniform. A similar comparison can be made between two chips from the same wafer but with different geometric dimensions. A chip with 50 µm diameter and 162 µm depth vias and a chip with 20 µm diameter and 131 µm depth vias under the same growth conditions give very different results. CNT bundles grown from the former one (figure 2 (c)) are very uniform and well aligned and those from the latter one (figure 2(d)) are not uniform. Some CNTs on the chip shown in figure 2 (d) are even not tall enough to stick out from the vias. On the other hand, the growth performed under low pressure using the commercial growth system shows better uniformity and controllability for vias with different dimensions and in different arrangements. We have grown CNT bundles in vias with depths from 86 to 139 µm and arranged in different patterns, all of which give good uniformity over the whole chip. As examples, figures 2(e) and (f) show the uniform CNT bundles grown on two chips with 50 µm diameter and 120 µm depth vias in different arrangements. The chips shown on figure 2(e) are further etched to reveal the structure of the CNT bundles inside the vias (figures 2(g) and (h)). It can be observed that the CNT bundles are straight and the CNTs are well aligned inside the vias. A TEM image of the CNTs grown in vias is shown in figure 3, from which the straight tubular structure of the CNTs can be clearly seen.

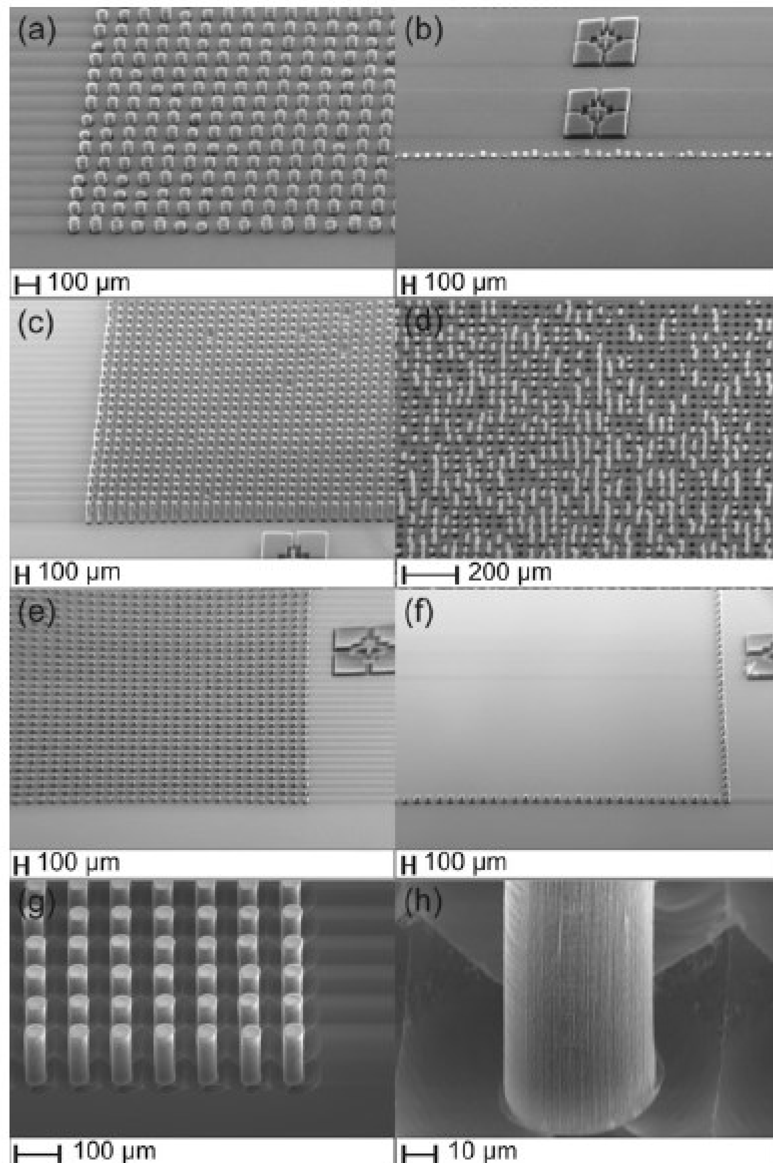

Figure 2. SEM images of CNT bundles grown from the bottom of deep Si vias with different arrangements and geometric dimensions. (a) Vias with 50 µm diameter and 125 µm depth in an array arrangement. (b) Vias with 50 µm diameter and 125 µm depth in a peripheral arrangement. (c) Vias with 50 µm diameter and 162 µm depth. (d) Vias with 20 µm diameter and 131 µm depth. (e) Vias with 50 µm diameter and 120 µm depth in an array arrangement. (f) Vias with 50 µm diameter and 120 µm depth in a peripheral arrangement. (g) and (h) The chip in (e) after Si surrounding the CNT bundles has been etched away. Note that (a) –(d) are results grown under atmospheric conditions from the home –made TCVD system and (e)-(h) are results grown under low pressure from the commercial growth system.

The lapping and CMP processes described in section 2 are shown to be able to effectively planarize the CNT-Si structures. Figure 4 shows SEM pictures taken both before and after the planarization step. The flat surface created by the planarization process is essential for the subsequent processes.

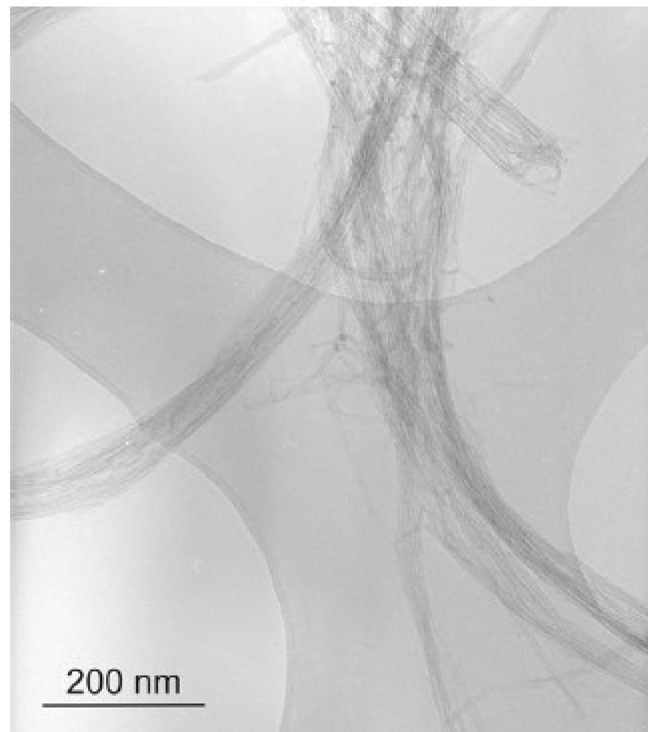

Figure 3. TEM image of CNTs grown inside vias.

The measured I-V curves of the CNT vias are highly linear, three examples of which, measured from vias with 50 μm diameter and 86 μm, 120 μm and 139 μm depth, respectively, are shown in figure 5(a). These three samples grown by a commercial growth system under low pressure have 0.21 kΩ, 0.28 kΩ and 0.34 kΩ, resistances respectively. From the depth and resistances measured, it can be estimated that the contact resistance in our configuration is much smaller than the bulk resistance of the CNT bundles (figure 5(b)), although further investigation on this issue needs to be done. We also measured filled vias with CNTs grown by the homemade system under atmospheric pressure, which are 50 μm in diameter and 125 μm deep. The resistance of the vias in these dimensions is approximately 1.8 to 2.0 kΩ, which is about one order higher than that grown at low pressure probably due to the poorer tube quality grown at high pressure. This value is however, very close to the result previously reported by Xu *et al.* [30] although our tested vias are about 25 μm deeper. These resistance values are far too high for real application purposes.

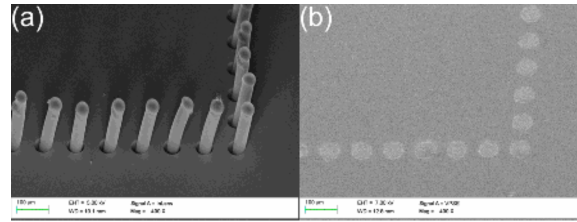

Figure 4. SEM images of CNT bundles before (a) and after (b) the planarization process.

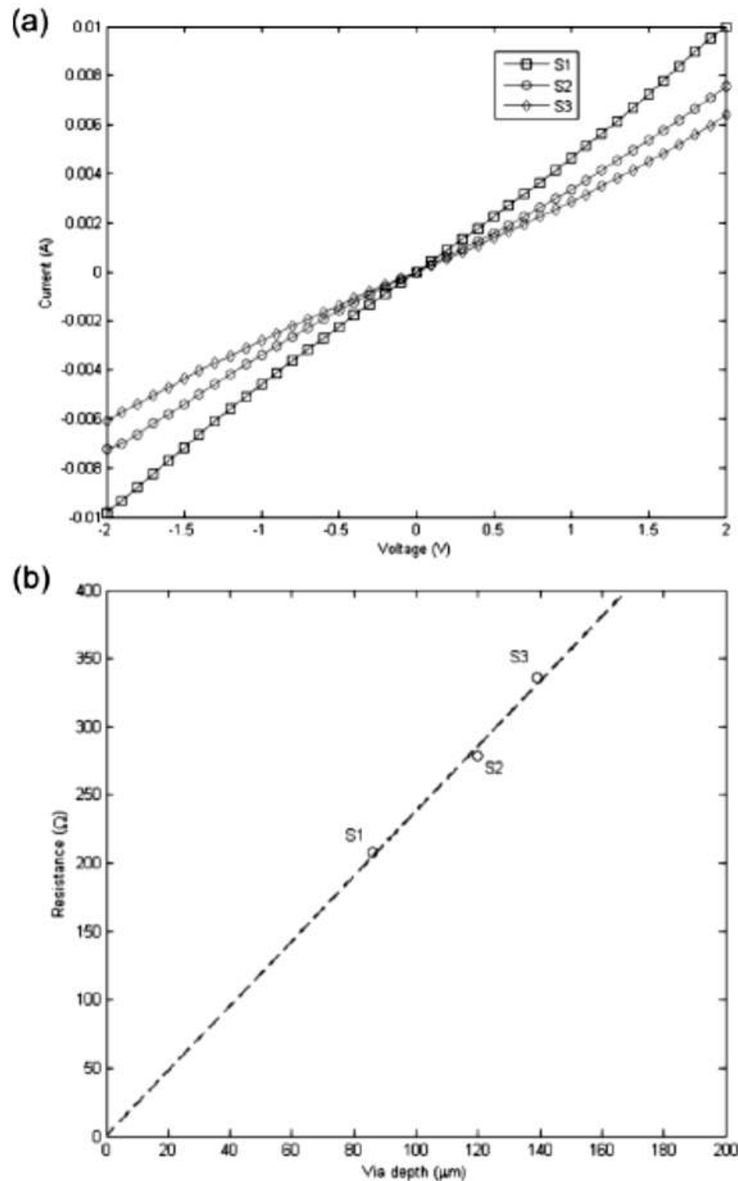

Figure 5. (a) I-V curves of a measured CNT-filled TSV. S1(square): 86 μm deep via: S2 (circle): 120 μm deep via: S3 (diamond): 139 μm deep via. The corresponding resistances are 0.21 kΩ, 0.28 kΩ and 0.34 kΩ, respectively. (b) Estimation of the contact resistance based on S1, S2 and S3.

Obviously, there is a big gap in trying to repeat the results obtained from measurements on single CNTs with lengths in the range of a few micrometers [20, 25] for CNT bundles with lengths in the range of one or two hundred micrometers. Two major reasons can be identified as follows. First, the actual filling ratio of CNTs in a bundle is very low, i.e. there are large empty spaces among the nanotubes within a bundle. Vertically aligned arrays of multiwalled nanotubes typically have a porosity on the order of 90% [34]. Second, the CNTs grown by TCVD may suffer from structural defects. There are many bends on a CNT with a length of hundreds of mirometers, as well as many crossings from neighboring nanotubes. Huang *et al.* experimentally demonstrated that the resistance of a nanotube is dramatically increased by introducing bends during its growth [35]. The large empty space among the nanotubes, as well as their bends and crossings, can be clearly observed from the sideview SEM image of an as-grown CNT bundle shown in figure 6.

Based on the discussion above, several technical routes can be proposed to decrease the resistance of the CNT vias to an acceptable level. A post-growth densification method [31] can be applied to create densely packed bundles of CNTs, which might be used to fill Si vias afterwards. Regarding the growth method, plasma-enhanced CVD (PECVD) can be used to produce CNTs with better straightness and alignment. Morjan *et al.* demonstrated, using PECVD, the growth of CNTs longer than 150 μm [36], a length long enough for the TSV application. The growth method may be adapted to grow CNTs inside deep vias. Besides, post-growth plating of metals on CNTs has also been shown [37] where the metal contributes to the electrical conduction while CNTs act as good mechanical connections.

We have also made estimation of the resistance of TSVs filled with perfect CNTs using a compact physical model developed by Naeemi and Meindl [38]. Assuming the CNTs have 30 μm outer diameter, 15 nm inner diameter, 100 μm length and 1 μm electron mean free path [39], the resistance of one such multiwalled CNT can be estimated to be 40 kΩ. We also assume the CNTs are arranged in a square lattice with 70nm spacing between the neighbouring tubes, which leads to a tube density of 100 tubes μm^{-2} and a 93% porosity, a value very close to that reported in [34]. The resistance of a via with 50 μm diameter can be estimated as 40 $k\Omega/[100\ \mu m^{-2}\pi(25\ \mu m)^2] = 0.20\ \Omega$. If the CNTs are assumed to be closely packed in a hexagonal lattice, the tube density is then 1.3 thousand tubes μm^{-2} and the via resistance can thus be reduced to 0.016 Ω. This calculation shows the potential of CNT-filled TSVs, as well as the importance of producing closely-packed CNTs of good structural quality.

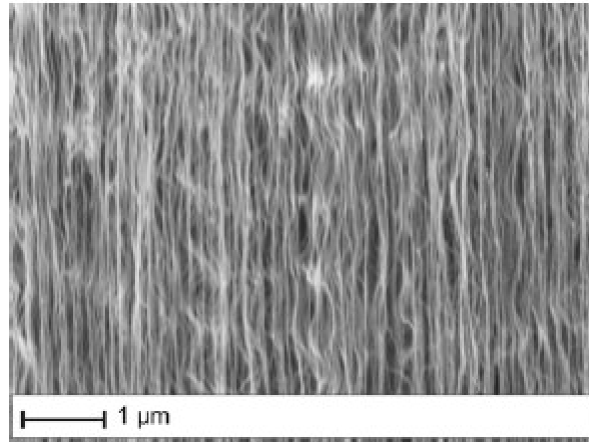

Figure 6. Sideview SEM image of an as-grown CNT bundle. The large empty space among the CNTs and their bendings and crossings can be clearly observed.

4. Conclusions

In summary, we have demonstrated the feasibility of using CNT bundles to fill deep TSVs, which may be used for future 3D stacking of integrated chips. CNTs can directly grow from deep TSVs but we found that their growth is highly dependent on the arrangements and the dimensions of the vias. A post-growth planarization process has been successfully developed to flatten the CNT-Si structures. Electrical tests of the CNT vias have also been performed. The resistance of vias with 50 µm diameter is of the order of a few hundred ohms. The reasons for this high resistance and possible routes to decrease it have also been discussed.

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