

Time-Dependent Dielectric Breakdown of 4H-SiC/SiO₂ MOS Capacitors

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Abstract—Time-dependent dielectric breakdown (TDDB) is one of the major issues concerning long-range reliability of dielectric layers in SiC-based high-power devices. Despite the extensive research on TDDB of SiO₂ layers on Si, there is a lack of high-quality statistical TDDB data of SiO₂ layers on SiC. This paper presents comprehensive TDDB data of 4H-SiC capacitors with a SiO₂ gate insulator collected over a wide range of electric fields and temperatures. The results show that at low fields, the electric field acceleration parameter is between 2.07 and 3.22 cm/MV. At fields higher than 8.5 MV/cm, the electric field acceleration parameter is about 4.6 cm/MV, indicating a different failure mechanism under high electric field stress. Thus, lifetime extrapolation must be based on failure data collected below 8.5 MV/cm. Temperature acceleration follows the Arrhenius model with activation energy of about 1 eV, similar to thick SiO₂ layers on Si. Based on these experimental data, we propose an accurate model for lifetime assessment of 4H-SiC MOS devices considering electric field and temperature acceleration, area, and failure rate percentile scaling. It is also demonstrated that temperatures as high as 365 °C can be used to accelerate TDDB of SiC devices at the wafer level.

Index Terms—Reliability, time-dependent dielectric breakdown (TDDB), 4H-silicon carbide (SiC) MOS capacitors.

I. INTRODUCTION

EXCELLENT material properties are possessed by 4H-silicon carbide (SiC) for high-temperature, high-frequency, and high-power applications. It has a wide bandgap (3.26 eV), a high thermal conductivity (more than twice higher than Si), a high critical field (2.2 MV/cm versus 0.25 MV/cm for Si), a high saturated drift velocity (higher than GaAs), and high thermal stability; it is chemical inert; and it forms a native oxide. Despite these beneficial properties, the current SiC MOSFET technology still suffers from performance and reliability problems that prevent its application for commercial power devices.

The reported channel mobility values of SiC MOSFETs with thermally grown SiO₂ are extremely and unacceptably low (less

than 10 cm²/V · s). This poor mobility is attributed to the high density of traps at and near the SiO₂/SiC interface [1]. Postoxidation annealing of the gate oxide in nitric oxide (NO) or nitrous oxide (N₂O) seems to have considerably improved the device performance, and peak field-effect-mobility values of up to 50 cm²/V · s have been reported [2]. Recently, a record peak field-effect mobility of 150 cm²/V · s has been achieved after performing the oxidation process in the presence of alumina [3].

In spite of the considerable progress in device performance, reliability is still an important issue. One of the major reliability concerns is the instability of the threshold voltage in SiC MOSFETs under normal operation conditions. This instability is attributed to transient trapping of channel electrons in interface and bulk oxide traps [4]–[6]. Post oxidation annealing in NO has been shown to dramatically reduce this transient trapping, and the short-term reliability of NO-annealed MOS devices looks promising. On the other hand, it is unclear whether thermally grown silicon dioxide layers on SiC can reliably withstand the high electric fields and high temperatures over the desired long operating lifetime.

One of the major concerns for long-time reliability of dielectric layers in high-power devices is time-dependent dielectric breakdown (TDDB). Although the dielectric layer material in the SiC and Si MOS systems is identical (SiO₂), the barrier height between the SiC substrate and SiO₂ is much smaller. The reported conduction-band offset (ΔE_C) values between SiO₂ and 4H-SiC vary between 2.45 [7] and 1.92 eV [8] (0.65–1.18 eV lower than that for SiO₂ on silicon). The conduction-band offset controls the injection of electrons from the semiconductor to the oxide via Fowler–Nordheim tunneling. Thus, 4H-SiC exhibits a much higher tunneling current than in Si under similar applied fields. Indeed, Fowler–Nordheim tunneling has been suggested to contribute to dielectric breakdown, particularly at high electric fields [9]. Another variation is the incorporation of carbon species into the thermally grown SiO₂ layer [10]. Due to these intrinsic differences, in order to accurately assess the lifetime of SiC power MOS devices, it is highly important to find out whether SiO₂ dielectric layers on SiC behave similarly to comparable-thickness SiO₂ layers on Si. The oxide thickness in power devices is much thicker (> 50 nm) than those in modern Si devices in order to sustain the high gate voltages. Consequently, different breakdown mechanisms such as field-driven electron energy and positive charge generation are dominant. A good review of dielectric breakdown mechanisms in thick SiO₂ layers is given in [11].

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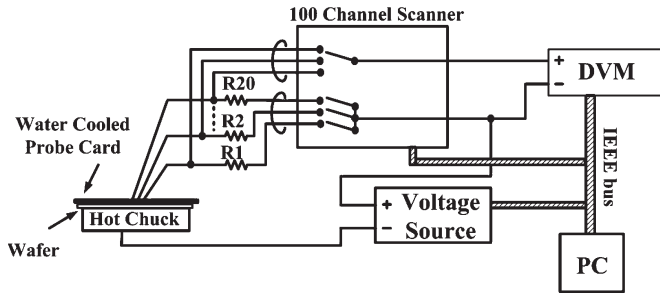


Fig. 1. Schematic diagram of wafer level constant voltage stress system. The system is capable of stressing 20 devices simultaneously at temperatures as high as 400 °C.

While there is extensive research on TDDB of SiO₂ layers on Si, there are only a handful of publications about TDDB of SiO₂ layers on SiC and there is a lack of high-quality statistical data. Maranowski and Cooper [12] presented constant voltage TDDB measurements on steam oxides on 6H-SiC. While their data sets show a large extrinsic failure population, extrapolations from the intrinsic populations predict a mean-time-to-failure (MTTF) of 100 years at 240 °C and 3 MV/cm, with a field acceleration parameter of 2.3 cm/MV. By using only one or two measurements per electric field, Lipkin and Palmour [13] measured time-to-breakdown on dry oxide 6H-SiC samples at 350 °C, estimating an MTTF of 3 h at 3 MV/cm and a field acceleration factor of 2.3 cm/MV. Krishnaswami *et al.* [14] compared constant voltage TDDB measurements of n-type MOS capacitors with the reliability of 4H-SiC DMOSFETs, suggesting that both have extrapolated lifetimes greater than 10¹⁰ h at 3 MV/cm and 175 °C. These capacitor and DMOSFET results, measured at fields greater than 8.5 MV/cm, indicate a field acceleration factor of approximately 4.6 cm/MV. Recently, Matocha *et al.* [15] showed that field acceleration parameter of 4H-SiC MOS devices at temperature of 200 °C abruptly changed at electric fields higher than 8.5 MV/cm. The extrapolated lifetime based on these high electric fields overestimated the normal operating condition lifetime.

In this paper, we present comprehensive TDDB data of 4H-SiC capacitors with a SiO₂ gate insulator collected over a wide range of electric fields and temperatures. By using these experimental data, we propose an accurate model for lifetime assessment of 4H-SiC MOS devices considering electric field and temperature acceleration, area, and failure rate percentile scaling.

II. EXPERIMENTAL SETUP

Silicon carbide MOS capacitors were fabricated on n-type epitaxial layers ($N_D = 10^{16} \text{ cm}^{-3}$) on 4H-SiC Si face wafers at 4° off-axis. These capacitors utilize a thick deposited field oxide and a ~50-nm gate oxide grown by successive N₂O at 1250-°C and NO at 1175-°C thermal oxidations followed by deposition of a Mo gate using sputtering. The capacitors were rectangular in shape with active areas ranging from 25×10^{-8} up to $4 \times 10^{-4} \text{ cm}^2$.

Fig. 1 shows a schematic diagram of a wafer level constant voltage stress system. The capacitors were tested simultane-

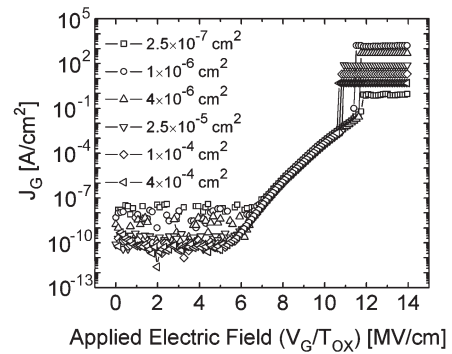


Fig. 2. Current density as a function of the electric field across the oxide of 4H-SiC capacitor with various areas at room temperature.

ously at the wafer level on a specially designed wafer probe station. This station features a water-cooled probe card and test fixture that allows testing up to 400 °C. A water jacket is attached to a ceramic probe card that removes the heat from the top of the card. All test devices are connected through a series resistor to a constant voltage source. The voltage is monitored across each device sequentially to determine if breakdown has occurred without interrupting the applied stress to the device. Once a failure is detected, the stress to that device is disconnected to ensure that the additional current flowing through failed devices does not interfere with adjacent devices under test. The system is capable of testing up to 20 devices simultaneously. In tests where the MTTF was shorter than 2000 s, devices were sequentially characterized to increase the test time resolution.

Initially, we had to verify that the fabrication process is uniform and that there are no edge or perimeter effects. Otherwise, it is impossible to compare results of capacitors of different areas. To accomplish that, we conducted voltage ramp tests on capacitors of all areas. The voltage ramp test followed the JEDEC standard procedure [16].

III. RESULTS AND DISCUSSION

Fig. 2 shows the current density as a function of the electric field across the oxide of 4H-SiC capacitors with various areas at room temperature. The oxide thickness was 43 nm. All the curves are depicted on top of each other, and the breakdown fields are identical, within the error margin. These results confirm that the process is uniform and that we can compare devices of different areas.

In some tests, devices were characterized using a semiconductor parameter analyzer to accurately determine the current as a function of time. Fig. 3 shows the current density as a function of time of $4 \times 10^{-4} \text{ cm}^2$ 4H-SiC capacitors with a 24-nm thick oxide. The temperature was 230 °C, and the applied electric field was 8.5 MV/cm. The current density curves are typical of thick oxide MOS capacitors under a constant voltage stress. The current continuously decreases due to electron trapping until the dielectric layer breaks down and the current abruptly increases. Some of the devices had failed earlier due to defect-induced failures and were removed from the rest of the analysis.

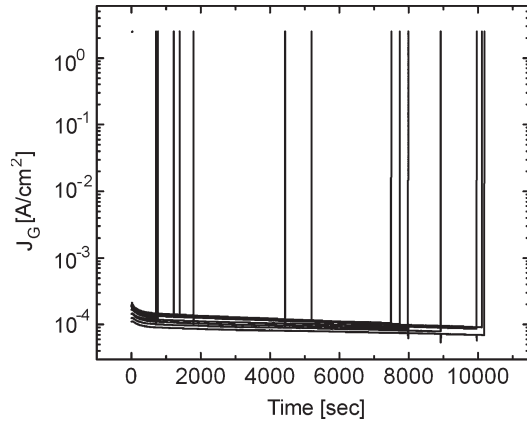


Fig. 3. Current density as a function of time of 4×10^{-4} -cm² 4H-SiC capacitors with a 24-nm-thick oxide. The temperature was 230 °C, and the applied electric field was 8.5 MV/cm.

A. Statistical Distribution and Area Scaling

In the past, dielectric breakdown was characterized using log-normal statistics. As the oxide layers became thinner ($t_{ox} < 5$ nm), it was found that the percolation model [17] and the ensuing Weibull statistics described the TDDB breakdown statistics much better. The benefit of using the percolation model is that it allows area scaling. Equation (1) describes the Weibull relationship

$$\ln(-\ln(1-F)) = -\beta \cdot \ln(\alpha) + \beta \cdot \ln(t) \quad (1)$$

where F is the cumulative failure function, β is the shape parameter (or “Weibull slope”), and α is the scale parameter. The following equations describe the area and percentile scaling rules derived from the percolation model and Weibull statistics [18]:

$$\ln(-\ln(1-F_2)) - \ln(-\ln(1-F_1)) = \ln\left(\frac{A_2}{A_1}\right) \quad (2)$$

$$\frac{t_{BD1}}{t_{BD2}} = \left(\frac{A_2}{A_1}\right)^{1/\beta} \quad (3)$$

$$\frac{t_{BD-F}}{t_{BD-63\%}} \cong \left(\frac{F}{F_{63\%}}\right)^{1/\beta} \quad (4)$$

where t_{BD} is the time of breakdown and A is the oxide area. In Weibull analysis, $t_{63\%}$ is typically used, rather than the MTTF. This is the time at which 63.2% of the population has failed and is called the Weibull characteristic time.

In thick oxides, the percolation model may not be valid. However, Weibull statistics can theoretically describe any “weakest link” mechanism, even in the thick oxide case. Due to the lack of reported Weibull results of thick oxides, we had to first verify that TDDB of thick oxides does fit the Weibull statistics and its area scaling rules. Fig. 4 shows the Weibull distributions of 4H-SiC capacitors with three different areas (squares— 4×10^{-4} cm², circles— 1×10^{-4} cm², and triangles— 25×10^{-6} cm²). The curves are normalized with respect to the 25×10^{-6} -cm² capacitor. The obtained failure distributions, after area scaling, produce a single linear curve. This result

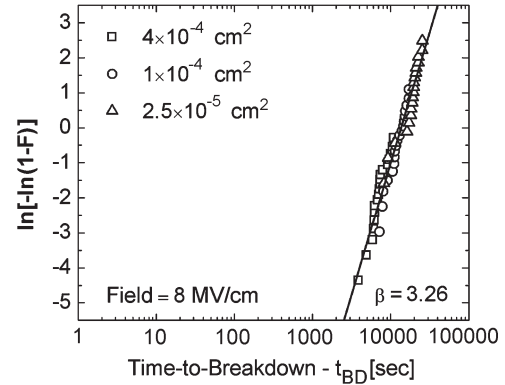


Fig. 4. Weibull distributions of 4H-SiC capacitors with three different areas (4×10^{-4} cm²—squares, 1×10^{-4} cm²—circles, and 2.5×10^{-5} cm²—triangles). The results are normalized with respect to the 2.5×10^{-5} -cm² capacitor area.

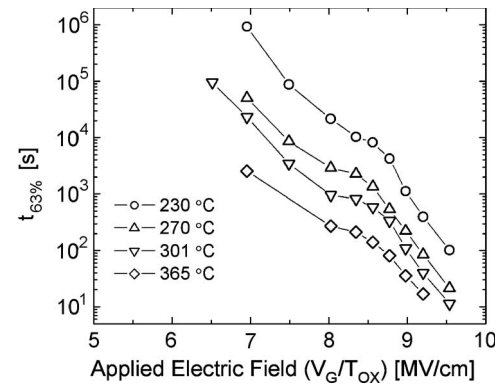


Fig. 5. $t_{63\%}$ as a function of applied electric field of 4×10^{-4} -cm² 4H-SiC capacitors at different temperatures ranging from 230 °C to 365 °C. The gate oxide thickness was 43 nm.

confirms that Weibull statistics and area scaling rules are valid for thick oxide characterization. However, the extracted Weibull slope β is much lower than the prediction of the percolation model when considering the experimentally determined values of β for thinner oxides. The measured β values in this paper varied in the range of 3–10.

Both log-normal (not shown here) and Weibull statistics fit well the breakdown results of these thick oxide devices. For some of the results, log-normal fits better, but mostly Weibull statistic gives a better fit. The advantage of using the Weibull is the ability to perform area scaling. If log-normal statistics had been used, lifetime projection to larger area devices and chips would not be possible.

B. Electric Field Acceleration

We used the thermochemical “ E model,” $t_{63\%} \propto \exp(-\gamma E)$, to model the electric field acceleration [19]. To find the electric field acceleration parameter (γ), $t_{63\%}$ was extracted from the Weibull plots and plotted as a function of the applied electric field. Fig. 5 shows the $t_{63\%}$ as a function of the applied electric field of 4×10^{-4} -cm² 4H-SiC capacitors at different temperatures ranging from 230 °C to 365 °C. The gate oxide thickness was 43 nm. Each point on the graph is extracted from a distribution of between 20

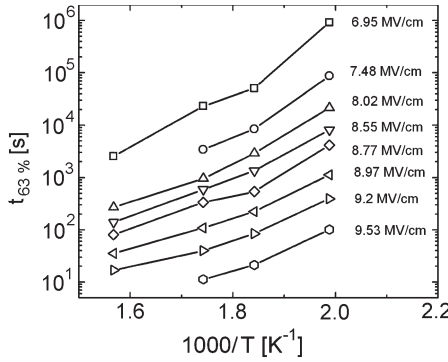


Fig. 6. $t_{63\%}$ as a function of $1000/T$ of 4×10^{-4} -cm² 4H-SiC capacitors for different applied electric field values. The gate oxide thickness was 43 nm.

and 60 failed devices. There are two different regions in the field acceleration plot. At high electric fields, the acceleration parameter is about 4.6 cm/MV, whereas at low electric fields, the acceleration parameter is between 2.07 and 3.22 cm/MV. If we convert γ , in the lower field range, into an effective dipole moment: $P_{eff} = K_B T \times \gamma = 11.3 - 14.0 \text{ e\AA}$, then the data agree extremely well with the value of $\sim 13 \text{ e\AA}$, which is widely reported for silica-based dielectrics at low electric fields [20]. The point where the slope changes in the plot is at about 8.5 MV/cm. It is clear that another failure mechanism may become dominant at high electric fields. Matocha *et al.* [15] demonstrated this phenomenon at a single temperature of 200 °C. The results in Fig. 5 show that this phenomenon is temperature independent in the range of 230 °C–365 °C. Matocha *et al.* suggested that either increased Fowler–Nordheim tunneling or impact ionization was the possible cause for the abrupt change in the field acceleration. Schlund *et al.* [9] have shown that Fowler–Nordheim tunneling causes a similar effect in SiO₂/Si MOS devices at electric fields above 11 MV/cm. Because of the smaller conduction-band offset between SiO₂ and SiC, Fowler–Nordheim is expected to dominate in much smaller fields. Arnold *et al.* [21] have shown that the threshold electric field for impact ionization is thickness dependent and decreases from above 14 MV/cm for SiO₂ layers thinner than 10 nm down to about 8 MV/cm for 50-nm thick oxides. This is about the same electric field where we observe the change in the acceleration parameter.

This result is extremely important for lifetime extrapolation from accelerated tests. One should calculate the electric field acceleration factor from measurements conducted at fields lower than 8.5 MV/cm. Otherwise, the extrapolated value overestimates the real lifetime under normal operating conditions. To compensate for the use of lower electric fields and achieve a practical accelerated test length, the temperature must be accelerated furthermore. Fig. 5 shows that temperatures of up to 365 °C may be used to accelerate TDDB of 4H-SiC capacitors at the wafer level. Higher temperature stressing may also be feasible but has not been tested in this paper.

C. Temperature Acceleration

To find the temperature acceleration parameter, we took the data points from Fig. 5 and plotted $t_{63\%}$ in an Arrhenius plot.

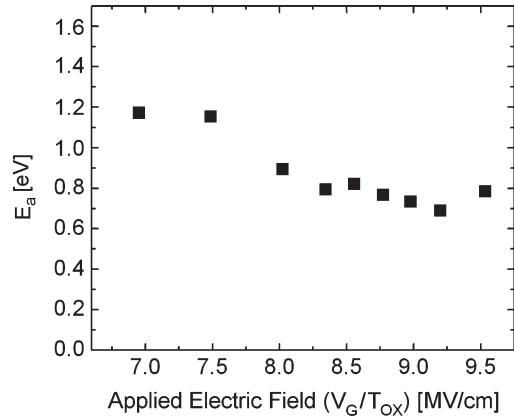


Fig. 7. Activation energy as a function of applied electric field of 4×10^{-4} -cm² 4H-SiC capacitors.

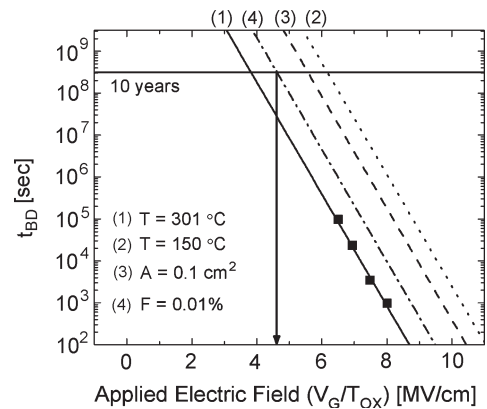


Fig. 8. Prediction of the maximum operating field for 43-nm-thick SiO₂ gate dielectric on top of SiC at low percentile failure rate of 0.01%. The squares represent measured failure data of 4×10^{-4} -cm² 4H-SiC at an accelerated temperature of 301 °C. (1) The solid line is a linear fit of the logarithm of the time-to-breakdown (t_{BD}) as a function of applied electric field. The dotted lines represent the (2) lifetime projection for 150 °C, (3) total gate active area of 0.1 cm^2 , and (4) low percentile failure rate of 0.01%.

Fig. 6 shows $t_{63\%}$ as a function of $1000/T$ of 4×10^{-4} -cm² 4H-SiC capacitors for different applied electric field values. The gate oxide thickness was 43 nm. For all the electric fields, the curves are not perfectly linear and seem to have a slight curvature. This suggests that activation energy is not exactly constant with temperature. However, within acceptable error margins, the temperature acceleration can be described using the Arrhenius model, $t_{BD} \propto \exp(-E_a/kT)$, for a wide range of temperatures and electric fields. Fig. 7 shows the activation energy, extracted from Fig. 6, as a function of the applied electric field of 4×10^{-4} -cm² 4H-SiC capacitors. The extracted activation energy shows a weak dependence on the electric field and is about 1.1 eV for an electric field of 7.0 MV/cm, a result that has been obtained for thick SiO₂ layers on Si in previous studies [22].

D. Lifetime Projection

Fig. 8 shows an example of how to extrapolate the lifetime under usage conditions from the accelerated conditions test results. The projection process takes into consideration the

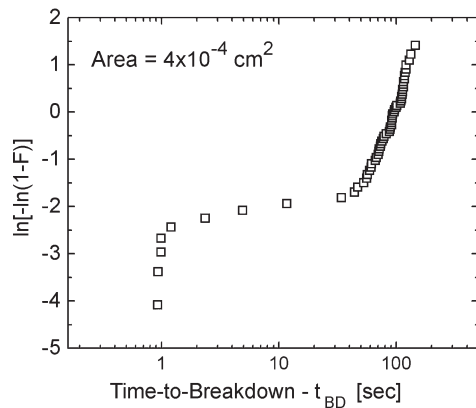


Fig. 9. Uncensored Weibull distribution of 4×10^{-4} -cm² 4H-SiC capacitors at a temperature of 230 °C and under electric field of 8.9 MV/cm.

electric field acceleration, temperature acceleration, area, and percentile scaling. The squares represent the measured failure data of 4×10^{-4} -cm² 4H-SiC at an accelerated temperature of 301 °C. The solid line is a linear fit of the logarithm of the time-to-breakdown (t_{BD}) as a function of applied electric field. The dotted lines represent the lifetime projection for 150 °C, total gate active area of 0.1 cm², and low percentile failure rate of 0.01%. It is projected that the maximum tolerable operating electric field is 4.6 MV/cm for a 43-nm-thick gate dielectric at 150 °C with a ten-year TDDB lifetime. However, if the temperature is increased to 250 °C, the maximum tolerable operating electric field is reduced to 2.9 MV/cm (not shown here).

The temperature acceleration factor was calculated using an activation energy (E_a) of 1 eV, and a Weibull slope (β) value of three was used for the area and percentile scaling factors calculation.

E. Extrinsic Population

The models used in this paper describe only the *intrinsic* failure distribution. These failures are due to the intrinsic material properties of the SiO₂/SiC system. This is the case when the fabrication process is perfect and lacks any preexisting defects. Unfortunately, the present state-of-the-art fabrication processes of SiC power devices are far from perfect. The density of *extrinsic* defects is still unacceptably high. Fig. 9 shows the complete Weibull distribution of 4×10^{-4} -cm² 4H-SiC capacitors at a temperature of 230 °C and an electric field of 8.9 MV/cm. The data set in this figure had a relatively high percentage of extrinsic failures and was thus chosen to demonstrate the problem. The average ratio of extrinsic failures for the 4×10^{-4} -cm² capacitors was about 5%. The extrinsic defect population follows the Poisson distribution with area size. Commercial power devices, such as IGBTs and DMOSFETs, have a much larger active area than the devices we used in this paper. Even if we can find the optimal temperature and field for long operation lifetime safe of intrinsic failures, the effective device lifetime will be dominated by the high density of extrinsic defects. Thus, further work is required to improve the fabrication process of SiC power device.

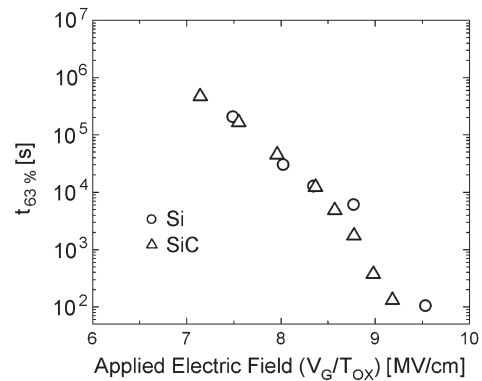


Fig. 10. $t_{63\%}$ as a function of applied electric field of 1×10^{-4} -cm² SiO₂ on Si capacitors (triangles) and SiO₂ on SiC capacitors (circles) at temperature of 230 °C. The gate oxide thicknesses were 50 and 43 nm, respectively.

F. Material Considerations

To study the differences regarding the TDDB failure mechanism between the Si-SiO₂ and the SiC-SiO₂ systems, we compared capacitors fabricated on Si and on SiC substrates with similar oxidation process. Fig. 10 shows the $t_{63\%}$ as a function of applied electric field of 1×10^{-4} -cm² capacitors at temperature of 230 °C. The square symbols represent SiO₂ on Si capacitors, and the circles represent SiO₂ on SiC capacitors. The gate oxide thicknesses were 50 and 43 nm, respectively.

For applied electric fields below 8.5 MV/cm, both Si and SiC devices exhibit similar intrinsic failure times and electric field acceleration. This is not surprising since the oxide is SiO₂ for both cases, and the “E-model” [19], which is used to describe TDDB in thick oxides, predicts that the oxide failure time depends only on the applied electric field, regardless of the oxide thickness. Furthermore, Ogawa *et al.* [23] have shown that while carbon incorporation into SiO₂ films has a major impact on the oxide strength, it has little or no effect on the observed field acceleration parameter— γ .

However, at higher fields, the electric field accelerations of Si and SiC devices are different. In the previous section, we have shown that the failure mechanism changes at fields above 8.5 MV/cm. Increased F-N tunneling and impact ionization were considered as a cause of the change in the field dependence at high electric fields. This may explain the difference between Si and SiC at high electric fields since both phenomena strongly depend on the conduction-band offset (ΔE_C) and the oxide thickness.

Even though Si and SiC devices have similar $t_{63\%}$ values at electric fields below 8.5 MV/cm, there is a difference in their statistical distribution. For a given electric field, the Weibull slope parameter (β) of SiC devices is only half of the Si. These lower β values may be attributed to the high density of preexisting traps in the SiC-SiO₂ system. According to Sune’s percolation theory [17], the gate oxide is modeled as a 3-D array of cells. The size of the cells (a_0^3) represents the “sphere of influence” of a single defect. During the stress period, defects are randomly created in these cells. Breakdown occurs as soon as a column of cells is fully defective inducing a conductive path through the oxide. Sune has shown that the Weibull slope

(β) is proportional to the number of cells in one column— $\beta \propto t_{\text{ox}}/a_0$. At the poor SiC/SiO₂ interface, there is a high density of interface and near-interface preexisting traps, which may be treated as defective cells. If these traps are treated as defective cells, the “effective” number of cells in one column is smaller; thus, β is expected to be smaller.

From these results, it may be concluded that the reliability of SiC–SiO₂ technology due to TDDDB is limited only by the quality of the oxide and the interface, and not by the intrinsic properties of the SiC.

IV. CONCLUSION

TDDDB data are presented for 4H-SiC capacitors with SiO₂ gate insulator collected over a wide range of electric fields and temperatures. Weibull statistics and area scaling rules for thin oxides were found to accurately describe TDDDB of thick oxides, with the exception of a lower β value than theoretically predicted. At low fields, the electric field acceleration parameter is between 2.07 and 3.22 cm/MV. At fields higher than 8.5 MV/cm, the electric field acceleration parameter is about 4.6 cm/MV, indicating a different failure mechanism present under high electric field stress. Thus, lifetime extrapolation must be based on failure data collected below 8.5 MV/cm. It was also demonstrated that temperatures as high as 365 °C can be used to accelerate TDDDB at the wafer level. Higher temperature stressing may be feasible as well but has not been tested in this paper. Temperature acceleration follows the Arrhenius model with activation energy of about 1 eV, similar to thick SiO₂ layers on Si. Further work is required to improve SiC power device processing so that the high density of extrinsic defects is eliminated.

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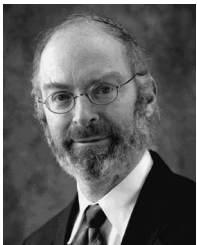


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