Time Dependent Dielectric Wearout (TDDW) Technique for Reliability of Ultrathin Gate Oxides

Yider Wu, Qi Xiang, David Bang, Gerald Lucovsky, and Ming-Ren Lin

***Abstract*— The degradation of ultrathin oxides is measured and characterized by the dual voltage time dependent dielectric wearout (TDDW) technique. Compared to the conventional time-dependent dielectric breakdown (TDDB) technique, a distinct breakdown can be determined at the operating voltage I–t curve. A *noisy*, soft prebreakdown effect occurs for 1.8–2.7 nm ultrathin oxides at earlier stress times. The different stages of wearout of 1.8–2.7 nm oxides are discussed. The wearout of oxide is defined when the gate current reaches a critical current density at the circuit operating voltage. Devices still function after the soft breakdowns occur, but are not functional after the sharp breakdown. However, application of the *E model* to project the dielectric lifetime shows that this is more than 20 y for thermal oxides in the ultrathin regime down to 1.8 nm.**

***Index Terms*—Reliability, TDDB, TDDW, ultrathin oxide.**

I. Introduction

THE aggressively scaling of MOS devices has led to a need to understand the reliability and degradation mechanism for gate oxide thicknesses less than 2 nm. Much research has been devoted to the characterization and understanding of the oxide wearout mechanism, in particular, the development of a functional definition of dielectric breakdown [1]–[4]. It has been shown that the initial continuous increase of the direct tunnel current during constant voltage stress is followed by a complex fluctuation mode, which was define initially as the dielectric breakdown for ultrathin (<2 nm) oxides [2]. However, no significant degradation of g_m or V_t is observed after these so-called soft breakdown effects, and the gate current remains at the same level [1]. It is difficult to use soft breakdown to determine an oxide lifetime because, for many applications, devices remain functional after these soft breakdown events. However, using the conventional TDDB measurement, breakdown is difficult to detect by the following:

1) distinct voltage drop (for constant-current testing);
2) an abrupt current jump (for constant-voltage testing);
3) significant increase in low-voltage leakage current [1].

In this letter, we propose a new technique, time dependent dielectric wearout (TDDW), to qualify reliability in these ultrathin gate oxides. The gate dielectric is stressed at high voltage bias and the gate current is monitored at low voltage bias. The wearout of oxide is defined when the gate current reaches a critical current density at the device operating voltage. This can occur during the wearout process either after soft breakdown events, or after a major current runaway. When either event occurs, the device is determined to be no longer functional. Additionally, it has been found that although the breakdown may not be clearly defined for the high voltage I–t curve, a distinct current jump can easily be identified at the low operation voltage I–t curve. This demonstrates that this dual voltage measurement technique is more effective in detecting the function breakdown point for ultrathin oxides down to 1.8 nm.

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II. Experimental

MOS capacitors were fabricated on ⟨100⟩ p-type Silicon substrates. The 1.8–2.7 nm thick oxides were grown by furnace oxidation at 800 °C in a dilute oxygen ambient. The oxide thickness was determined by analysis of CV data including a quantum effect correction. The poly-silicon was implanted with phosphorus as the gate electrode. The capacitors are isolated by an N^+ area by arsenic and phosphorus implants. An HP4156B precision semiconductor parameter analyzer was programmed for the dual voltage TDDW measurement. The capacitors with an area of 100 μm × 100 μm were continuously stressed at high voltage at an oxide electric field of ∼13 MV/cm in the inversion region. Quantum effects and poly depletion corrections are made by the method described in [5]. The N^+ area surrounding each capacitor is connected to ground to supply electrons. During the constant high voltage stress the gate dielectric leakage current is monitored at low operation voltage as shown in the testing flow chart of Fig. 1. The breakdown criterion is defined as the gate leakage current at low voltage $(I_{g\text{-low}})$ reaches 1 A/cm^2, which is generally believed a leakage limitation for logic applications [6].

III. Results and Discussion

The dual voltage TDDW measurements for 2.3 and 1.8 nm oxides are shown in Fig. 2(a) and (b), respectively. High-voltage I–t curves for both 2.3 and 1.8 nm oxides show a gradual increase in gate current, but it is difficult to identify the *final* hard breakdown at this stress voltage level. In Fig. 2(a), a gradual wearout of 1 V I–t curve can be observed for 2.3 nm oxide in the soft breakdown region, but this slowly wearout only increases the gate current by about an order of magnitude. However, a larger current breakdown with

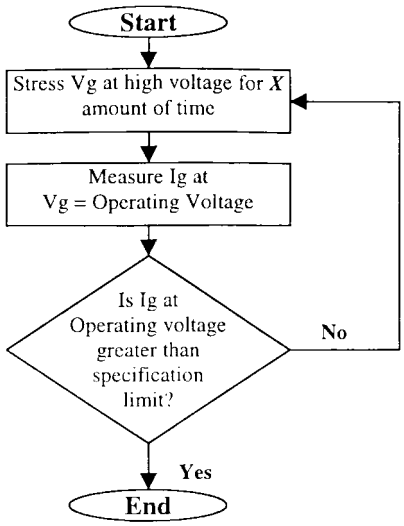

Fig. 1. Testing flow chart of time dependent dielectric wearout (TDDW).

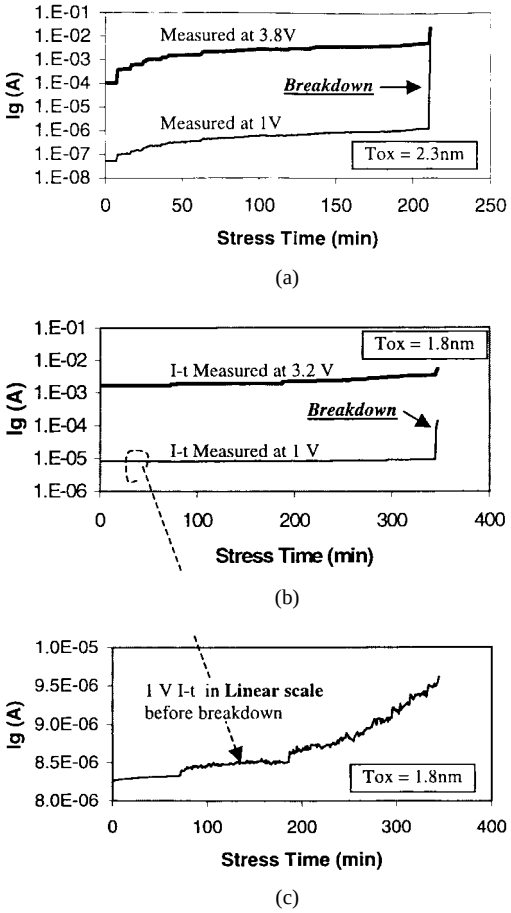

Fig. 2. (a), (b) Dual voltage I_g measured during constant voltage stress for 2.3 and 1.8 nm oxide in a logarithmic scale. The breakdown is hard to identify at the stress voltage, but can be easily identified in the 1 V I–t curve. The capacitor size is 100 μm × 100 μm. (c) The 1 V I–t curve plotted in linear scale before hard breakdown.

increases in I_g of about four orders of magnitude is readily detected at breakdown time. This larger current runaway is harder to detect in the stress voltage I–t curve. In Fig. 2(b), the 1 V I–t curve of 1.8 nm oxide at the stress bias shows

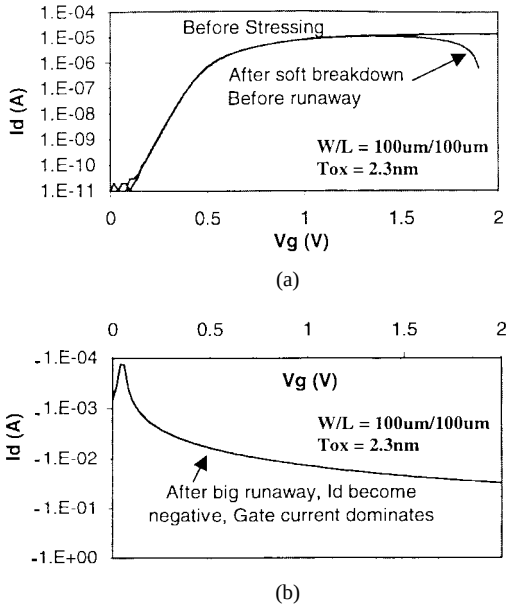

Fig. 3. Subthreshold $I_d - V_g$ characteristics measured for 2.3 nm oxide: (a) before 3.8 V constant current stress and after soft breakdown, and (b) after a large current runaway. Negative I_d current was measured after the large current runaway. The NMOSFET's dimensions are $W/L = 100$ μm/100 μm, and $V_d = 0.05$ V.

almost no difference before and after soft breakdowns on the *logarithmic scale*, and, the same as for the 2.3 nm oxide, the hard breakdown is more easily detected at the operating voltage. Another advantage of this technique is that for some oxides, the wearout (increase in leakage current) may be fast and the gate current reaches the upper limit of acceptable leakage current at the operating voltage before a hard breakdowns occurs. In this case, the time to a particular "oxide leakage current" can also be used as a reliability metric. Fig. 2(c) shows the 1 V I–t curve plotted on a *linear scale* before hard breakdown. We can easily identify the initial continuous increase of the direct tunnel current during the constant voltage stress. Several distinct soft breakdowns occur before the final current runaway or hard breakdown takes place. In our measurements, some 1.8 nm devices show soft breakdown characteristics immediately after stressing starts. This may be due to variations in the oxide quality associated with the initial defect density. However, no matter when the first soft breakdown occurs, a large current runway or hard breakdown is always detected with a strong oxide E-field dependence. For the 1.8 nm oxide, if the stressing voltage is reduced from 3.3 to 3 V, which corresponds to a reduction of the oxide electric field from 13.9 to 13.0 MV/cm, time to hard breakdown is increased from 1 h to 2.6 days. This strong E-field dependence makes it very difficult to define breakdown at a stressing field of less than 13 MV/cm.

Fig. 3 shows the effect of soft breakdown and hard breakdown on device performance for 2.3 nm oxides. After a soft breakdown, the 2.3 nm oxide device still performs well functionally for V_g less than 1.5 V, as shown in Fig. 3(a). The drain current decreases at higher V_g because the current through gate becomes comparable to the channel current and the drain current equal to $I_d = I_s - I_g$ decreases. However,

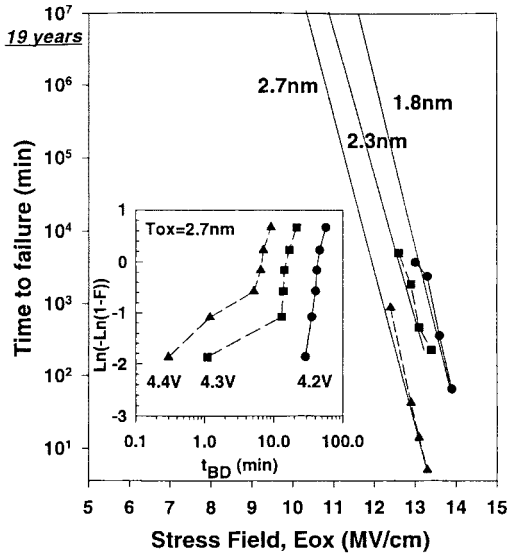

Fig. 4. Empirical linear extrapolation of breakdown lifetime respect to oxide field for 1.8–2.7 nm ultrathin oxides. The inset is the cumulative failure distribution of TDDW for 2.7 nm oxide at different V_g.

after the big runaway or breakdown, a negative drain current is observed because the broken-down oxide can no longer sustain a high E-field and form an inversion layer in the channel and the gate capacitor acts as a resistor, as shown in Fig. 3(b). The device is no longer a functioning transistor after this hard breakdown event.

Fig. 4 shows the E-model extrapolation of time-to-device-failure for 1.8, 2.3, and 2.7 nm oxides [7] and the cumulative failure distribution of TDDW for 2.7 nm oxide with different values of V_g. The Weibull plot of the TDDW distribution shows a similar shape to the conventional TDDB distribution, which then relates the TDDW failure analysis to the conventional hard breakdown in thick oxides. The E model extrapolation of TDDW clearly demonstrates that under extended device operation with $E_{\rm ox} \sim 6$ MV/cm, the oxide lifetime would be very long for ultra thin oxides. The extrapolations indicates that more than a twenty year lifetime can be expected if the E model remains valid. One volt is assumed as the operating voltage for all three ultrathin oxides. The operating voltage may actually be different for different thickness oxides. This long lifetime to breakdown may possibly be due to the reduced energy of the tunneling electrons. Patel *et al.* found that for oxides of thickness greater than 5.2 nm, a threshold electron energy of 1.7 eV in the oxide conduction band is required for breakdown [8]. This energy corresponds to $\sim$4.7 V of $V_{\rm ox}$ or approximately an $E_{\rm ox}$ of 26 MV/cm for a 1.8 nm oxide, which is well above the operating field and stressing fields studied here. If this same threshold energy holds in the ultrathin oxide region, one could perhaps speculate that energetic electrons provided by the high-energy tails in the energy distribution are the possible source for the ultrathin oxide degradation. This would imply that after enough high-energy electrons tunnel through oxide, hard breakdown occurs.

IV. Conclusion

A dual voltage time dependent dielectric wearout (TDDW) technique is proposed as an accurate and efficient method to monitor oxide wearout and breakdown for ultra thin gate oxides. In TDDW tests, the device is stressed at a high voltage and the dielectric leakage current is monitored at a lower operating voltage. This technique demonstrates that the oxide wearout or breakdown can be easily identified from an I–t measurement at the lower operating voltage. It has also been shown that a large current runaway or hard breakdown may still exist for ultra thin oxides down to 1.8 nm although there generally is one or more soft breakdown effects before this current runaway takes place. The device still functions as a transistor after soft breakdown effects but becomes disfunctional after the large current runaway or hard breakdown. E model projection extrapolations indicate a TDDW lifetime of more than 20 years for oxide thickness down to 2.0 nm range for an operating voltage of 1 V.

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