Open access • Journal Article • DOI:10.1109/TPEL.2011.2160358

Time-Domain Design of Digital Compensators for PWM DC-DC Converters

Mor Mordechai Peretz, Sam Ben-Yaakov

Institutions: University of Toronto, Ben-Gurion University of the Negev

Published on: 01 Jan 2012 - IEEE Transactions on Power Electronics (IEEE)

Topics: PID controller, Control theory, Digital control, Control system and Digital signal processing

Time-Domain Design of Digital Compensators for PWM DC-DC Converters

Mor Mordechai Peretz, *Student Member, IEEE*, and Shmuel (Sam) Ben-Yaakov, *Fellow, IEEE*

***Abstract*—A time-domain design method for the digital controller of pulsewidth modulation dc–dc converters was developed. The proposed approach is based on the fact that the closed-loop response of a digitally controlled system is largely determined by the first few samples of the compensator. This concept is used to fit a digital PID template to the desired response. The proposed controller design method is carried out in the time domain and, thus, bypasses errors related to the transformation from the continuous to discrete domain and to discretization. The method was tested by simulations and experimentally. Digital PID controllers for experimental buck- and boost-type converters were designed according to the proposed method and implemented on a TMS320LF2407 DSP core. The measured closed-loop attributes were found to be in good agreement with the design goals. The study was further expanded to investigate the possible realistic closed-loop performance that can be obtained from a system that is controlled by a PID template controller, as well as the stability boundaries of the proposed time-domain controller design approach. The results of the study delineate a normalized map of deviation from the target closed-loop performance goals possible for PID control of switch-mode converters and the areas in which the use of this control law is feasible.**

***Index Terms*—Closed-loop performance, DC-DC power converters, digital control, discrete-time analysis, digital signal processing, PID control, pulse width modulation converters, stability analysis, time-domain analysis, voltage-mode control.**

I. Introduction

TWO general approaches have been described hitherto for the design of digital compensators. The most popular one is the frequency-domain-based method [1]–[4]. Another design scheme proposes the use of MATLAB in a trial-and-error procedure based on pole-zero location in the z-plane [5]. Inasmuchas there is a theoretical relationship between the frequency domain and sampled-data domain (via the various transformation algorithms), a digital compensator operates, in reality, in the sampled-data domain and notions of phase margin, bandwidth and the like are alien to the finite-difference equation algorithm that is implemented on the digital platform. The digital compensator, in fact, handles, in each computational event, only a few samples of error signals and previous results, so basically all the relevant information is short-lived around the sampling instance. One can find an analogy between this situation and the frequency-domain case. In the latter, the relevant feedback information is around the crossover frequency of the loopgain. In the time-domain case, all relevant feedback data are located near each sampling event. That is, in the frequency-domain case, the behavior of the system at frequencies higher or lower than the crossover frequency is to a large extent unimportant. In an analogous way, in the time-domain case, information at times other than close to the sampling instances is irrelevant. In other words, the digital compensator handles only a handful of adjacent data points and is blind to all other samples prior to the sampling event. It follows, then, that the algorithm of the compensator (which is implemented as finite-difference equations) can be based on the short-term time response of the system rather than on the full response, which in many design procedures is derived from the frequency-domain response.

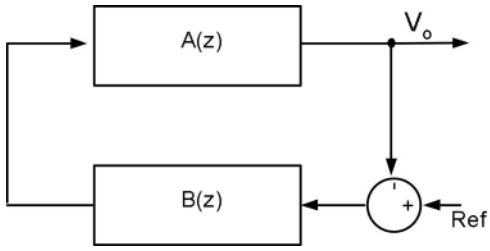

Fig. 1. Basic feedback system.

In this study, we test the previous conjecture by developing and testing a design procedure of a digital compensator for pulsewidth modulation (PWM) dc–dc converters that is based on the short-term time responses of the system. The motivation for this effort stems from the underlying assumption that such digital compensator design methods could provide not only a more natural and streamlined approach, but could lead to better designs and improved performance of the system in closed-loop.

II. Theoretical Consideration

The precursor to the proposed design method is the Ragazzini–Franklin method [6], [7] in which the compensator $B(z)$ is derived from the known open-loop response of the converter $A(z)$ and the desired closed-loop response $A_{\mathrm{CL}}(z)$ [8]. This is demonstrated by considering the basic feedback system

Manuscript received November 29, 2010; revised February 22, 2011 and May 10, 2011; accepted June 6, 2011. Date of current version December 16, 2011. This work was supported by The Israel Science Foundation under Grant 476/08. The work of M. M. Peretz was supported by the Adams Fellowship Program of the Israel Academy of Sciences and Humanities. This paper is an expanded version of a paper that was presented at the IEEE Applied Power Electronics Conference (APEC) 2007, Anaheim, CA. Recommended for publication by Associate Editor P. Mattavelli.

Mor. M. Peretz is with the Laboratory for Power Management and Integrated SMPS, University of Toronto, Toronto, ON, M5A 2N4, Canada (e-mail: morp@ee.bgu.ac.il).

Shmuel (Sam) Ben-Yaakov is with the Power Electronics Laboratory, Department of Electrical and Computer Engineering, Ben-Gurion University of the Negev, Beer-Sheva 84105, Israel (e-mail: sby@ee.bgu.ac.il).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPEL.2011.2160358

of Fig. 1. Since

$$A_{\mathrm{CL}}(z) = \frac{A(z)B(z)}{1 + A(z)B(z)} \tag{1}$$

then

$$B(z)_{\mathrm{ideal}} = \frac{A_{\mathrm{CL}}(z)}{1 - A_{\mathrm{CL}}(z)} \frac{1}{A(z)}. \tag{2}$$

The disadvantage of this method is that it may end up with a high-order compensator (poles and zeros) that would translate into many terms in the compensator's difference equation and hence a long computation time.

Another issue that needs to be resolved is the specification of $A_{\mathrm{CL}}(z)$. In most dc–dc converters, the relevant closed-loop response is the step response rather than the frequency-domain transfer function from which $A_{\mathrm{CL}}(z)$ is normally derived by, say, an s-to-z transformation. Here, we propose to extract $A_{\mathrm{CL}}(z)$ from the time-domain response. The proposed procedure includes two steps. The first is to specify the characteristic equation of $A_{\mathrm{CL}}(z)$ as a function of time-domain parameters. This could be achieved by applying the relationships between time and frequency domain as carried out in [9]. An alternative is to consider a simpler particular case of the typical response of a closed-loop system with phase margin smaller than 50° [6]. The closed-loop response in this case will behave like a second-order system (see [10]). The denominator [characteristic equation, CE(s)] can be described by the conventional template

$$\mathrm{CE}(s) = \frac{s^2}{w_n^2} + \frac{s}{w_n Q} + 1 \tag{3}$$

where ω_n is the angular resonant frequency and Q is the quality factor. For this dynamic system, the rise time t_r as a function of ω_n and the overshoot M_p as a function of the quality factor can be presented by

$$t_r \approx \frac{1.8}{w_n} \tag{4}$$

and

$$M_p = e^{-(\pi/2\mathrm{Q})/\sqrt{1-(1/)4\mathrm{Q}^2}}. \tag{5}$$

That is, the angular resonant frequency and the quality factor can be expressed as

$$w_n \approx \frac{1.8}{t_r} \tag{6}$$

$$Q = -\frac{\sqrt{1 + (\ln(M_p)/\pi)^2}}{2(\ln(M_p)/\pi)}. \tag{7}$$

Equations (6) and (7) provide a way of defining the characteristic equation of $A_{\mathrm{CL}}(s)$ as a function of the desired rise time and overshoot. Once the time-domain response of A_{CL} is set, the denominator of $A_{\mathrm{CL}}(z)$ can be obtained by one of the s-to-z transformations. The second step of the $A_{\mathrm{CL}}(z)$ derivation procedure is to set the numerator such that the closed-loop response is of second order [6], [11]. That is, to obtain the form of $A_{\mathrm{CL}}(z)$ such that the closed-loop system: 1) is casual; 2) has zero error in the steady state to a step perturbation; and 3) has a constant error to a ramp signal. This set of rules is commonly known as "Truxal-rules" [6], [11] and can be obtained by the following constraints

$$A_{\mathrm{CL}}(z)_{|z=\infty} = 0 \tag{8}$$

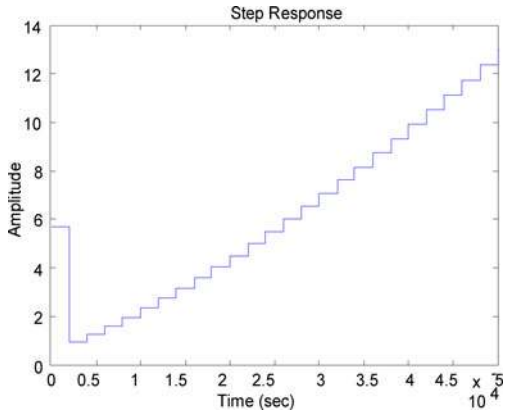

Fig. 2. Step response of "ideal" $B(z)$ compensator.

$$A_{\mathrm{CL}}(z)_{|z=1} = 1 \tag{9}$$

$$\frac{dA_{\mathrm{CL}}(z)}{dz}_{|z=1} = \frac{1}{K_V}. \tag{10}$$

Following the previous procedure, one can derive from (2) the transfer function of the compensator $B(z)$ that will yield the desired rise time t_r and overshoot M_p [i.e., $A_{\mathrm{CL}}(z)$ for a given power stage $A(z)$]. The compensator that will be derived is an "ideal" compensator in the sense that it will reproduce the exact $A_{\mathrm{CL}}(z)$ that was prescribed.

Examination of the step response of a typical $B(z)$ compensator (see Fig. 2) suggests that many functions apart from the ideal $B(z)$ would do the job. The reason is (as pointed out in Section I) that, in reality, the compensator is concerned only with the data points around the sampling instance. Hence, the behavior of the compensator after more than, for instance three steps is irrelevant. This implies that any transfer function that reproduces the first few samples of the step response of the ideal $B(z)$ will also be capable of reproducing the same (or at least close to) $A_{\mathrm{CL}}(z)$. This idea was pursued in the proposed compensator design method.

III. Time-Domain Compensator Design Method

The proposed design procedure follows three basic steps.

1) Derive the ideal compensator from the specified rise time t_r and overshoot M_p based on a knowledge of $A(z)$. Namely, derive $B(z)$ from (2) after the closed-loop response is set by following (3)–(10).
2) Obtain the step response of the ideal $B(z)$.
3) Curve fit a given response of a template compensator to the first few samples of the step response of the ideal compensator.

The small-signal open-loop response of the converter $A(z)$ can be obtained by either theoretical calculations [12], [13], prediction, or by experimental parameters extraction procedure such as system identification [14]–[16].

Among the possible compensator templates for a PWM dc–dc converter, the popular PID is a candidate that has a long proven track record. This was the approach adopted in this analysis.

Applying the matched pole-zero method [6], the continuous template of the PID compensator is

$$\frac{V_c(s)}{V_e(s)} = \frac{(s^2/w_c^2) + (s/w_c Q) + 1}{s} \tag{11}$$

$$\frac{V_c(z)}{V_e(z)} = \frac{a + bz^{-1} + cz^{-2}}{1 - z^{-1}}. \tag{12}$$

It should be noted that (12) is the compensator template that will later be implemented on the digital hardware. For a simulation model, however, the time interval between sampling the output and updating the control signal V_c which, in the case under study, is the duty-cycle command, has to be taken into account. This delay depends on: A/D acquisition time, conversion period, and computational delays. This time interval can be approximated by one sampling cycle delay [1], [5], [8], [17] (i.e., Z^{-1}) and is taken into account when combined with (12)

$$\frac{V_c(z)}{V_e(z)} = \frac{a + bz^{-1} + cz^{-2}}{z - 1}. \tag{13}$$

This relationship can be described by the difference equation

$$V_c[n+1] = V_c[n] + aV_e[n] + bV_e[n-1] + cV_e[n-2]. \tag{14}$$

The three coefficients (*a, b, c*) can now be calculated by indexing and solving (14) for the first three samples

$$\begin{bmatrix} V_c[0] - 0 \\ V_c[1] - V_c[0] \\ V_c[2] - V_c[1] \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 1 & 1 & 0 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{15}$$

where the indices 0, 1, 2 stand for the first three samples (after one cycle delay) of the output of the ideal $B(z)$ compensator for the step input: 1, 1, 1.

IV. Time-Domain Compensator Design Example

The following example illustrates the proposed digital compensator design method. Assuming:

A buck type converter power stage described by

$$A(s) = \frac{3.333 \times 10^8}{s^2 + 2500s + 1.333 \times 10^8}. \tag{16}$$

Required closed-loop time-domain performance

$$t_r = 100\,\mu\text{s}; \quad M_p = 10\%.$$

The first step is to transform $A(s)$ into $A(z)$ by the Zero-Order Hold (ZOH)transformation

$$A(z) = \frac{0.06548z + 0.06459}{z^2 - 1.908z + 0.96}. \tag{17}$$

It should be noted that ZOH transformation provides good approximation of the sampled-data system to account for the sample-and-hold action of the A/D converter (A/DC) and for symmetrical PWM case [12]. For a more accurate model of the open-loop system for the general case of PWM, one may consider the model refinement presented in [12] or the direct modeling method in [13].

Next, t_r and M_p are used to calculate ω_n and Q [by (6) and (7)] that define the characteristic equation of $A_{\text{CL}}(s)$ (3)

$$\text{CE}(s) = 3.086 \cdot 10^{-9}\, s^2 + 1.1 \cdot 10^{-3}\, s + 1. \tag{18}$$

To properly specify the closed-loop response in the discrete domain $A_{\text{CL}}(z)$, we follow the rules presented in Section II. The discrete equivalent of (18) is extracted by applying one of the s-to-z transformations (here, we used the normalized matched *p–z* [6], [18])

$$\text{CE}(z) = z^2 - 1.401z + 0.4933. \tag{19}$$

The reason that either of the transformation methods is applicable at this point is that, as opposed to (17), the form or value of CE(z) is not restricted by the design and, therefore, does not need to be further approximated to any sampled signal. That is, since the entire compensation operation (from error to control) is obtained in the discrete domain, the mathematical manipulations to extract $B(z)$ are free from practical constraints as long as the conditions set by (6) and (7) are satisfied. In the event that the parameters of CE(z) change, either due to changes in specifications or to different transformation, the values of the derived compensator will vary accordingly.

The second step in the derivation of $A_{\text{CL}}(z)$ is to extract the numerator. For proper design, the order of the numerator must not exceed the order of CE(z) [6], [18], so $A_{\text{CL}}(z)$ will be of the form

$$A_{\text{CL}}(z) = \frac{n_0 z^2 + n_1\, z + n_2}{z^2 + d_1\, z + d_2} = \frac{n_0 z^2 + n_1 z + n_2}{z^2 - 1.401\, z + 0.4933} \tag{20}$$

where d_1 and d_2 are the denominator coefficients extracted in (19), and n_0, n_1, n_2 are the numerator coefficients to be found by applying (8) to (10).

Equation (8) forces causality by dictating that the system will not contain zeros at infinity. Setting n_0 to zero will satisfy this term.

In order to extract n_1 and n_2, we apply (9) and (10) to (20) and solve

$$\begin{aligned} &n_1 + n_2 = 1 + d_1 + d_2 \\ &n_1 + 2n_2 = (1 + d_1 + d_2) \\ &\qquad\quad + (1 + d_1 + 2d_2) \end{aligned} \quad \rightarrow \quad \begin{aligned} n_1 &= 0.5067 \\ n_2 &= -0.4148. \end{aligned} \tag{21}$$

The resulting discrete closed-loop transfer function $A_{\text{CL}}(z)$ is

$$A_{\text{CL}}(z) = \frac{0.5067\, z - 0.4148}{z^2 - 1.401\, z + 0.4933}. \tag{22}$$

$A(z)$ and $A_{\text{CL}}(z)$ are then used to express $B(z)$ (2)

$$B(z) = \frac{0.5044\, z^3 - 1.375\, z^2 + 1.271\, z - 0.3958}{0.06548\, z^3 - 0.1249\, z^2 + 0.05945\, z}. \tag{23}$$

This expression can now be used to obtain the step response of the ideal compensator. This could conveniently be done with MATLAB using the function: [Vc_data] = step(B). Since $B(z)$ was already assigned to the step function as a discrete function, the time steps are adjusted automatically to the sampling period (20 μs) [17].

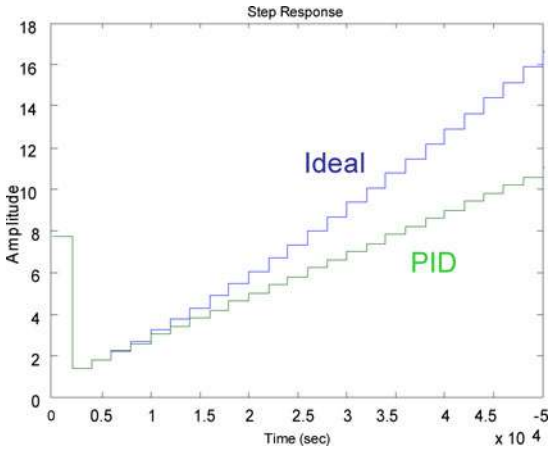

Fig. 3. Step responses of the "ideal" compensator and proposed PID compensator.

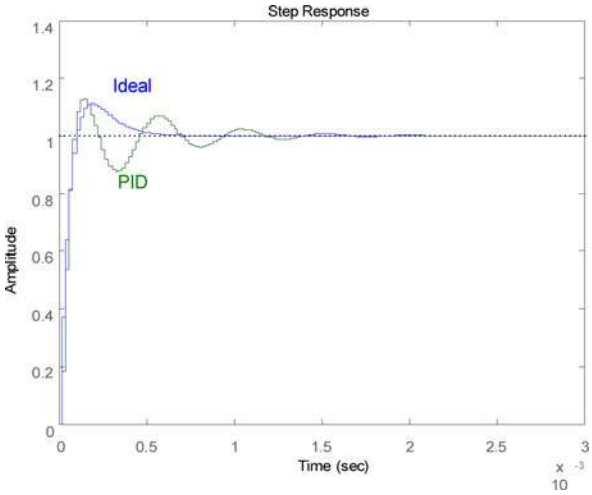

Fig. 4. Closed-loop step responses of a system controlled by the "ideal" compensator and proposed PID compensator.

Once the vector of response (Vc_data) is evaluated, the PID coefficients (a, b, c) are calculated by applying (15) to be

$$a = 3.4; \quad b = -6.15; \quad c = 2.93.$$

Comparison of the step response of the proposed compensator with that of the ideal compensator shows (see Fig. 3) a good fit for the first three steps, which was the objective of the fitting. More importantly, Fig. 4 shows that the system's closed-loop step response with the proposed compensator is very close to the response of the ideal compensator around the area of interference ($t = 0$) and reproduces the closed-loop attributes that were set.

An interesting insight into the performance of the proposed compensator can be obtained by reconstructing the responses in the frequency domain (see Fig. 5). It can be observed that $1/B(z)_{\mathrm{PID}}$ crosses $A(z)$ at nearly the same frequency as $1/B(z)_{\mathrm{ideal}}$. However, the phase of the PID network is slightly lagging with reference to the ideal compensator. This implies that for a given set of design specifications, systems that are controlled by either the ideal compensator or by PID will have the

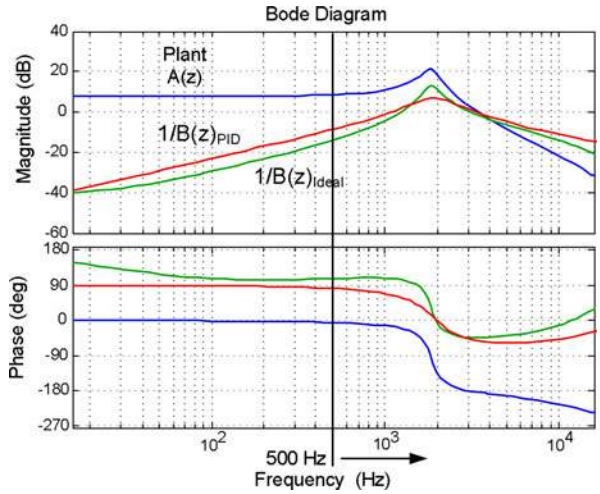

Fig. 5. Frequency response of converter (control-to-output TF), "ideal" compensator and PID compensator.

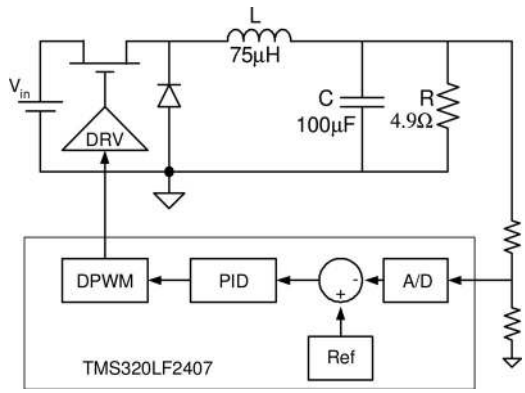

Fig. 6. Experimental setup.

same bandwidth, but with modest phase margin when controlled by PID. In time-domain terms, both systems will produce the same overshoot and respond with the same rise time; however the PID controlled system will decay somewhat slower, yet still at an acceptable rate, as can be observed in Fig. 4.

Notwithstanding the excellent match between time responses the ideal and PID compensators around the sampling instance, the two responses deviate as a function of time (see Fig. 3). The main reason for this is the lower order of the PID compensator as compared to the ideal compensator, which enables the ideal compensator to neutralize the plant's behavior, and thus, to generate any desired response. The implications of this deviation and the limitation that it poses on proposed time-domain compensator design are discussed in the Appendix.

V. Experimental Verification

The experimental converter (see Fig. 6) was controlled by a TMS320F2407 DSP evaluation board (Texas instruments) [19], [20]. The input voltage was 15 V, output voltage 5 V, sensing gain 1/7, and switching frequency and sampling rate were 50 kHz. The A/D resolution was 6.4 mV/bit, the resolution of the Digital Pluse Width Modulator (DPWM)was 9 bits . Following

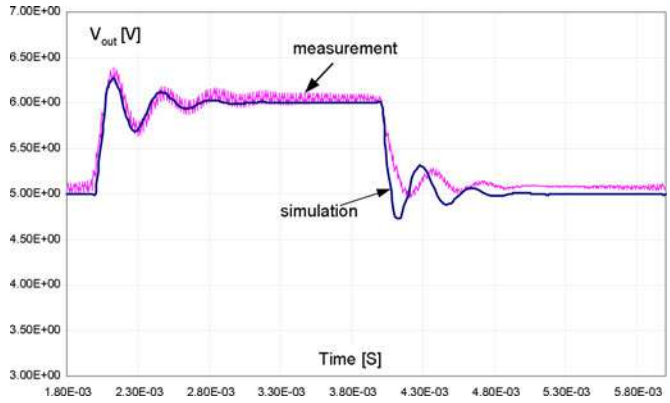

Fig. 7. Comparison of simulated and experimental output voltage step responses to a step change in reference voltage (5 to 6 V). Faster compensator $(B(z)_F)$.

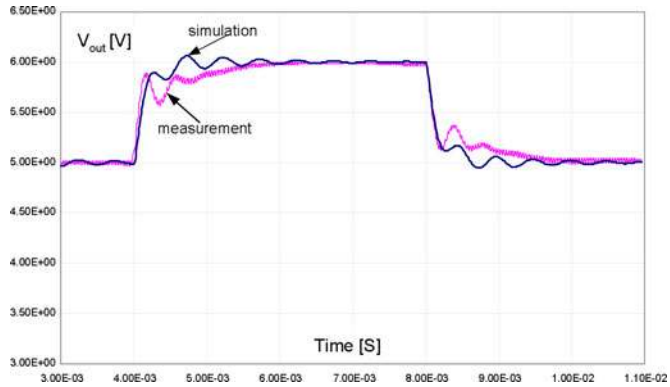

Fig. 8. Comparison of simulated and experimental output voltage step responses to a step change in reference voltage (5 to 6 V). Slower compensator $(B(z)_S)$.

the proposed design procedure, the digital PID compensator was derived for two cases. A relatively slow response $B_S(z)$: $t_r = 500\ \mu$s; $M_p = 0$; and a faster response $B_F(z)$: $t_r = 100\ \mu$s; $M_p = 10\%$. The compensators were found to be

$$B(z)_S = \frac{1.52 - 2.81z^{-1} + 1.38z^{-2}}{1 - z^{-1}} \tag{24}$$

and

$$B(z)_F = \frac{3.4 - 6.15z^{-1} + 2.93z^{-2}}{1 - z^{-1}}. \tag{25}$$

Figs. 7 and 8 show good agreement between the experimental closed-loop responses and simulation results. The discrepancy between the responses is probably due to inaccurate estimation of the system plant; this was remedied by applying system identification as detailed in the following section. The objective of the experiment was to change the reference values from 110 to 130 (digital values), such that the output voltage is changed from 5 to 6 V, respectively. The responses to a load step changing from 1 to 1.5 A are given in Figs. 9 and 10. The loop gain of the system with "Fast" compensator design was measured with an HP4395 A network analyzer (resolution measurement of 10 Hz). The measured loopgain (see Fig. 11) was found to

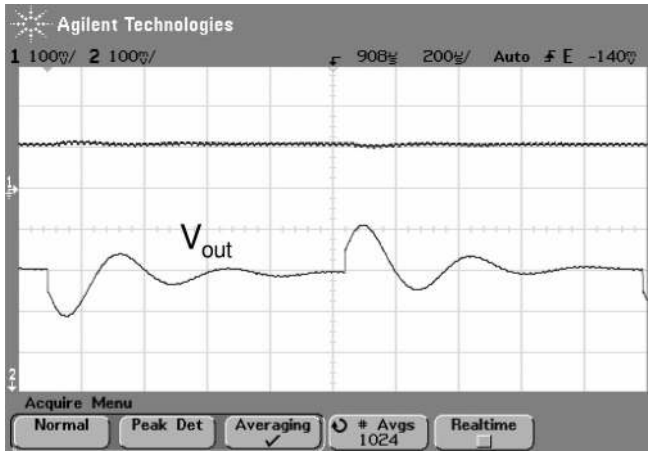

Fig. 9. Experimental result for output voltage response to a load step (1 to 1.5 A). Closed-loop buck converter with faster compensator $(B(z)_F)$. $V_{\rm out}$ (100 mV/div). Horizontal scale (200 μs/div).

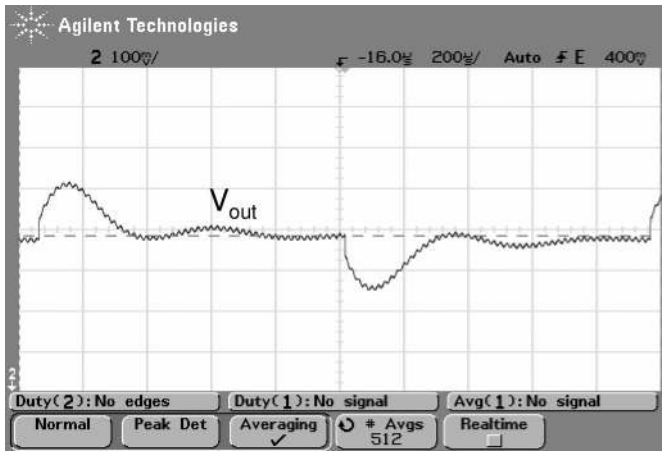

Fig. 10. Experimental result for output voltage response to a load step (1 to 1.5 A). Closed-loop buck converter with slower compensator $(B(z)_S)$. $V_{\rm out}$ (100 mV/div). Horizontal scale (200 μs/div).

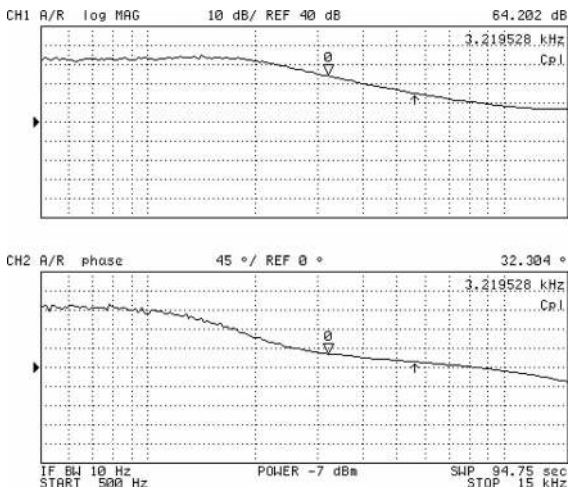

Fig. 11. Experimental loopgain of system controlled by faster compensator $(B(z)_S)$.

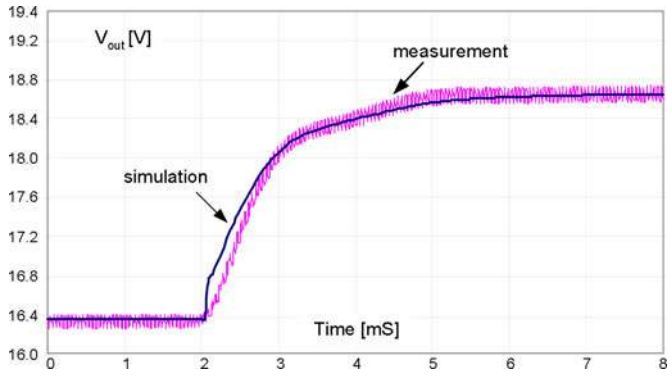

Fig. 12. Comparison of simulated and experimental closed-loop boost converter responses to a step change in reference voltage (16.4 to 18.7 V). Controller design was based on a time-domain identification of the plant's response. Slower compensator ($B(z)_{\mathrm{Boost\_}S}$).

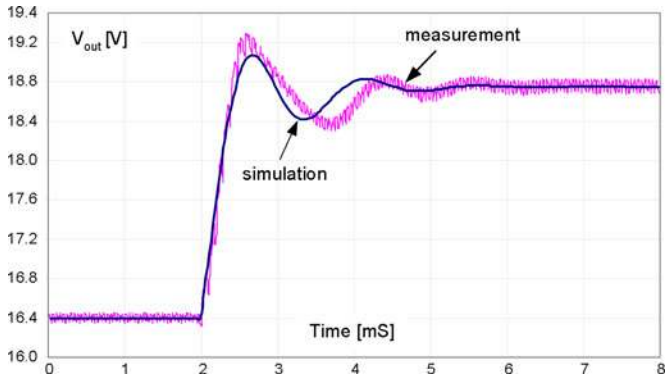

Fig. 13. Comparison of simulated and experimental closed-loop boost converter responses to a step change in reference voltage (16.4 to 18.7 V). Controller design was according to the proposed methods and the system's response was based on a time-domain identification of the plant's response.

match the one predicted by simulation at intersection point of $A(z)$ and $1/B(z)$ in Fig. 5). The measured bandwidth and phase margin were 3.5 kHz and 35°, respectively.

The proposed compensator design method can be further refined by applying an experimentally derived small-signal model of the converter open-loop response rather than using the theoretical response that may not include all parasitic effects. This was accomplished by applying the time-domain-based parametric identification procedure detailed in [16]. The results of the refined procedure are shown for a boost type converter with the following parameters: input voltage: 10 V; output voltage: 16 V; sensing gain: 1/7; load current: 0.3 A/DC; switching frequency and sampling rate: 20 kHz. The nominal value of the converter's components were: $L = 300$ μH ($R_L = 350$ mΩ), $C = 100$ μF (ESR = 300 mΩ), switch-ON resistance (IRF640): 0.18 Ω, diode forward voltage (1N5822): 0.5 V. The identified discrete-time boost transfer function $A_{\mathrm{Boost\_ID}}(z)$ was found to be

$$A_{\mathrm{Boost\_ID}}(z) = \frac{0.2526z - 0.197}{z^2 - 1.866z + 0.8844}. \tag{26}$$

The slow closed-loop response PID controller ($t_r = 1000$ μS, $M_p = 0$) was evaluated to be

$$B(z)_{\mathrm{Boost\_}S} = \frac{1.91 - 3.379z^{-1} + 1.528z^{-2}}{1 - z^{-1}} \tag{27}$$

and the faster response PID ($t_r = 400$ μS, $M_p = 10\%$) was found to be

$$B(z)_{\mathrm{Boost\_}F} = \frac{2.287 - 3.122z^{-1} + 1.03z^{-2}}{1 - z^{-1}}. \tag{28}$$

The excellent agreement between the experimental closed-loop step responses and simulation results for both controller cases are depicted in Figs. 12 and 13. The reference values were changed from 350 to 400 (digital values), to cause a change from 16.3 to 18.7 V at the output.

VI. Conclusion

The proposed design procedure of a digital compensator for a PWM dc–dc converter follows the concept, developed in this study, of the local behavior of discrete compensators. The basic idea behind this concept is that the system's closed-loop response is largely determined by the first few samples of the step response of the compensator. Based on this conjecture, many templates can be fitted to approximate the "ideal" compensator (as defined in Section II). In this study, we explored the possibility of applying a PID template to the proposed design procedure. The proposed compensator derivation method relies entirely on the discrete domain and does not involve any transformation-related approximations. Thus, the extracted compensator can be considered more accurate in the sense that it produces the exact design specifications that were prescribed.

The proposed parameter extraction procedure (15) is based on matching the PID compensator's step response to the ideal compensator's step response in the vicinity of the sampling instance, i.e., at the sampling instance and two previous samples. This procedure was implemented by solving a set of three linear equations with three unknowns (the PID coefficients a, b, c). The main advantages of this method are that the derived PID compensator will reproduce the system's rise time and overshoot that were prescribed, which was the objective of the fitting, and that this extraction procedure is very simple and can be easily implemented on a digital platform.

One may consider a different selection of points of matching the responses of the ideal compensator and PID compensator for the parameters extraction procedure that may make the PID and ideal compensators' responses similar in a different region or in a larger time scale. It was found by a series of experiments that were carried out that a different selection of the matching points deteriorates the PID capability to generate the required rise time and overshoot and may increase the complexity of the coefficients extraction procedure.

Simulation and experimental results confirm the viability of the proposed design method. The proposed method is, thus, a good candidate for an alternative approach to the design of digital compensators for PWM dc–dc converters.

The (continuous) average model of the converter can be used to model the open-loop small-signal response of the converter $A(z)$. When transformed to the z-domain, it will be corrupted by the inherent inaccuracy of the transformation as well as numerical errors such as truncation errors. An alternative way to obtain $A(z)$ is by a system identification procedure that applies experimental data. In doing so, all parasitic effects (e.g., R_L, ESR, $R_{\mathrm{ds\_on}}$, $V_{D\,\mathrm{on}}$, etc.), quantization gains (A/D and DPWM) and delays are taken into account and do not need to be estimated. Hence, it should lead to more accurate controller design.

A comparison of PID controllers derived from average models and from identified models of the converter, supports the previous assumption. It was found that the PID compensators extracted by identification have better dynamic performance in closed loop, especially in slow rise time (i.e., low BW) cases and the resulting closed-loop responses were found to be emulated more accurately by simulation.

A comprehensive comparison of the ideal compensator and proposed PID template compensator was carried out. As detailed in the Appendix there are practical limitations in terms of rise time and overshoot where a PID compensator is capable of reproducing the desired closed-loop response. These limitations are due to the fixed template of the proposed compensator. That is, the PID controller will generate an "ideal"-like behavior in cases where the required compensation scheme is close to PID. A map was derived for the realistically possible regions of rise time and overshoot combinations for a given converter and PID controller template.

Notwithstanding the limitations of the PID template, within the valid range of closed-loop specifications, it was made worthwhile to avoid the practical drawbacks of the "ideal" compensator such as complicated compensator implementation and long computational intervals.

It should be noted that the somewhat limited range of the extracted compensator in faithfully reproducing the target performance goals is related to the controller template that is selected and not to the proposed coefficients extraction method. The procedure can be similarly applied to other compensation schemes, which may have different ranges of operation. The discussion on the limitations of the PID compensator was expanded due to the popularity and versatility of this structure and is applicable to any PID, regardless of how its coefficients have been obtained.

It should also be noted that due to the relatively low switching frequency (and sampling rate) used in the experimental part of this study (Section VI), the absolute closed-loop attributes of the results may seem modest when compared to other published digital control examples where the switching frequency is in the region of hundreds of kilohertz to over 1 MHz. Obviously, the proper criterion for evaluating the performance is the ratio of the crossover frequency to switching frequency which, in the present design, is measured to be 1:12.5, which is comparable to the majority of digital feedback designs that have been carried out by other methods [1], [21]–[23].

The potential advantages of the proposed method are the fact that it is carried out in the time domain (and hence bypasses some of the errors due to the s-to-z transformation) and that it is does not involve a trial-and-error procedure.

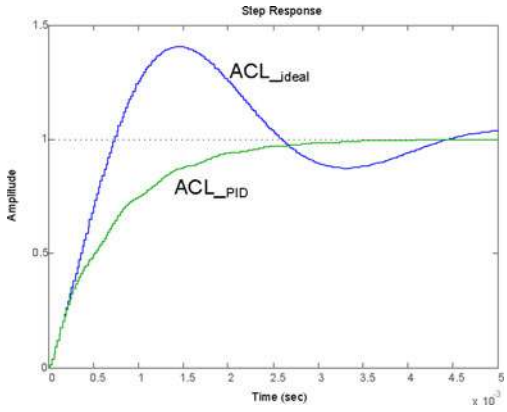

Fig. A1. Step responses of closed-loop system compensated with ideal controller and derived compensator, for closed-loop specifications of slow rise time and high overshoot.

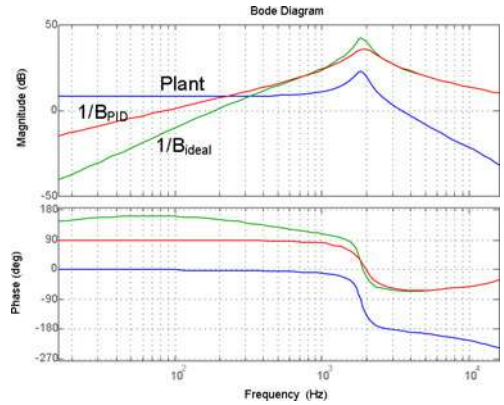

Fig. A2. Frequency responses of the plant, ideal controller and derived compensator for closed-loop specifications of slow rise time and high overshoot.

APPENDIX

DIFFERENCES BETWEEN DERIVED AND "IDEAL" COMPENSATORS AND PERFORMANCE IN CLOSED-LOOP

The compensators that were derived by the method proposed in this study were shown to have a transient response that is similar to the ideal compensators for the first few samples. However, over time there is a growing deviation between the two responses as seen, for example, in Fig. 3. It stands to reason that this deviation will have an effect on the performance of the derived PID controller and may cause large errors and possible instability in some cases. Furthermore, one would expect that the limited poles and zeros of the PID compensator will fail to produce a behavior which is not consistent with PID capabilities. For example, consider the case in which the closed-loop response is set to be a very small bandwidth but a relatively high overshoot. This requirement can be easily met by the ideal compensator since it generates a closed-loop response on demand with as many poles and zeros as required. However, due to the fixed template of the PID controller, it will fail to match this requirement [see Figs. A1 and A2)].

In this Appendix, the difference between the derived compensator and the ideal controller has been explored, the relationship

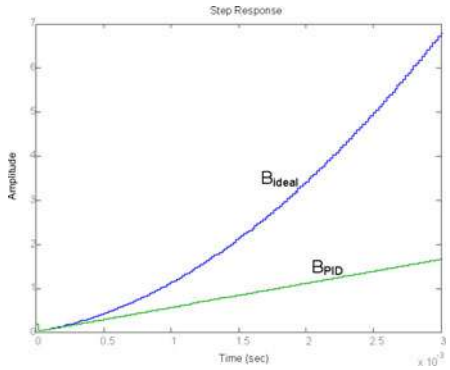

Fig. A3. Step responses of ideal controller and derived compensator to achieve a closed-loop specifications of slow rise time and high overshoot of Figs. A1 and A2.

of the deviation between responses and the compensator coefficients has been derived, the conditions in which the extracted compensator will meet the performance goals in closed-loop have been extracted and the regions of rise time and overshoot combinations that are realistically possible for a given converter (plant) and PID controller template have been delineated.

In the following derivations, it is assumed that the step responses of the ideal and extracted compensators are identical for the first two samples. It is further assumed that the desired compensator template is known and is given by (13) and that the desired closed-loop system that is generated by the previous procedure $A_{\mathrm{CL\_des}}$ is stable and is of the form (20)–(22)

$$A_{\mathrm{CL\_des}}(z) = \frac{n_1\, z + n_2}{z^2 + d_1\, z + d_2}. \tag{29}$$

According to Fig. A3, the difference between the ideal compensator B_{ID} and the extracted compensator B_{PID} can be approximated in discrete form to

$$B_{\mathrm{ID}}(z) - B_{\mathrm{PID}}(z) = \frac{k}{(z-1)\left[z-(d_2-n_2)\right]}\frac{1}{z}. \tag{30}$$

That is, zero deviation for the first two samples and a difference growing with time by a factor of $k/[1-(d_2-n_2)]$.

Based on (30), $B_{\mathrm{ID}}/\,B_{\mathrm{PID}}$ is found to be

$$\frac{B_{\mathrm{ID}}(z)}{B_{\mathrm{PID}}(z)} = \frac{k}{(z-1)\left[z-(d_2-n_2)\right]}\frac{1}{z}\frac{1}{B_{\mathrm{PID}}(z)} + 1. \tag{31}$$

Given the desired compensator template of (13)

$$B_{\mathrm{PID}}(z) = \frac{a + bz^{-1} + cz^{-2}}{1 - z^{-1}} \tag{32}$$

where a, b, and c are the compensator coefficients extracted by the previous procedure.

The ratio $B_{\mathrm{PID}}/B_{\mathrm{ID}}$ can be written as a function of the compensator's coefficients

$$\frac{B_{\mathrm{PID}}(z)}{B_{\mathrm{ID}}(z)} \equiv G(z) = 1 - \frac{k}{(az^2+bz+c)\left[z-(d_2-n_2)\right]+k} \equiv 1 + H(z). \tag{33}$$

That is, as the difference factor $k/[1-(d_2-n_2)]$ becomes smaller, the response of the extracted compensator will be closer to the response of the ideal compensator.

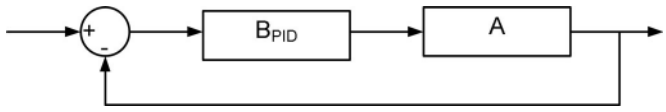

Fig. A4. Block diagram representation of the closed-loop system controlled by the desired compensator.

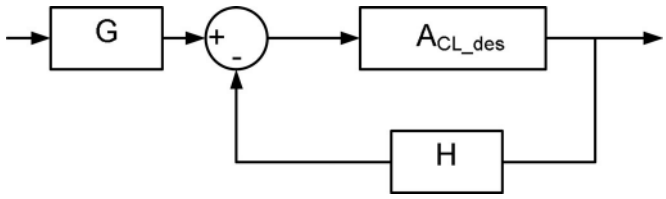

Fig. A5. Block diagram representation of the closed-loop system of Fig. A4 by means of the desired closed-loop response.

The closed-loop transfer function of the system that is controlled by $B_{\mathrm{PID}}(z)$, $A_{\mathrm{CL\_PID}}(z)$, (see Fig. A4) can be expressed as

$$A_{\mathrm{CL\_PID}}(z) = \frac{A(z)B_{\mathrm{PID}}(z)}{1 + A(z)B_{\mathrm{PID}}(z)} \tag{34}$$

where $A(z)$ is the discrete representation of the converter's open-loop transfer function.

Substituting $[1 + H(z)]B_{\mathrm{ID}}$(z) into B_{PID}(z), $A_{\mathrm{CL\_PID}}(z)$ can be expressed by (see Fig. A5)

$$A_{\mathrm{CL\_PID}}(z) = G(z)\frac{A_{\mathrm{CL\_des}}(z)}{1 + A_{\mathrm{CL\_des}}(z)H(z)} \tag{35}$$

or

$$A_{\mathrm{CL\_PID}}(z) = \frac{A_{\mathrm{CL\_des}}(z)\left(az^2+bz+c\right)\left[z-(d_2-n_2)\right]}{(az^2+bz+c)\left[z-(d_2-n_2)\right]+k\left(1-A_{\mathrm{CL\_des}}(z)\right)} \tag{36}$$

Given the coefficients of the compensator $\{a, b, c\}$ and of the desired closed loop $\{d_2, n_2\}$, one may explore the boundaries of the difference factor "k" for stability of $A_{\mathrm{CL\_PID}}(z)$. An examination of the stability of the characteristic equation of (36) based on the full description of $A_{\mathrm{CL\_des}}$ is quite complex due to the high order of the resultant polynomial equation and the number of parameters. We simplify the closed-loop system, for the purposes of analytical derivation, by approximation it to a first-order system. This is done based on the assumption that the frequency range that is of interest is below the closed-loop bandwidth. The simplified $A_{\mathrm{CL\_des}}$ is of the form

$$A_{\mathrm{CL\_des}}(z) \xrightarrow{\approx} \frac{1 - e^{\omega_0 T_s}}{z - e^{\omega_0 T_s}} \tag{37}$$

where ω_0 is the bandwidth of $A_{\mathrm{CL\_des}}$ and T_s is the sampling period.

The characteristic equation of the approximated system is found to be

$$\mathrm{Char\_Eq\_}A_{\mathrm{CL\_PID}}(z) = [z-(d_2-n_2)](z-e^{\omega_0 T_s})(az^2+bz+c) + k(z-1). \tag{38}$$

The boundaries of "k" for stability of $A_{\mathrm{CL\_PID}}(z)$ were delineated in this study by the Jury stability test [18] which is a

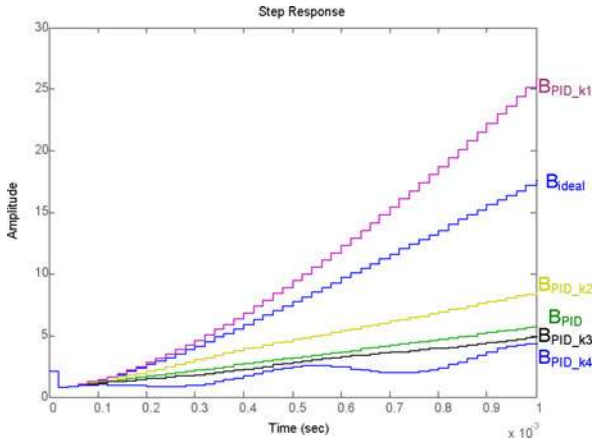

Fig. A6. Step responses of ideal controller, derived compensator extracted by the proposed procedure, and additional responses within the allowable boundaries of "*k*."

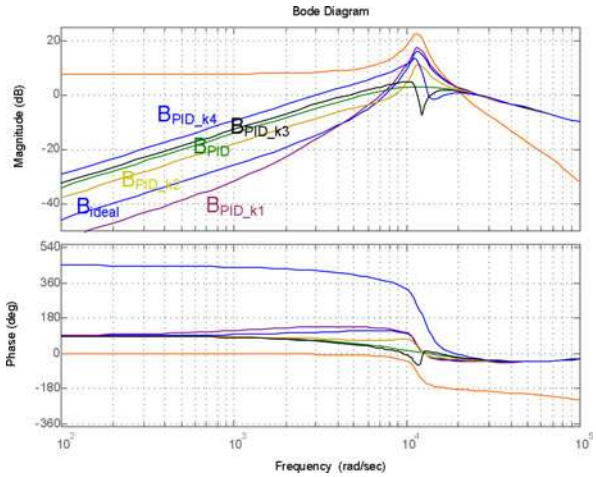

Fig. A7. Frequency responses of converter, ideal controller, derived compensator extracted by the proposed procedure, and additional responses within allowable boundaries of "*k*."

modification of the Routh–Horowitz stability test for the discrete domain. Fig. A6 shows the step responses of the ideal compensator and of the compensator extracted in Section IV, as well as the step responses of some possible extracted compensators that are allowed within the boundary of "k" values. It should be noted and it can be observed in Fig. A6 that the first few samples of all the responses take identical values, while for the rest of the responses there can be a significant difference.

An interesting insight into the performance of the system can be obtained from the frequency response of Fig. A7. It shows that the $1/B(z)$ of all compensators cross $A(z)$ (the converter's open-loop transfer function) at the same frequency which will result in a similar rise time in the time domain; however, the behavior of the transfer functions before the intersection point is quite different which will cause a different overshoot and settling behavior for each system. For example, at the intersection frequency of $1/B_{\mathrm{PID}\_k4}$ with A (see Fig. A7), the phase margin is around zero degrees which indicates that the system is operating at the boundary of stability.

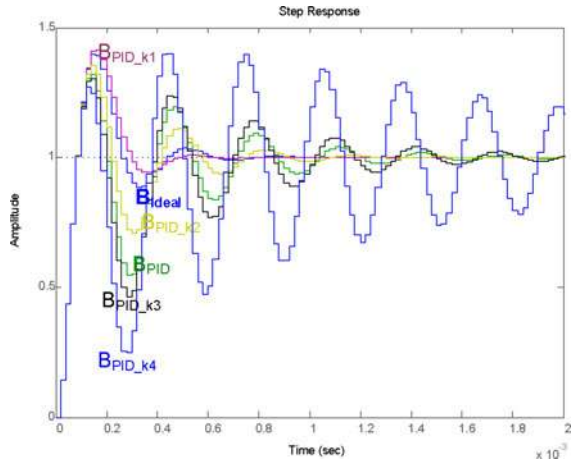

Fig. A8. Step responses of closed-loop system compensated by ideal controller and derived compensator, and other compensators that are within the allowable boundaries of "k".

The corresponding closed-loop step responses are depicted in Fig. A8. As predicted, all responses share a similar response for the first few samples. However, the rest of the responses deviate from the desired response considerably.

The resultant boundaries or constraints on "k" set the maximum deviation in the step response of the derived compensator that is allowed from the step response of the ideal compensator, which keeps the closed-loop system stable. These provide an alternative method (which can be integrated into computerized code) for validating the compensator extraction procedure.

Notwithstanding the theoretical importance of the stability boundaries of the proposed compensator design procedure, this by itself adds only limited information on the practical limitations and the realistic closed-loop specifications (rise time and overshoot) that may be obtained for a given converter and PID template compensator. A more significant contribution on this subject would be to map out the resulting rise time and overshoot combinations that are obtained from a system that is controlled by the proposed compensator as a function of the deviation (or difference) from the ideal (desired) response. This will enable one to learn the practical limitations and realistic performance goals that can be expected from a controller and the amount of error that is expected if these limitations are exceeded. To this end, we run a set of 1380 MATLAB simulations for different settings of rise times and overshoots in which, for each simulation, the error value and time-domain parameters of the system (rise time, overshoot, and settling time) were measured. Fig. A9 shows a 3-D (normalized) map of the closed-loop rise time ($\omega_n t_r$, normalized to the bandwidth of the converter) and overshoot (%) combinations that were obtained from a system controlled by the proposed compensator and the amount of difference that is expected from the ideal compensator.

The interpretation of the results depicted in Fig. A9 is that while some closed-loop performance goals are met such as 15% overshoot and relatively fast rise time (0.5) (normalized values) as indicated by circle "a" in Fig. A9, other sets of goals (circles b, and c, Fig. A9) are impractical to realize with a PID template. For example, it is intuitively obvious that cases of very fast rise

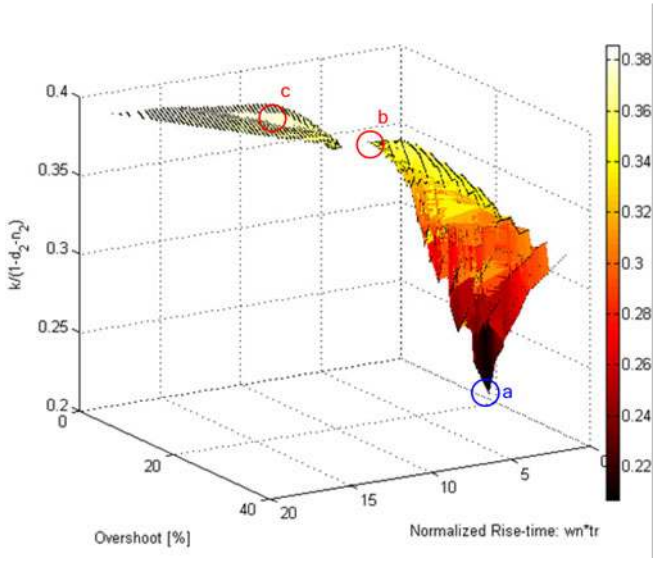

Fig. A9. 3-D map of possible closed-loop attributes (rise time and overshoot) that were obtained from a system controlled by the proposed PID compensator and the difference from desired specifications. Rise time was normalized to the converter's bandwidth, overshoot [%] and difference factor defined as $k/[1-(d_2-n_2)]$.

time and no overshoot, or slow rise time with high overshoot are not practical to obtain with a fixed low-order compensator.

The implication of the results is that for a power stage compensated by PID scheme (regardless of the method it was extracted) there exists regions for bandwidth—phase margin or rise time overshoot combinations that are not feasible. For example, the case of narrow bandwidth (slow rise time) and small phase margin (high overshoot) [see see Figs. A1 and A2)] cannot be achieved by PID compensator due to high-order lag network that is required at low frequency, before the plant's double pole.

REFERENCES

[1] V. Yousefzadeh, W. Narisi, Z. Popovic, and D. Maksimovic, "A digitally controlled DC/DC converter for an RF power amplifier," *IEEE Trans. Power Electron.*, vol. 21, no. 1, pp. 164–172, Jan. 2006.

[2] J. Morroni, R. Zane, and D. Maksimovic, "Design and implementation of an adaptive tuning system based on desired phase margin for digitally controlled DC–DC converters," *IEEE Trans. Power Electron.*, vol. 24, no. 2, pp. 559–564, Feb. 2009.

[3] Y.-F. Liu, E. Meyer, and X. Liu, "Recent developments in digital control strategies for DC/DC switching power converters," *IEEE Trans.Power Electron.*, vol. 24, no. 11, pp. 2567–2577, Nov. 2009.

[4] M. Shirazi, R. Zane, and D. Maksimovic, "An autotuning digital controller for DC–DC power converters based on online frequency-response measurement," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2578–2588, Nov. 2009.

[5] O. Garcia, A. de Castro, A. Soto, J. A. Oliver, J. A. Cobos, and J. Cezon, "Digital control for power supply of a transmitter with variable reference," in *Proc. IEEE Appl. Power Electron. Conf.*, Dallas, TX, 2006, pp. 1411–1416.

[6] G. F. Franklin, J. D. Powell, and A. Emami-Naeini, *Feedback Control of Dynamic Systems*, 5th ed. Upper Saddle River, NJ: Pearson Prentice Hall, 2006.

[7] J. R. Ragazzini and G. F. Franklin, *Sampled-Data Control Systems*. New York: McGraw-Hill, 1958.

[8] B. Miao, R. Zane, and D. Maksimovic, "Automated digital controller design for switching converters," in *Proc. IEEE Power Electron. Spec. Conf.*, Recife, Brazil, 2005, pp. 2729–2735.

[9] M. M. Peretz and S. Ben-Yaakov, "Revisiting the closed-loop response of PWM converter controlled by voltage feedback," in *Proc. IEEE Appl. Power Electron. Conf.*, Austin, TX, 2008, pp. 58–64.

[10] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Norwell, MA: Kluwer, 2000.

[11] J. G. Truxal, *Automatic Feedback Control Systems Synthesis*. New York: McGraw-Hill, 1955.

[12] D. M. Van de Sype, K. De Gussemé, F. M. L. L. De Belie, A. P. Van den Bossche, and J. A. Melkebeek, "Small-signal z-domain analysis of digitally controlled converters," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 470–478, Mar. 2006.

[13] D. Maksimovic and R. Zane, "Small-signal discrete-time modeling of digitally controlled PWM converters," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2552–2556, Nov. 2007.

[14] M. Shirazi, J. Morroni, A. Dolgov, R. Zane, and D. Maksimovic, "Integration of frequency response measurement capabilities in digital controllers for DC-DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2524–2535, Sep. 2008.

[15] B. Miao, R. Zane, and D. Maksimovic, "System identification of power converters with digital control through cross-correlation methods," *IEEE Trans. Power Electron.*, vol. 20, no. 5, pp. 1093–1099, Sep. 2005.

[16] M. M. Peretz and S. Ben-Yaakov, "Time domain identification of PWM converters for digital controllers design," in *Proc. IEEE Power Electron. Spec. Conf.*, Orlando, FL, Jun. 2007, pp. 809–813.

[17] Mathworks. (Apr. 2010). "Matlab control toolbox user guide," [Online]. Available: www.mathworks.com

[18] B. C. Kuo, *Automatic Control Systems*, 7th ed. Englewood Cliffs, NJ: Prentice Hall, 1995.

[19] Texas instruments. (2010, Apr.). "TMS320LF2407 A DSP controller" data sheet, [Online]. Doc No. sprs145 k.pdf. Available: www.ti.com.

[20] Texas instruments. (2010, Apr.). "TMS320LF/LC240xA DSP Controllers Reference Guide." [Online]. Doc No. spru357c.pdf. Available: www.ti.com.

[21] A. V. Peterchev, X. Jinwen, and S. R. Sanders, "Architecture and IC implementation of a digital VRM controller," *IEEE Trans. Power Electron.*, vol. 18, no. 1–2, pp. 356–364, Jan. 2003.

[22] B. J. Patella, A. Prodic, A. Zirger, and D. Maksimovic, "High-frequency digital PWM controller IC for DC-DC converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1–2, pp. 438–446, Jan. 2003.

[23] S. Saggini, P. Mattavelli, M. Ghioni, and M. Redaelli, "Mixed-signal voltage-mode control for DC-DC converters with inherent analog derivative action," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1485–1493, May 2008.

Shmuel (Sam) Ben-Yaakov (M'87–SM'08–F'10) received the B.Sc. degree in electrical engineering from the Technion, Haifa, Israel, in 1961, and the M.S. and Ph.D. degrees in engineering from the University of California, Los Angeles, CA, in 1967 and 1970, respectively.

He is currently an Emeritus Professor with the Department of Electrical and Computer Engineering, Ben-Gurion University of the Negev (BGU), Beer-Sheva, Israel, where he served as Chairman from 1985–1989. He serves as the Head of the Power Electronics Group of BGU. His current research interests include power electronics, circuits and systems, electronic instrumentation and engineering education.

Mor Mordechai Peretz (S'05) was born in Beer-Sheva, Israel, in 1979. He received the B.Tech. degree in electrical engineering in 2003 from the Negev Academic College of Engineering, Beer-Sheva, and the M.Sc. and Ph.D. degree in electrical and computer engineering from Ben-Gurion University of the Negev, Beer-Sheva, in 2005 and 2010, respectively.

He is currently a Postdoctoral Fellow at the Laboratory for Power Management and Integrated SMPS, University of Toronto, Canada. His research interests include digital control, switch-mode dc–dc converters, modeling and computer aided design, lighting systems and ballasts, nonlinear magnetics, and resonant power conversion systems.