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TIME-INTERLEAVED DELTA-SIGMA MODULATOR FOR WIDEBAND DIGITAL GHz TRANSMITTERS DESIGN AND SDR APPLICATIONS

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Abstract—This paper presents a development of a wideband delta-sigma modulator for fully digital GHz transmitters. The fully digital RF transmitter is developed as a promising solution for software defined radio (SDR) terminals and applications. The fully digital transmitter consists of a delta-sigma modulator, a high-speed multiplexer and a switching-mode power amplifier. The speed limitation of delta-sigma modulator is the main limitation to increase the signal bandwidth in fully digital transmitters. In this paper, the bandwidth of the fully digital transmitter is increased 8 times using parallel processing time-interleaved architecture, while maintaining the same signal quality. This architecture was implemented on FPGA and tested for different standards (WiMAX and LTE) with a signal bandwidth up to 8 MHz. The concept was assessed in terms of SNDR by using a differential logic analyzer at the output of FPGA, and the SNDR was found to be around 60 dB.

1. INTRODUCTION

The concept of a fully digital transmitter indicates many promising performances for modern radio systems; one of which is its applicability to software defined radio (SDR) architecture. The advantage of SDR-based radio systems is the possibility of switching between the settings of different standards through software programming without any changes in the radio's hardware. This can be accomplished by utilizing components that can be easily reconfigured. However, the design of reconfigurable and programmable components is not easy, especially

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for analog components, such as a frequency up-converter. A fully digital transmitter would provide a programmable radio, even for radio frequencies.

Another advantage of fully digital transmitters is the suitability for utilizing advanced, highly efficient transmitting techniques. One of the major problems of modern communication systems is the efficiency degradation due to the signal's peak-to-average power ratio (PAPR). Recent wireless communication standards apply advanced schemes, such as OFDM to provide higher throughput; however, these modulations generate signals with higher PAPRs. For example, WiMAX with OFDM modulation can easily have a PAPR of more than 12 dB. For a signal with 12 dB PAPR, the maximum theoretical efficiency of a class A power amplifier (PA) decreases from 50% to less than 15%, and the efficiency of a class B PA decreases from 78.5% to less than 20% [1].

In advanced transmitting methods using different techniques, such as Envelope Elimination and Restoration (EER) or Polar transmitters [2–5], delta-sigma based transmitters [6–10] and Linear amplification with Nonlinear Components (LINC) [11, 12], the envelope-varying signal is converted to a signal with a constant envelope. Consequently, it is possible to use highly efficient saturated linear amplifiers or switching-mode power amplifiers (SMPAs) such as classes D, E or F [13].

Fully digital transmitter architecture, by using an oversampled delta-sigma modulator, changes the signal to a bi-level constant envelope signal. This digital bi-level signal is ideal for use in conjunction with SMPAs. Therefore, fully digital transmitters not only satisfy the demand for reprogrammable, reconfigurable, multi-band, multi-standard transmitters for SDR, but also allow for the application of a delta-sigma modulation technique and, consequently, the use of power efficient SMPAs, while ensuring good linearity of the system.

The major limitation of delta-sigma modulators is the requirement for very high processing speed. Indeed, the main idea in delta-sigma modulation is producing quantized data, usually in a bi-level format, by oversampling the signal much higher than the Nyquist frequency. At the same time, the quantization noise is shaped and pushed to the outside of the useful band of the signal [14].

The performance of the delta-sigma modulator is proportional to the oversampling ratio (OSR), where a higher OSR gives better performance. Typically, OSRs of 100 to 200 result in high-quality output signals. For example, an application with a signal bandwidth of 5 MHz and an OSR of 200 requires a delta-sigma modulator with a clock speed of 1 GHz, which is difficult to achieve in practice.

In this paper, parallel processing techniques are applied to address and alleviate the limitation of the modulator clock speed for scenarios with wideband input signals. In these techniques, multiple modulators work in parallel simultaneously, performing as a single modulator working at a much higher speed.

This paper follows and extends the initial concept of all-digital transmitter presented in [10]; however, the work being presented herein reports the full development of an integrated demonstrator. It includes the novel design and implementation of a suitable time-interleaved parallel delta-sigma modulator that enables a significant broadening of the modulator signal bandwidth to handle current and emerging communication signals, while keeping a relatively good signal-to-noise-and-distortion ratio (SNDR) of about 60 dB. To the best knowledge of the authors, the achieved performance results presented in this paper are the best reported in the open literature in terms of signal bandwidth, carrier frequency and signal quality.

This paper is organized as follows: In Section 2, the architecture of fully digital transmitters is described, and its main building blocks are presented in more detail. Parallel processing and time-interleaved design of the delta-sigma modulator is explained in Section 3. Section 4 demonstrates the implementation of the proposed fully digital transmitter. Finally, the measurements results, in terms of SNDR, for WiMAX and LTE wireless standards with different bandwidths are reported in Section 4.

2. FULLY DIGITAL TRANSMITTER ARCHITECTURE

Figure 1 shows a block diagram of the fully digital transmitter architecture. It consists of three main sections:

1. Control and signal processing unit,
2. Signal shaping (delta-sigma modulator) and digital up-converter unit,
3. RF digital amplification and bandpass filtering stage.

The control and signal processing unit manages the transmitter settings. In the signal shaping and digital up-converter unit, an oversampled delta-sigma modulator is used to produce a bi-level signal. For digital up-conversion, a 4×1 high-speed multiplexer is used.

The RF digital amplification and filtering stage is composed of an SMPA and integrated filter. The SMPA amplifies the binary RF signal to the desired power. The use of highly efficient SMPAs with constant envelope signals should, in principle, maximize the

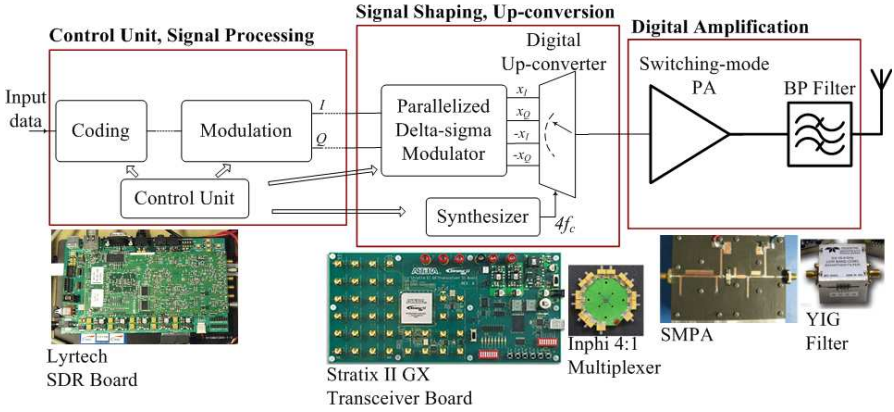

Figure 1. Fully digital transmitter block diagram.

transmitter's efficiency [13]. However, due to the presence of delta-sigma modulator, a huge amount of quantization noise exists at the output of the PA which should be removed by using a bandpass filter at the output of transmitter.

The scope of this paper is focused on the development and improvement of the signal shaping and digital up-conversion unit.

3. DELTA-SIGMA MODULATOR AS A SIGNAL SHAPER

The concept of delta-sigma modulation consists of oversampling and quantizing the data. The use of a feedback loop in the modulator results in different transfer functions for the used signal and the quantization noise. The quantization noise is shaped outside the useful band, and its value is decreased significantly in the band of interest. Fig. 2 shows a first-order delta-sigma modulator and its input and output signals in both time and frequency domains. The z-transform of the output signal can be related to the input as follows:

$$Y(z) = z^{-1}X(z) + \left(1 - z^{-1}\right)E(z) \tag{1}$$

where the signal transfer function (STF) and the noise transfer function (NTF) of the modulator are, respectively:

$$STF(z) = z^{-1} \tag{2}$$

$$NTF(z) = \left(1 - z^{-1}\right) \tag{3}$$

The NTF corresponds to a high-pass filter that shapes the quantization noise outside of the useful band of the signal. Generally,

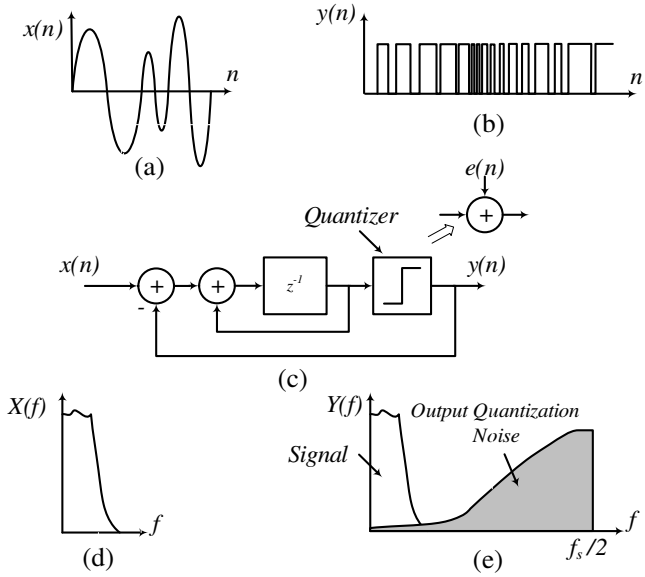

Figure 2. Delta-sigma modulator.

due to stability issues and speed limitation, second- or third-order modulators with oversampling ratio (OSR) in the range of 100 to 200 are often used [14].

4. HIGH-SPEED MULTIPLEXER AS FREQUENCY UP-CONVERTER

In the proposed fully digital transmitter, a multiplexer is used for IQ modulation and up-conversion. In this approach, a single 4×1 multiplexer is used to up-convert the digital baseband signal to RF frequency [10, 15, 16]. The inputs of the multiplexer must be derived by x_I, x_Q, $-x_I$ and $-x_Q$, where x_I and x_Q represent the in-phase and quadrature-phase of the delta-sigma modulator's outputs. The carrier frequency of the up-converter's output depends on the multiplexer's clock; whereas, the carrier frequency of f_c requires the clock speed of $4f_c$ for the multiplexer. Fig. 3 presents this up-converter.

The clock speed of a delta-sigma modulator is defined by the signal bandwidth and the modulator's OSR. To achieve good performance and acceptable signal quality and to ease filtering at the output of the SMPA, a large OSR and consequently a very high speed modulator clock is required. The modulator will usually be implemented in

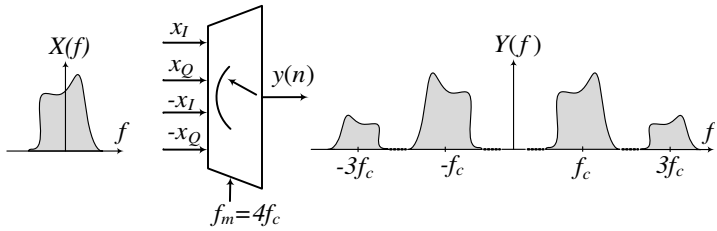

Figure 3. High-speed 4×1 multiplexer working as a frequency up-converter.

FPGA, where the maximum FPGA clock is limited; hence, the delta-sigma modulator is confined to relatively narrowband signals. To address this limitation, the concept of parallel signal processing is adopted herein to achieve a wider bandwidth without sacrificing the signal quality at the output of the modulator, while using a relatively lower speed FPGA.

5. TIME-INTERLEAVED PARALLEL DELTA-SIGMA MODULATOR

5.1. Parallel Delta-sigma Modulation Techniques

Parallel processing techniques alleviate the high-speed clock requirements of the delta-sigma modulator. However, greater complexity results, and more resources are needed in the implementation of delta-sigma modulators.

In one approach, a bank of filters is used to break the signal to a couple of smaller bandwidth signals. Therefore, the speed required by the modulator for each of these sub-bands is significantly reduced [17]. The technique is usually called frequency band decomposition (FBD).

In another technique, the Hadamard transformer is used to decompose the input spectrum to several sub-bands, where each sub-band needs lower speed for modulation [18]. After modulation, the Hadamard transformer is again applied, and the modulated sub-bands are mixed, and the modulated form of the input signal is reconstructed at the output. This is also known as the parallel delta-sigma (ΠDS) approach.

In a different technique, by using M interconnected modulators working in parallel, the processing speed of the modulator can be reduced M times [19–21]. This last technique, which has been adopted in this work to extend the supported bandwidth, is called the time-interleaved delta-sigma (TIDS) approach. TIDS application

has mostly been limited to analog-to-digital and digital-to-analog converters [19–21]. However, the idea can benefit the performance of the DSM in terms of bandwidth improvement and suitability for FPGA implementation. To drive the SMPA in fully digital transmitter, the signal should be in bit-stream format and among different parallel processing techniques; time-interleaving is the only one that can be adopted for fully digital transmitter architecture.

In this work, this concept has been adopted, for the first time, to design and implement a parallel time-interleaved delta-sigma based transmitter, in order to extend the signal bandwidth by about an order of magnitude without any need to increase the processing frequency of the FPGA. The designed transmitter will be tested with a modulated signal of bandwidth of 8 MHz with processing frequency of 100 MHz to validate the concept. This is 8 times lower than the required processing frequency of 800 MHz, when using conventional delta-sigma modulator with OSR equals to 100.

5.2. Time-interleaved Delta-sigma Modulation

Providing that the transfer function of a discrete system is $H(z)$, the application of a polyphase multi-rate technique gives an equivalent circuit for $H(z)$, as shown in Fig. 4 [19].

The $\overline{H}(z)$ in Fig. 4 is an $M \times M$ transfer function and is given by

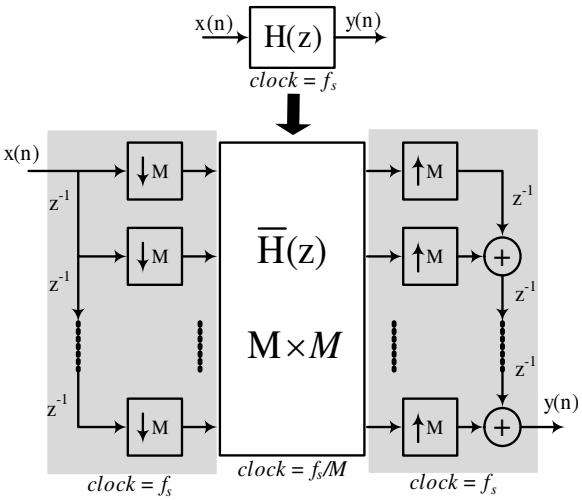

Figure 4. Time-interleaved delta-sigma modulator.

the following equation [19–21]:

$$\overline{H}(z) = \begin{bmatrix} E_0(z) & E_1(z) & \dots & E_{M-1}(z) \\ z^{-1}E_{M-1}(z) & E_0(z) & \dots & E_{M-2}(z) \\ z^{-1}E_{M-2}(z) & z^{-1}E_{M-1}(z) & \dots & E_{M-3}(z) \\ \vdots & \vdots & \ddots & \vdots \\ z^{-1}E_1(z) & z^{-1}E_2(z) & \dots & E_0(z) \end{bmatrix} \tag{4}$$

where $E_l(z)$ is the polyphase component of $H(z)$. If $h(n)$ and $e_l(n)$ are the time domain presentations of $H(z)$ and $E_l(z)$, the relation between $H(z)$ and $E_l(z)$ is as follows:

$$e_l(n) = h(Mn + l) \qquad 0 \le l \le M - 1 \tag{5}$$

$$H(z) = \sum_{l=0}^{M-1} z^{-l} E_l\left(z^M\right) \tag{6}$$

The M-time down-samplers at the input of $\overline{H}(z)$ indicate that $\overline{H}(z)$, while providing the same performance, would work at a speed M times lower than its equivalent $H(z)$. At the output of $\overline{H}(z)$, a series of M-time up-samplers and delays should be used to construct the output signal.

Most of the delta-sigma modulators are composed of integrators. Here, as an example, $E_l(z)$ is found for a simple integrator and then $\overline{H}(z)$ is easily constructed. Fig. 5(a) shows a second-order delta-sigma modulator that is made of two blocks: A and B. The transfer function for block A is:

$$H_1(z) = \frac{1}{1 - z^{-l}} \tag{7}$$

Using the general equation in (6), the transfer function in (7) can be rewritten for a two-channel interleaved modulator as follows:

$$H_1(z) = \sum_{l=0}^{1} z^{-l} E_l\left(z^2\right) = E_0\left(z^2\right) + z^{-l} E_1\left(z^2\right) = \frac{1}{1 - z^{-l}} = \frac{1 + z^{-l}}{1 - z^{-2}}$$
$$= \frac{1}{1 - z^{-2}} + z^{-l}\frac{1}{1 - z^{-2}} \tag{8}$$

.

Based on (8), $E_l(z^{-1})$ is defined as follows:

$$E_0(z^{-1}) = E_1(z^{-1}) = \frac{1}{1 - z^{-l}} \tag{9}$$

.

Using (4), $\overline{H}(z)$ for $H_1(z)$ will be as follows:

$$\overline{H}_1(z) = \begin{bmatrix} \frac{1}{1-z^{-l}} & \frac{1}{1-z^{-l}} \\ z^{-1}\frac{1}{1-z^{-l}} & \frac{1}{1-z^{-l}} \end{bmatrix} \tag{10}$$

Similarly for block B in Fig. 6(a), $H_2(z)$ can be determined as:

$$H_2(z) = \sum_{l=0}^{1} z^{-l} E_l(z^2) = E_0(z^2) + z^{-l} E_1(z^2) = \frac{z^{-l}}{1-z^{-l}} = \frac{z^{-l}+z^{-2}}{1-z^{-2}}$$
$$= \frac{z^{-2}}{1-z^{-2}} + z^{-l}\frac{1}{1-z^{-1}} \tag{11}$$

which ends up with the following equations for $E_l(z^{-1})$:

$$E_0\left(z^{-1}\right) = \frac{z^{-l}}{1-z^{-l}} \tag{12}$$

and

$$E_1\left(z^{-1}\right) = \frac{1}{1-z^{-l}}. \tag{13}$$

Finally, the expression of $H_2(z)$ will be as follows:

$$\overline{H}_2(z) = \begin{bmatrix} z^{-1}\frac{1}{1-z^{-l}} & \frac{1}{1-z^{-l}} \\ z^{-1}\frac{1}{1-z^{-l}} & z^{-1}\frac{1}{1-z^{-l}} \end{bmatrix}. \tag{14}$$

Figure 5(b) shows the time-interleaved equivalent circuits of blocks A and B. Using (10) and (14), $\overline{H_1}(z)$ and $\overline{H}_2(z)$, in Fig. 5(b), are the polyphase equivalents of block A and block B, respectively where

$$U = \overline{H}_1 \cdot T \quad \text{or} \quad \begin{bmatrix} U_1 \\ U_2 \end{bmatrix} = \begin{bmatrix} \frac{1}{1-z^{-l}} & \frac{1}{1-z^{-l}} \\ z^{-1}\frac{1}{1-z^{-l}} & \frac{1}{1-z^{-l}} \end{bmatrix} \begin{bmatrix} T_1 \\ T_2 \end{bmatrix} \tag{15}$$

and

$$W = \overline{H}_2 \cdot V \quad \text{or} \quad \begin{bmatrix} W_1 \\ W_2 \end{bmatrix} = \begin{bmatrix} z^{-l}\frac{1}{1-z^{-l}} & \frac{1}{1-z^{-l}} \\ z^{-1}\frac{1}{1-z^{-l}} & z^{-l}\frac{1}{1-z^{-l}} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{16}$$

These blocks will work at half the speed of the original modulator and only delay blocks and down-samplers will work at the original clock speed. These parts can be implemented using very high speed de-serializers at the input and serializers at the output of the time-interleaved modulator. Such component are embedded in some FPGAs with the capability of supporting up to 32 channels and clock speed higher than 6 GHz. Fig. 5(b) can be simplified further, by removing the consecutive down-samplers and up-samplers and modifying the modulator's feedback path, as shown in Fig. 5(c). The output signal of this modulator has bi-level format and is ideal for deriving SMPAs.

Table 1. Comparison of simulated SNDR of time-interleaved and non time-interleaved modulators for different signals.

Standard	BW (MHz)	OSR	M*	Modulator Clock (MHz)	SNDR (dB)
WiMAX	4	160	1	640	69.17
			2	320	69.17
			4	160	69.17
			8	80	69.17
	8	100	1	800	64.27
			2	400	64.28
			4	200	64.24
			8	100	64.24

*M shows the number of interleaved channels, $M = 1$ means modulator without time-interleaving (basic modulator).

6. SIMULATION COMPARISON OF TIME-INTERLEAVED AND BASIC MODULATORS

MATLAB and SIMULINK have been used for simulation of designed TIDSM. OFDM based WiMAX signal with 4 MHz and 8 MHz bandwidths and 160 and 100 oversampling ratios are used for simulation. While the sampling frequency of the signals are 640 MHz and 800 MHz respectively, for example by using eight channels TIDS modulator, the clock speed required for the modulator will be 80 MHz and 100 MHz respectively to achieve the same performance. Table 1 shows the simulation results of the SNDR for modulator shown in Fig. 5(a) and its equivalent parallel modulators. The SNDR definition is shown in (17), where I_{in} and Q_{in} are the in-phase and quadrature-phase of the input signal, respectively, and I_{out} and Q_{out} are the in-phase and quadrature-phase of the output signal, all of them normalized, respectively:

$$\begin{aligned} SNDR &= 10\log\left(\frac{Signal\,Power}{Noise\,and\,Distortion\,Power}\right) \\ &= 10\log\left(\frac{I_{in}^2 + Q_{in}^2}{(I_{in} - I_{out})^2 + (Q_{in} - Q_{out})^2}\right) \end{aligned} \tag{17}$$

These results show that, while the modulators' performances are maintained, the clocks or processing speeds decrease considerably with an increase in the number of interleaved channels.

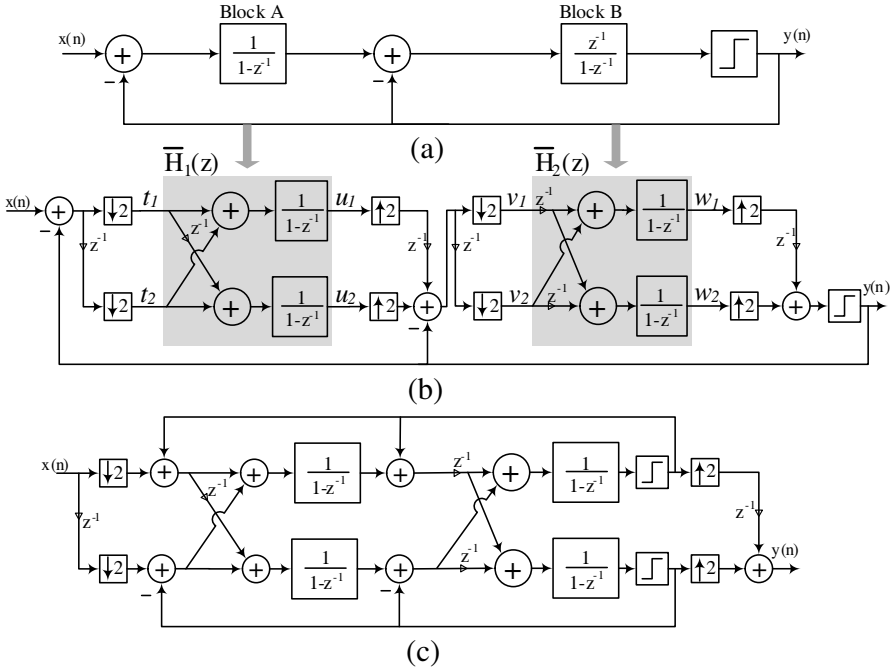

Figure 5. Second-order delta-sigma modulator and its equivalent two-branch TIDS modulator.

The drawbacks of using time-interleaved parallel delta-sigma modulators are complexity and the requirement for more resources in the FPGA. Table 2 shows a comparison between the FPGA's resources needed for the original modulator in Fig. 6(a) and its equivalent time-interleaved modulators. The resources required to implement the modulator with eight time-interleaved channels represent a very small amount of the total resources in a typical FPGA. Indeed, the required resources increase from 1% for the conventional implementation of the delta-sigma modulator to 6% when eight parallelization channels are used.

7. DESIGN, IMPLEMENTATION AND MEASUREMENT RESULTS

The time-interleaved delta-sigma modulator was implemented in a Stratix II GX FPGA from Altera [22]. To implement the IQ modulator, a 2080MX 4×1 multiplexer from Inphi with a maximum clock speed of 20 GHz was usedwhere. We are able to cover carrier frequencies up to 5 GHz.

Table 2. Used resource comparison of FPGA for time-interleaved and non time-interleaved modulators.

Modulator Structure	ALUT*	Registers	Memory (bits)	PLL
Total in FPGA	**72768**	**72768**	**4520488**	**8**
$M^{**} = 1$	270 (< 1%)	95 (< 1%)	1015808 (22%)	1 (13%)
$M = 2$	554 (< 1%)	290 (< 1%)	1015808 (22%)	1 (13%)
$M = 4$	1443 (2%)	603 (< 1%)	1015808 (22%)	1 (13%)
$M = 8$	4156 (6%)	1339 (2%)	1015808 (22%)	1 (13%)

*ALUT means adaptive look-up table.
**M shows the number of interleaved channels, $M = 1$ means not time-interleaved modulator.

The only parts in time-interleaved parallel modulator that need to work in original clock, are delays and down-samplers at the input and up-samplers and delays at the output of modulator as shown in Fig. 4. By using high speed 6.34 GHz embedded de-serialzier and serializer in Stratix II GX FPGA, these high speed blocks are implemented easily [22]. In fact, time-interleved structures are extremely sensitive to gain, offset and timing mismatch between branches. Implementing the topology in digital domain and especially using embedded FPGA's serializer and de-serializer avoid most of these problems.

The parameters and constraints required to be considered in designing the proposed fully digital transmitter were signal bandwidth (BW), output carrier (f_c) and maximum clock of FPGA (f_{FPGA}). The procedure to extract the required parameters was as follows:

1. In first step, the clock speed of the multiplexer (f_m) is assigned, considering the fact that it must always be four times of the output carrier frequency as:
$$f_{in} = 4f_c \tag{18}$$
For example, a carrier frequency of 2.5 GHz results in 4×1 multiplexer with a clock speed of 10 GHz. Since, the maximum clock of the multiplexer is limited to 20 GHz, the maximum carrier frequency is 5 GHz.
2. Moreover, to avoid the aliasing, f_c should be equal to or higher than the signal's sampling frequency (f_s). Therefore, knowing the signal's bandwidth and carrier frequency, the maximum allowed OSR is as follows:
$$f_s = OSTR_{\max} * BW \leq 2f_c \Rightarrow OSTR_{\max} \leq {}^{2f_c}/_{BW} \tag{19}$$

For example, if f_c is equal to 2.5 GHz and BW is equal to 20 MHz, the $OSR_{\max}$ is 250. This is the maximum possible OSR; however, a lower OSR can be used in cases where the required performance in terms of SNDR is achieved.

3. Finally, it is required to set a constraint on the maximum usable clock, which depends mainly on the signal type, quality of signal and specified maximum FPGA clock. However, for the signals used, the order of the modulator selected and based on our experience, the FPGA clock (f_{FPGA}) that guarantees good performance of FPGA, was found to be around 150 MHz, despite the maximum FPGA processing speed of 500 MHz. With this constraint, the minimum number of branches, M, of the parallel time-interleaved modulator can be found as:

$$f_s/M \leq f_{FPGA} \Rightarrow M \geq ceil\left(OSR * BW/f_{FPGA}\right) \tag{20}$$

The described procedure was applied for scenarios with carrier frequencies of 2.1 GHz and 2.5 GHz and signal bandwidths of 4 MHz and 8 MHz. Using (18), the f_m would be 8.4 GHz and 10 GHz for the 2.1 GHz and 2.5 GHz carrier frequencies, respectively.

According to (19), for 4 MHz and 8 MHz bandwidths and a 2.1 GHz carrier frequency, the maximum OSRs are 1050 and 525, respectively. However, as explained before, it is possible to choose smaller OSRs, when the required SNDR performance is achieved. Here, OSRs of 160 and 100 for 4 MHz and 8 MHz signal bandwidths were selected.

Finally, using (20), the minimum number of parallel delta-sigma modulator branches for 4 MHz and 8 MHz signal bandwidths were found to be 5 and 6. Herein, an 8-branch parallel delta-sigma modulator was developed for all the scenarios.

MATLAB and Simulink software were used for simulation, and Quartus II from Altera was used for analysis and synthesis of the designed delta-sigma modulator and FPGA programming.

The multiplexer up-converter had four differential input data, one differential input clock and one differential output data. Using differential signals reduces the noise and parasitics, which is very useful at these high-speed frequencies.

In the implementation phase, two important issues should be considered to insure the good modulator's performance. One is extracting the correct bit widths for all the components of delta-sigma modulator in the FPGA to avoid the integrators to overflow and at the same time to minimize the FPGA's resources needed for the delta-sigma modulator implementation. MATLAB's fixed-point toolbox is used to find the optimum bit widths of all components. The second one

is applying time constraint to avoid different delays on similar paths in the FPGA which can degrade the performance of the delta-sigma modulator significantly. This problem is more pronounced for time-interleaved modulators, which have more parallel paths and are more complex.

To measure the performance of the designed time-interleaved delta-sigma modulator, Agilent 16901A Logic Analyzer is used to capture the signal at the output of FPGA. The logic analyzer will be put in a synchronized method where its clock is provided in the FPGA with the same speed of the signal. These assure that our measurement only shows the effect of the time-interleaved delta-sigma modulator on signal quality. Fig. 6 shows the block diagram of the measurement setup and Fig. 7 shows a photograph of the measurement setup including FPGA board, logic analyzer and connector adaptors to connect FPGA's outputs to logic analyzer's probe.

Figures 8(a)–(b) show the measured power spectrums for a LTE signal with a 3.84 MHz bandwidth and a WiMAX signal with an 8 MHz bandwidth, respectively. In both cases, time interleaving equal to 8 was used. The 4 MHz signal has an OSR equal to 160, which resulted in SNDR equal to 64 dB. The 8 MHz signal has lower OSR — equal to 100 and resulted in slightly lower SNDR equal to 60 dB as reported in Table 3. The difference in SNDR values between simulation results in Table 2 and measurement results in Table 3 is due to the hardware non-ideal behaviors, which increase the noise floor of the system. These effects were not taken into account in simulation. Despite the degradation in noise floor between measurement and simulation, the measured results in Table 3 for the time-interleaved technique showed a are very acceptable linearity performance (SNDR = 60 dB) for a signal bandwidth as wide as 8 MHz.

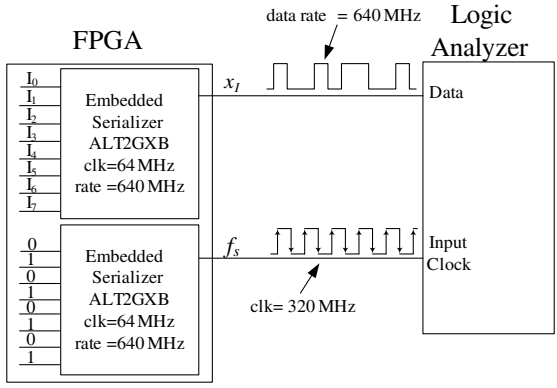

Figure 6. The block diagram of the measurement setup.

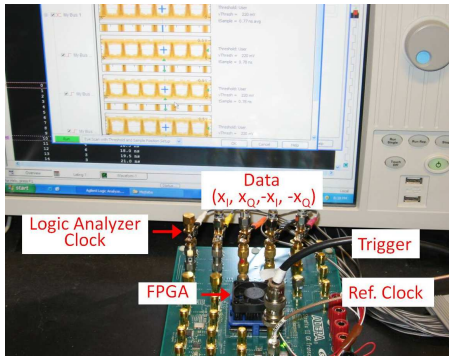

Figure 7. Photo of measurement setup including FPGA and logic analyzer.

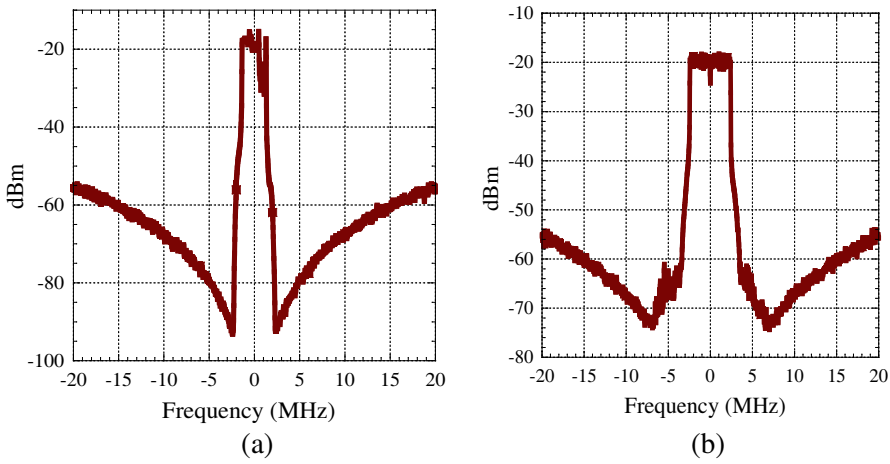

Figure 8. Measurement results for: (a) LTE signal with OSR = 160 and a bandwidth equal to 3.84 MHz for $M = 8$; (b) WiMAX signal with OSR = 100 and bandwidth equal to 8 MHz for $M = 8$.

To the best of the authors' knowledge, this is the first use of time-interleaved 1 bit delta-sigma modulator for transmitter applications. The performance of the proposed approach is compared in Table 4 to the state-of-the art results obtained for delta-sigma modulator for applications as ADC and DAC. The table compares the requirements on the clock speed, number of bits, number of time-interleaved channels, bandwidth and SNDR are listed in Table 4. While most of these results are achieved with integrated circuit, the results of

Table 3. SNDR measurements for different signals and bandwidths.

Signal	BW (MHz)	OSR	SNDR (dB)
WiMAX	4	160	64.5
LTE	3.84	160	62.4
WiMAX	8	100	60.3
LTE	7.68	100	59.1

Table 4. Comparison of high-bandwidth state-of-the-art $\Delta\Sigma$ modulators.

Ref	Architecture	BW (MHz)	Sampling Freq (MHz)	Number of Channels	Number of Bits	SNDR (dB)
[23]	2-Cascaded	10	160	1	4	57
[24]	5th Order	12.5	200	1	14	72
[25]	4th Order	15	300	1	11	64
[26]	3rd Order	10	100	2	4	50
[27]	3rd Order	10	640	1	1	65
This work	2nd Order	4	640	8	1	65
This work	2nd Order	8	800	8	1	60

our FPGA implemented modulator are competitive with recent high-bandwidth modulators. It matches the highest input bandwidth obtained with recently published modulators, and has the potential to operate at a higher sampling frequency up to 6.34 GHz and therefore higher bandwidth, as was discussed before.

8. CONCLUSION

This paper describes the wideband, highly efficient, fully digital transmitter for SDR applications, where, by utilizing a parallel time-interleaved technique, the transmitter bandwidth can be significantly extended using the same clock speed for the FPGA. Delta-sigma modulation is used to provide a constant amplitude bi-level signal for highly efficient switching-mode PAs and a high-speed 4×1 multiplexer used for digital IQ modulation and up-conversion.

A step-by-step design procedure is presented to determine the transmitter's parameters, such as multiplexer clock, delta-sigma modulator clock, maximum *OSR* and total number of branches for the modulator.

The architecture developed in this work has been validated, through simulation and FPGA implementation, with new standards as WiMAX and LTE. Results show an SNDR around 60 dB for an 8 MHz signal bandwidth with 100 oversampling ratio at the output of the FPGA using Agilent 16901A high speed differential Logic Analyzer.

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