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Time interleaved optical sampling for ultra-high speed A/D conversion

A. Yariv and R.G.M.P. Koumans

A scheme is proposed for increasing the sampling rate of analogue-to-digital conversion by more than an order of magnitude by combining state-of-the-art A/D converters with photonic technology. Ultra-high speed sampling is performed optically by a multiwavelength pulse train. Wavelength demultiplexers convert the high repetition rate data stream of samples into parallel data streams that can be handled by available electronic A/D converters.

Introduction: The increasing demand in military systems, and soon in civilian systems, for real-time data over a wide range of signal frequencies has created the need for high speed analogue-to-digital (A/D) converters. Current state-of-the art electronic A/D converters operate at a sampling rate of about 10Gsample/s. Such a rate is not sufficient for sampling, for example, high-end microwave signals. Sampling at a rate of, for example, 100Gsample/s would require electronic circuitry with uniform frequency responses up to 200–300GHz. This technology is not available today and new approaches need to be considered. One such approach, realisable with state-of-the-art electronic and optoelectronic components, is described in the following.

The main tenet of our scheme is to use wavelength multiplicity to increase the sampling rate of A/D converters. This approach has been made practical by recent developments in wavelength division multiplexing (WDM) 'add/drop' filters [1] and semiconductor modelocked lasers [2]. The scheme makes use of a multiwavelength sampling pulse train (MW-SPT). This pulse train consists of ultra-short optical pulses with different wavelengths. To be specific, the wavelength of each pulse in the train is different from the wavelength of its neighbours, in a repeating fashion (see Fig. 1).

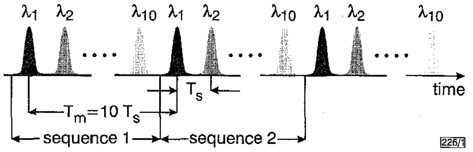

Fig. 1 *Multiwavelength ultra-short pulse train with 10 different wavelengths*

T_s: sampling period; T_m: period for pulses with same wavelength

If the goal, for example, is to sample an analogue signal at a rate f_s = 100Gsample/s, the temporal spacing between two adjacent sampling pulses will be $T_s = 1/f_s$ = 10ps. As depicted in Fig. 1, neigbouring pulses in the pulse train will have different wavelengths $\lambda_1 \ldots \lambda_N$, where N is the number of wavelengths used. In our example we will use $N = 10$. The optical pulse train is thus made up of a repeating sequence of pulses with 10 different wavelengths within each sequence. The temporal spacing between pulses of the same wavelength is $T_m = NT_s$ = 100ps, i.e. the sampling rate for pulses at a particular wavelength is $f_m = f_s/N$ = 10Gsample/s.

A schematic view of our photonic A/D converter incorporating this MW-SPT is shown in Figs. 2 and 3. The MW-SPT is used to sample the analogue signal $V(t)$ by feeding it as the optical input to an electro-optic modulator. The modulator is driven by the microwave signal to be sampled (see Fig. 2).

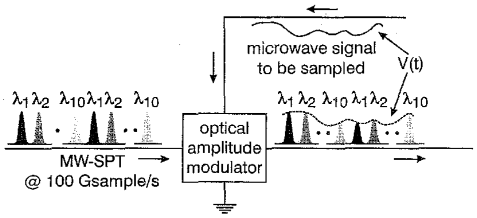

Fig. 2 *MW-SPT sampling microwave signal at 100Gsample/s*

The train of optical pulses at the output of the modulator is thus multiplied by the analogue signal $V(t)$. An optical high resolution wavelength demultiplexer ('drop' filters) is then used to separate the 10 wavelengths, resulting in 10 individual parallel optical pulse trains with a relatively low sampling rate f_m. Each of these trains can now be detected by a photodetector and converted into a digital signal by available state-of-the-art A/D converters (see Fig. 3).

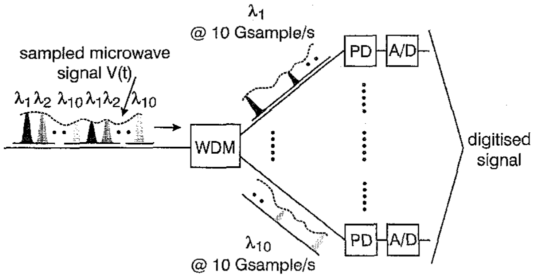

Fig. 3 *Stream of samples at 100 Gsample/s wavelength demultiplexed (WDM) into 10 parallel 10Gsample/s streams detected by photodetectors (PD) and processed by electronic A/D converters*

The net result is thus 10 parallel electronic bit-streams that contain the sampled information of the analogue signal $V(t)$ in a parallel and interleaved fashion.

Generation of MW-SPT: The most crucial part in the photonic A/D converter is the MW-SPT. Pulse to pulse fluctuations, i.e. amplitude-, pulsewidth and timing-jitter, should be small in order to avoid distortion. Also, the pulsewidth of an individual pulse should be small compared to the sampling time T_s so that individual pulses behave essentially as delta functions when sampling the analogue signal. Hybridly modelocked semiconductor lasers are capable of generating stable high repetition rate ultra-short pulse trains with relatively little amplitude and timing jitter [2]. Recently, lowloss add/drop filters have become available for WDM [1], so that multiple pulse trains from lasers modelocked at different centre wavelengths can be multiplexed with low-loss into an even higher repetition rate MW-SPT suitable for A/D conversion. Our proposed scheme to generate the MW-SPT is depicted in Fig. 4.

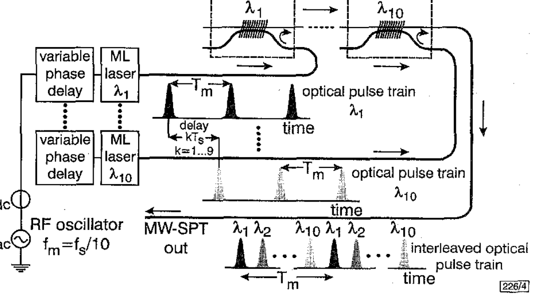

Fig. 4 *Generation of MW-SPT using hybridly modelocked lasers, electronic phase delays and low-loss add filters*

We use 10 monolithically modelocked semiconductor lasers to generate 10 pulse streams with different wavelengths $\lambda_1 \dots \lambda_{10}$. The wavelength of each laser can be controlled by changing its temperature. A more elegant method for wavelength control could be obtained by incorporating Bragg gratings inside the laser cavity. This would lead to an increase in pulse power by confining the gain to a specific wavelength region [3] as well as improving the locking bandwidth of the device for hybrid modelocking [4]. All lasers are hybridly modelocked by the same high quality, low timing-jitter electronic RF oscillator at a modulation frequency f_m = 10GHz. The delay between pulse streams is controlled electronically by variable phase delays to the RF signal. Low-loss add filters are used to interleave all 10 pulse trains into the MW-SPT of Fig. 1. For our example of T_s = 100Gsample/s, pulsewidths would be of the order of a few picoseonds while wavelength spacing would be around $\Delta\lambda = \lambda_n - \lambda_{n-1} \simeq 3$nm. These values can be easily achieved with present modelocked semiconductor lasers [5].

A multi (modelocked) laser system can be produced monolithically which has the advantage of compactness. The modelocking process takes place in a cavity of only a few millimetres in contrast to externally modelocked semiconductor lasers and fibre modelocked lasers where long term cavity stability and bulk optics are a problem. The repetition rate of the sampling pulses for a particular wavelength needs to be in the gigahertz range. The repetition rate of a modelocked laser is determined by its cavity length. When using monolithic semiconductor lasers, a gigahertz repetition rate can be easily obtained by cleaving the semiconductor wafer to a few millimetres. Externally modelocked lasers and fibre lasers usually have cavity lengths up to a couple of metres leading to an extremely low pulse repetition rate, meaning that additional temporal multiplexing will be necessary to obtain a repetition rate in the gigahertz range.

Pulse trains with different wavelengths can also be generated in various other ways [6] using a single laser, for example by spectral slicing. In our approach we have explicitly chosen to use separate lasers with the advantage that wavelength dependent losses in the A/D system can be compensated by changing the gain of the laser that provides that particular wavelength.

A major system advantage of using multiple lasers is that the delay between pulses in the multiwavelength train can be easily controlled electronically by phase delays of the RF drives to the individual lasers. Pulses from a single laser would require very accurate picosecond optical delay units which are difficult to engineer.

Summary: We have proposed a scheme for incorporating an ultra-high speed A/D converter combining photonics and electronics. Monolithically modelocked semiconductor lasers are used to generate ultra-short pulse trains at different wavelengths with low noise which are interleaved into an MW-SPT with WDM add filters. Sampling of the analogue signal is performed optically using this MW-SPT and an electro-optic modulator. The ultra-high speed sample stream is subsequently demultiplexed with drop filters into parallel streams with a lower sampling rate. State-of-the art electronic A/D converters then digitise the low-rate samples in a parallel fashion.

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BiCMOS logic circuit for single-battery operation

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A novel BiCMOS logic circuit is described that provides high-speed rail-to-rail operation with only one battery cell (1–1.5V). The proposed circuit utilises a novel pull-down scheme that involves bootstrapping the base of the pull-down *pnp* bipolar junction transistor to a negative potential during the pull-down transient period. Circuit simulations have shown that the proposed circuit outperforms the transient-saturation full-swing BiCMOS [1] and the bootstrapped bipolar CMOS [2] circuits in terms of delay, power and cross-over capacitance for all simulated supply voltages.

Introduction: As supply voltage reduction is the key to low-power operation, the supply voltage of digital logic circuits has been scaled down aggressively in recent years. Indeed, several BiCMOS circuits that achieve high-speed full-swing operation for a supply voltage as low as 1.5V have been reported [1 – 4]. The transient-saturation full-swing BiCMOS (TS-FS-BiCMOS) circuit proposed in [1] has a high transistor count and power dissipation (verified by our simulations, shown in Table 1 and Fig. 3*b*). The bootstrapped bipolar BiCMOS (B^2CMOS) circuit reported in [2] utilised bootstrapping to provide fast pull-up operation, but suffers from high intrinsic output capacitance and non-full-transient swing at low supply voltages. Moreover, it fails to function properly when MOSFET devices with low threshold voltages (less than half V_{BE} of a bipolar device) are used. This is due to charge leakage from the bootstrapping capacitor into the supply during the pull-up operation. We proposed the use of bootstrapping in the pull-down section in [3], but the circuit suffers from relatively high input gate capacitance. This Letter describes a novel BiCMOS logic circuit that provides fast full-transient-swing operation down to a supply voltage of 1V, using only *pnp* bipolar drivers. Although the performance of *pnp* bipolar junction transistors (BJTs) has so far been less than desirable, recent advances in *pnp* processes [5, 6] have provided means of developing high-performance *pnp* bipolar devices that offer high speed at lower power levels. This has prompted us to design a circuit that is based on an *n*-substrate, *p*-well 0.5μm BiCMOS process, using high-performance *pnp* BJTs in both its pull-up and pull-down sections.

Table 1: Comparisons of proposed, CMOS, TS-FS-BiCMOS and B^2CMOS circuits at 1.2V supply voltage and 1pF capacitive load

	Delay	Power	Power × delay	Area
	ps	μW	fJ	μm²
CMOS	2745	19	52	70
TS-FS-BiCMOS	1310	38	50	460
B^2CMOS	1145	32	37	490
Proposed	890	27	24	380

Circuit description and operation: The proposed circuit, an inverter, is shown in Fig. 1. As the pull-up section is identical to