TLP Calibration, Correlation, Standards, and New Techniques

Jon E. Barth, *Member, IEEE*, Koen Verhaege, Leo G. Henry, *Member, IEEE*, and John Richner

***Abstract*—This paper describes a constant impedance transmission line pulse system with new measurement capabilities and improved accuracy. The paper enforces a broader look at transmission line pulse (TLP) data, beyond the I–V curves. Accurate TLP measurements and actual TLP/HBM device data are used to demonstrate dV/dt effects and HBM/TLP correlation and miscorrelation. Finally, a calibration method and standard TLP test method are presented for adaptation by the industry. This is necessary to provide correlation and repeatability of experimental data.**

***Index Terms*—ESD, HBM, IC protection, pulse curve tracing, time domain measurements, TLP.**

I. Introduction

TRANSMISSION line pulse (TLP) test systems have been used to evaluate the electro static discharge (ESD) behavior of silicon devices and integrated circuits since Maloney *et al.* [1], [2] first published the application of transmission line pulses for ESD testing in 1985. Since then, TLP has allowed tremendous insight into the electrical characteristics of ESD protection circuits and devices [3]–[14]. The main value of TLP has always been to reduce design cycle time for these protection circuits [9], [15]. Section II will re-introduce the constant impedance TLP technique. The comparison with the 'classic' constant current TLP technique will be made. Advantages and disadvantages will be reviewed. Section III will introduce a new look at TLP data. In the literature, most authors show a TLP I–V response and indicate I_{t_2} as being the point of failure. Few have published the leakage current [8]–[10], [14] after each pulse discharge, and it appears that very few consistently published *in-situ* leakage evolution measurements. This paper will argue and show why leakage evolution during TLP should be monitored and will show an elegant plot that includes both the TLP I–V data and the leakage evolution data.

Many researchers have established that most HBM and TLP failures were junction and not dielectric related. It has been shown that both HBM and TLP can produce identical failure mechanisms and locations [12], [15]. Correlation has also been shown to occur between TLP (with rectangular pulse widths of 75–200 ns) and HBM (with a 150 ns double exponential pulse width **)** [7], [11]–[13]. The correlation is established through the TLP current and the assumed HBM peak current (i.e., $V_{\rm hbm}$ [V] divided by 1.5 kΩ [7], [13]. However, some authors have shown inconsistent and noncorrelation results, and have related this to risetime issues. Section IV will give the theory and show the data that explains most, if not all, of these issues. Section V will discuss contact resistance issues that arise in wafer level TLP systems. Section VI will review the need for calibration and standardization of TLP test systems and TLP data presentation. Suggestions for a TLP standard test method will be presented. Section VII is the summary.

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J. E. Barth and J. Richner are with the Barth Electronics Inc., Boulder City, NV 89005 USA (e-mail: jonbarth@ieee.org).

K. Verhaege is with the Sarnoff Corporation, Princeton, NJ 08543 USA (e-mail: kverhaege@sarnoff.com).

L. G. Henry is with ESD/TLP Consultant, Fremont, CA 94538 USA (e-mail: leogesd@pacbell.net).

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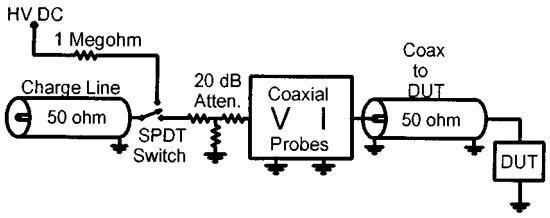

Fig. 1. TLP-50: a constant impedance 50 Ω TLP system.

II. Constant Impedance TLP

Changing a "classical," constant current TLP system to a constant impedance TLP system can significantly enhance the ESD value of the TLP test method. The TLP system we use has a constant impedance of 50 Ω throughout the system up to the device under test (DUT). We define the constant impedance TLP system as TLP-50 (Fig. 1). This TLP-50 produces a pulse from the standard 50 Ω transmission line source followed by a matched 50 Ω attenuator to absorb reflections from the DUT. From there, the pulse travels through rise time filters, coaxial voltage/current sensors, a coaxial switch, which allows connection of the DUT to a pA-meter, and on to the DUT. The operation of the 50 Ω transmission line, high voltage (HV) power supply and switch used to generate rectangular, or square, pulses has been well explained in a number of other sources [12] and will only be briefly described here.

One of the advantages of maintaining a 50 Ω constant impedance for the pulse travel through the system is that the pulse rise time of the TLP pulse is not degraded. Though the HV switch will provide the fundamental limit to the pulse rise time, the reflection losses among all coaxial connections including the transmission lines will further limit the usable test pulse rise time.

Using the circuit arrangement of Fig. 1, allows the DUT to be momentarily disconnected from the pulse source with a coax switch so that it can be connected to a pA-meter. During this time a dc leakage measurement at a selected voltage is made

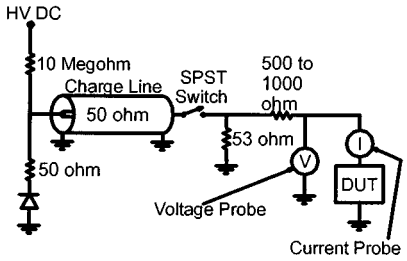

Fig. 2. TLP-500: a constant current TLP system.

after every test pulse with the DUT in situ. The leakage current measurement is then plotted against the measured pulse current. The constant impedance system allows both the pulse and leakage measurements to be made when testing either socketed devices or when TLP testing on wafer.

Unlike the simple switch found in most constant current TLPs, the single pole double throw (SPDT) switch completely disconnects the pulse generating circuit from the HV power supply after the line is charged. This prevents any leakage current from the HV supply from flowing through the charge resistor and into the test circuit when the discharge switch is closed. This is not a concern when the device is in the conducting mode, but can cause problems when the device is nonconducting. Using a SPDT switch can prevent any of these problems or errors.

The traditional or classical TLP system uses a shunt resistor to ground, and a 500 to 1000 Ω series resistor to the DUT to provide a constant current source. The shunt resistor is typically 53 Ω in an attempt to provide a 50 Ω match with the parallel combination of a 500 Ω resistor and the DUT. See Fig. 2. We define this as a TLP-500 system, because in most systems the series resistor used is 500 Ω [8].

It is difficult to make in situ leakage current measurements with a TLP-500 system after every test pulse directly at the DUT. This is because the 53 Ω shunt resistor is connected to ground at the end of the pulse source. That resistor is needed to provide a matched load to the pulse generator, and absorb most of the reflections from the DUT. It is important to absorb energy reflected from the DUT in either system to minimize re-reflected pulse energy to the DUT. If the reflected energy is not absorbed, it provides an unknown amount of excess energy dissipation in the DUT.

Measuring DUT leakage current with TLP-500 systems usually requires that the device be moved to a source measurement unit (SMU) after each test pulse. This (Nike process) is very time consuming. Based on the many TLP papers, which do not present leakage data, it appears that in situ leakage data is often not used. The most important concept of measuring leakage current in situ after every test pulse is that it allows the user to know how the leakage current evolved as the pulse test current amplitude was increased.

We choose to define the impedance of a TLP system as the source impedance that the DUT sees. This is because the voltage and current parameters at the DUT for any pulse source voltage are determined by both the DUT impedance and the tester source impedance.

The primary limitation of a TLP-50 system is that a low impedance does not permit measurements of typical "S" type negative resistance characteristics when the absolute value of the slope is greater than 50 Ω. The 50 Ω load line in the negative resistance area can obscure the true value of the holding current immediately after snapback. The TLP-500 system has a bigger window to look at such data, since the load I–V curve is 10 times flatter, in the negative resistance area. Each system can measure negative resistance slopes equal to or less than its impedance.

If the actual holding current is an important data point, it can be measured with a conventional AC curve tracer. The device holding current should be less than approximately 100 ma, if damage during this measurement is to be avoided. Conventional ac curve tracers dissipate higher average energy in the DUT than TLP curve tracers, because they use continuous ac instead of being pulsed.

However, as discussed below, the 50 Ω TLP-50 system can be designed with very fast rise times such that with the help of dV/dt, the trigger voltage can be reduced such that the lowest holding point can be accurately displayed. Because of the lower source impedance of the TLP-50, it can place I–V points with the finest steps in approaching and determining the exact trigger and hold points. This is difficult with TLP-500 systems.

Also, as discussed by Russ in [15], many devices have a nonuniform conductivity within a single finger which shows as a zero delta resistance (vertical) behavior after snapback, before a resistive phase in the I–V curve. This phenomenon can be seen with accurate TLP-50 measurements and allows a vertical extrapolation to determine the actual holding voltage.

A. Balanced Wafer Probe Testing

The TLP-50 system carries a 50 Ω constant impedance through to the DUT when testing on a wafer. A significant improvement has been made in testing on wafers with a two needle balanced wafer probe. The test pulse is carried through 50 Ω cable to the wafer probe, through a 50 Ω balun, through a 50 Ω balanced reversing switch, and through balanced 50 Ω line down to the needles. This allows it to transfer the fastest possible TLP test pulse rise time to the needles and pads. The test pulse reflected from the DUT can pass back to the wide bandwidth coaxial voltage probe with minimum distortion. This allows the speed of the snapback transition to be accurately measured with the extremely wide bandwidth coaxial voltage monitors in the TLP-50 system.

When the test pulse passes through the balun and becomes balanced, it passes through a balanced reversing switch and through a balanced 50 Ω transmission line to the needles. The reversing switch is used to change the test pulse polarity of the needles, as needed depending on pad orientation. Because both ungrounded needle connections to the wafer float above ground, this system closely simulates testing of packaged devices. Balanced needles prevent any capacitive currents from the circuit to the wafer chuck because they are isolated from the ground return path.

Existing TLP-500 systems have one grounded needle [16], [17]. With the high dielectric constant of silicon, testing of

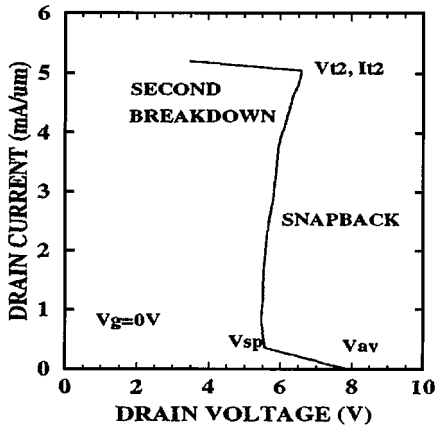

Fig. 3. High current I–V curve after Amerasekera [7].

circuits on wafer can have measurable displacement currents through the silicon to the grounded wafer chuck especially for fast rise time test pulses. Unbalanced TLP-500 testing on wafer with one grounded needle provides a ground return path from the ESD circuit to the test system. Because the TLP-50 balanced dual wafer probe has much lower displacement currents to a ground return, TLP tests of circuits on wafer are closer to the results when testing them in packaged form. Packaged devices have a capacitance of only 1 or 2 pF to ground when tested in a socket that is only slightly isolated from ground.

III. TLP Data Plotting

While measuring the I–V behavior of an ESD protection device with the TLP system, it is obvious that the device is actually being stressed with ESD type pulses. This is effective because 100 ns wide, high current pulses are used. When the device fails during TLP, one can extract a figure of merit that reflects the actual ESD hardness of the device. Due to the nature of the selected TLP pulse one expects to correlate the TLP failure result to the HBM results.

The traditional way to show TLP data is to draw the I–V curve. The common way to indicate failure is to show the so-called I_{t_2} point, or second breakdown point [13], [14], [18]. An illustration is shown in Fig. 3 [7], where V_{sp} is snapback voltage, V_{av} is the avalanche breakdown voltage, V_{t2} is the second breakdown trigger voltage and I_{t2} is the second breakdown trigger current. The above authors concluded that once I_{t2} is reached, damage occurs and that point is used as the monitor parameter for high current robustness. The common focus on the I–V behavior suggests that the failure occurs only when the I_{t2} point is reached. It suggests that I_{t2} equals the maximum current handling capability and thus I_{t2} equals failure. We will show that this may not always be the case if the leakage is monitored *in situ* after each current stress point.

An enhanced look at TLP data is shown in Fig. 4. A second curve is added to the data. On the bottom X, and Y axis the traditional I–V behavior is shown: TLP pulse current versus pulse voltage. On the top X, and Y axis we display the evolution of the leakage current: after the collection of every I–V data point, a simple DC leakage measurement is done on the device under test.

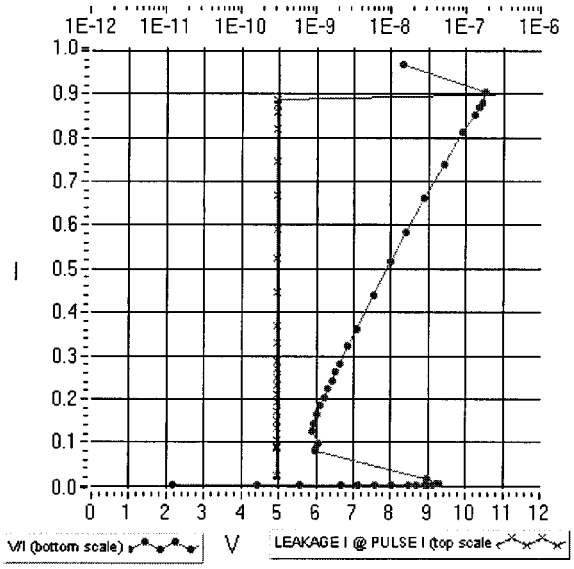

Fig. 4. Complete TLP data set: I–V curve (dot points) to be read on the (bottom) X- and Y-axis; leakage evolution during TLP on the Y- and (top)-X axis. The failure point indicated by the leakage increase corresponds to the second snapback/breakdown point in the I–V curve.

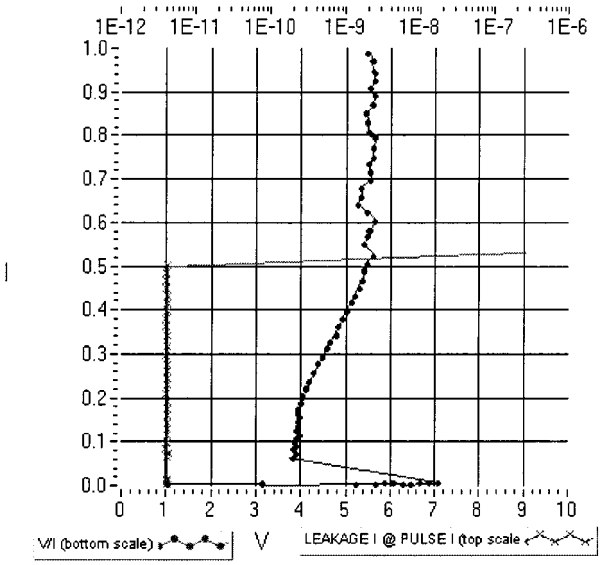

Fig. 5. Complete TLP data set showing correctly that the performance of this device is limited to 500 mA, while the observation of the I–V curve is inconclusive.

The dc leakage value at a given dc bias (e.g., $V_{dd} + 10\%$) is added to the TLP data plot. The leakage current scale is logarithmic and is displayed on the top X-axis. The Y-axis is re-used, as we want to display the leakage evolution as a function of the stress parameter, the TLP pulse current. From Fig. 4 is it clear that the device fails at 900 mA, which is when the leakage suddenly changes from the nA range into the mA range. This is in contrast to the example in Fig. 3 where leakages were measured only at the beginning of the stress testing and at the end of the maximum stress, that is after the I_{t2} point. When the leakage current does not increase until the I_{t2} point, it has little extra value.

For Fig. 5 however, we see a surprising picture: at about 500 mA, the leakage increases and clearly shows that the de-

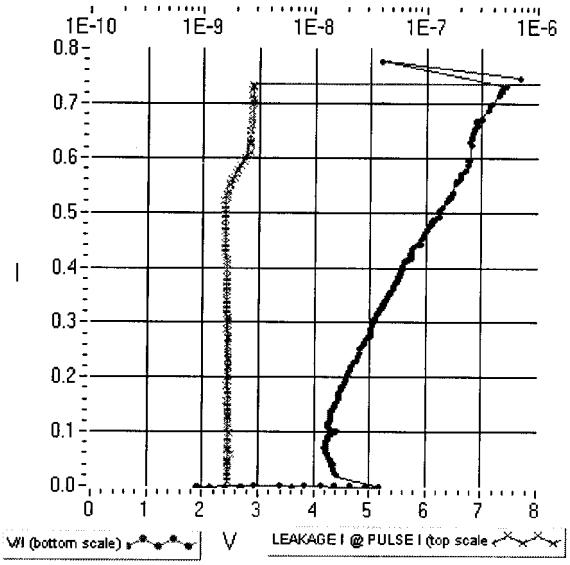

Fig. 6. Complete TLP data set showing correctly that the performance of this device is limited to 500 mA, while the observation of the I–V curve is inconclusive. A soft failure mechanism is demonstrated at a stress level 33% below the I_{t2} point in the I–V curve.

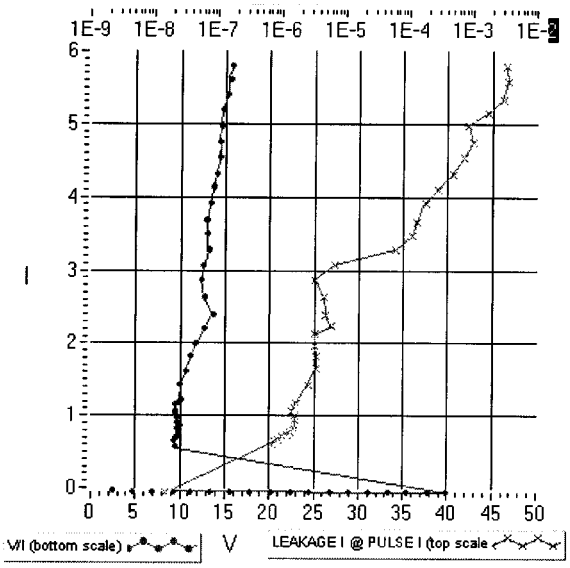

Fig. 7. Complete TLP data set showing a continuous changing leakage evolution, $\times$ points (top scale) from 10^{-8} to 10^{-2} amps.

vice-under-test has failed massively, yet the I–V curve shows no discriminating sign of I_{t2} or second breakdown failure. This is contrary to the data presented for Fig. 3. This is a typical and fairly common picture, a hard device failure where no clear I_{t2}, second snapback, or second breakdown occurs. This is seen mostly in well-ballasted protection devices. Clearly now, including the leakage evolution in the TLP data plot has significant value.

We see a different example for Fig. 6. A soft failure mechanism (at 540 mA—vertical scale) is developing before the hard failure occurs. In this case the I_{t2} or second breakdown point (at 740 mA) indicates hard failure, but the true performance of the device is limited by the on-set of a gradual leakage increase beginning at the device current of 540 mA (vertical axis). The device finally fails catastrophically at a device current of 740 mA (device voltage of 7.6 V, x-axis) where we also see the I_{t2} point on the I–V curve. In this example, the ESD designer cannot use the I_{t2} value, but may want to design the ESD protection level based on the soft failure point [19].

A final example is given in Fig. 7. This is certainly a bad ESD protection device because the leakage current continues to increase, even though the TLP I–V data shows no sign of trouble up to 6 amps. The leakage data indicates a bad device/design, while the I–V behavior is much less informative. In conclusion, when looking at TLP data, the plot with the leakage evolution added, provides valuable insight. A simple I–V plot without leakage data is not as informative and using it alone can lead to unexpected ESD failure.

IV. Pulse Width and Rise Time Effects

A. HBM-TLP Correlation

TLP testing can be done at any pulse width [11]–[13]. If a pulse width is chosen to provide the same current pulse amplitude damage level as is found in HBM, a one to one correlation

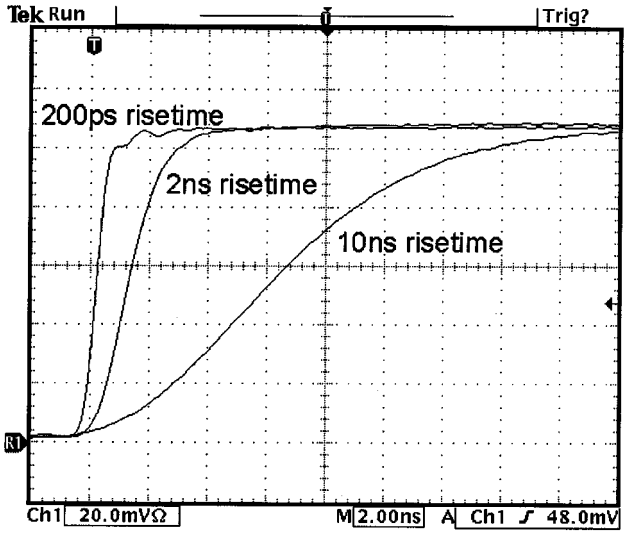

Fig. 8. Represents the 0.2 ns, 2.0 ns, and 10.0 ns Gaussian rise times without any ripples.

will simplify the analysis of ESD protection structures. There have been many different suggestions made as to the pulse width that provides the best correlation with HBM [15], [20]. Theoretically, the TLP rectangular test pulse should be 75 ns long to be equal to the energy in a 1/e decay time constant ($= 150$ ns) double exponential HBM test pulse [6], [12]. There are a couple of problems with determining the optimum pulse width for the closest correlation however. First the standard for HBM testing allows a $\pm 10\%$ range for the peak current and a 2–10 ns range in rise time is specified. These tolerances are quite broad. The risetime and ringing of the HBM tester used for TLP-HBM correlation work also adds to the range of currents that will damage a device [21], [22]. We use controlled 0.2 ns, 2.0 ns, and 10.0 ns, Gaussian shape risetime pulses (Fig. 8), to give a complete risetime range to provide correlation with HBM when using well defined structure dimensions.

TABLE I
TLP/HBM DATA [13] SHOWING THE CORRELATION OF CURRENT AMPLITUDES AT SEVERAL HBM VOLTAGES

	V(HBM) [V]	Ip(HBM) [A]	It2(TLP) [A]
Device-1	1900 +/- 300	1.2	1.25
Device -2	2700 +/- 400	1.8	2.25
Device -3	1100 +/- 200	0.7	0.70
Device -4	1250 +/- 300	0.8	0.70
Device -5	2300 +/- 250	1.5	1.20

TABLE II
TLP/HBM CORRELATION (COLUMN 4) IN A 0.18 μm CMOS TECHNOLOGY

Device #	HBM [kV]	TLP [A]	HBM/TLP
1	4.2	2.75	1.53
2	3.6	2.3	1.56

TLP systems have typically used 100 ns wide rectangular pulses because this length pulse has been found to initiate junction damage at the same peak current as that of HBM test pulses [13]. When the device fails during TLP testing one can extract a figure of merit that reflects the actual ESD hardness of the device. The pass or fail pulse current multiplied by 1500 provides the equivalent HBM voltage amplitude for pass or fail [18]. The 100 ns wide rectangular TLP pulse has been shown to provide correlation to the HBM pulse [13]. A good example from 0.35 μm complementary metal oxide semiconductor (CMOS) technology is shown in Table I after [13]. The columns 3 and 4 in Table I show the HBM peak currents correlates well with the TLP current using a 100 ns pulse width. The TLP test involved stressing the drain with the gate, source and substrate terminals grounded at 0 V. The table shows data for several devices at different pre-discharge HBM voltages.

Table II shows some data that we collected from a 0.18 μm CMOS technology. The Table shows a correlation factor between the HBM pre-discharge kilo-volt level and the TLP current of about 1.5 which was confirmed for many different device types in this technology. It is commonly suggested that the correlation between HBM and TLP results must be 1.5 because the peak HBM current is assumed to be equal to the HBM pre-charge voltage divided by 1.5 k Ω. This is not necessarily the case. The TLP pulse width and also the integrated circuit (IC) technology may have an impact on the correlation factor. It is not uncommon to find a correlation factor closer to 1 [13] or even closer to 3. However, in the author's experience, the correlation factor seems to be stable within one specific IC technology. We note that physical correlation between HBM and TLP can also be established by the comparison of the physical failure signature after failure analysis [24]. This issue is not addressed in this paper.

B. TLP-HBM Miscorrelation

There have been isolated reports of miscorrelation [23], [24]. Table III below shows an example illustrating the issue. The

TABLE III
TLP/HBM CORRELATION AND MIS-CORRELATION BETWEEN TWO DIFFERENT RISE TIMES

Device type / W	HBM [kV]	TLP 0.2 nsec [A]	TLP 10 nsec [A]
1 / 50 µm	1.0	4.1	0.6
2 / 50 µm	0.9	4.2	0.63
3 / 50 µm	1.2	4.4	0.7
1 / 100 µm	1.8	8.3	1.2
1 / 100 µm	2.1	8.5	1.3

results are confirmed by the TLP (10 ns risetime) results for current data in column 4 when compared with the HBM voltage data in column 2. The TLP 10 ns rise time data were taken on the TLP system using a 10 ns pulse rise time and 100 ns pulse width. The correlation (1.43–1.71) is excellent. The miscorrelation is shown by the TLP 0.2 ns data (column 2), which predicts a much better HBM ESD performance, as expected for an SCR device. The TLP pulse rise time for TLP 0.2 ns was 0.2 ns, and the mis-correlation values ranged from 0.21–0.25. The HBM and TLP 10 ns rise time threats have about the same pulse rise time, which provides this close correlation.

C. The dV/dt Triggering

The use of different rise time test pulses allows dV/dt effects to be measured. This testing was done with a 0.2 ns, 2.0 ns, and 10.0 ns Gaussian rise time test pulses with no overshoot or ringing as shown in Fig. 8. The measurement instrument used was the TEK 620B, 0.7 ns risetime scope digitizer. As indicated in an earlier section, there are a couple of problems with determining the optimum pulse width for the closest correlation. In addition, the broad tolerance of 2–10 ns range in rise time as specified in the HBM standard adds to the correlation problems. The risetime variation and added ringing of the HBM tester is avoided in the TLP-50 by using controlled 0.2 ns, 2.0 ns, and 10.0 ns Gaussian shape risetime pulses. These Gaussian waveforms are used because they transition gradually as do most real HBM threat pulses. The Gaussian waveforms are obtained with special filters that can produce the initial rise in a gradually increasing and controlled manner.

High voltage pulses in nature are usually produced this way, so being able to repeat the shape of the initial rise provides an inherent simulation of naturally occurring threats. Such risetime information will also provide data for the fundamentals of a TLP standard test method or standard practice. These clean and controlled test pulses can now be used to measure the magnitude of dV/dt effects. The faster rise times can be helpful to understand CDM like performance. However, one must be extremely careful about using TLP to extract CDM information. A detailed and interesting case study with slower rise times was presented by H. Gieser [5], [25], but is not addressed in this paper.

To address the dV/dt triggering effect, TLP data was taken on a grounded gate nMOS device. A schematic representation is shown in Fig. 9.

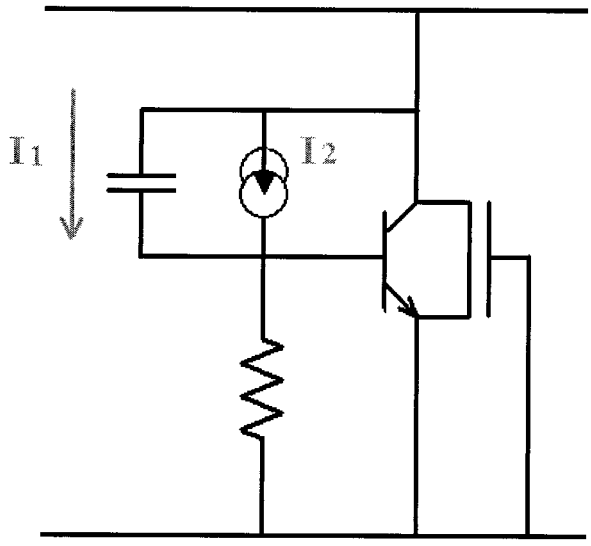

Fig. 9. Grounded Gate nMOS showing its bipolar npn with trigger sources: collector-base junction displacement current, I_1 and collector-base junction avalanche current, I_2.

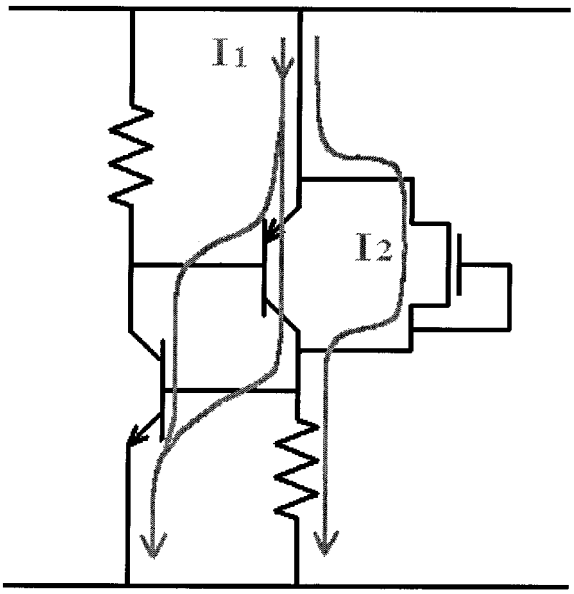

Fig. 10. A schematic representation of the device types: an SCR device with an external nMOS trigger device. This shows intended high current ESD path I_1 and the trigger current path, I_2, which is only intended to provide the trigger. When the SCR does not trigger, the nMOS must absorb the complete ESD current and thus will fail at the nMOS maximum ESD capability.

The triggering of an ESD protection device is influenced by the so-called dV/dt effect, and changes with pulse risetime. With faster pulses, more displacement current (I_1), Fig. 9, is available to help turn on a device. A large displacement (I_1) current may turn-on (e.g., a parasitic bipolar device) because enough current flows through the base resistance without the junction avalanche source (I_2) having to be fully on. This mechanism explains many reported miscorrelation issues (mentioned earlier) and is typically seen in multifinger devices.

The issue with the data presented in Table III, above, is due to a slightly different reason. The dV/dt plays a different role in this case: the SCR (Fig. 10) triggering needs to be supported by enough trigger current. In the TLP 0.2 ns rise time case, the

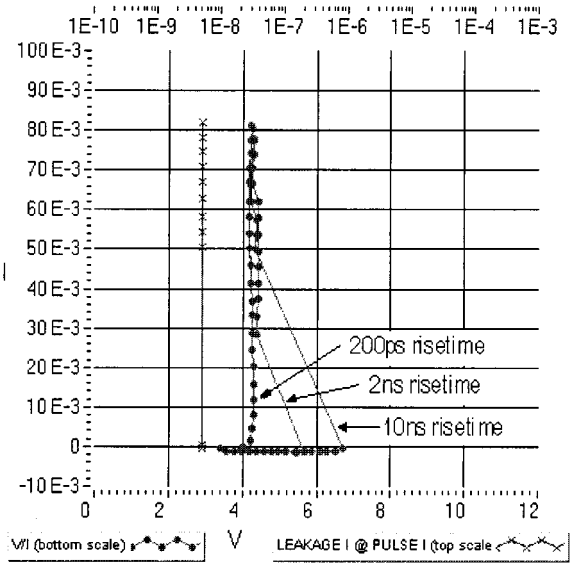

Fig. 11. TLP data set on the 0.25 μm CMOS device for the 10 ns rise time, the 2 ns rise time, and the 0.2 ns rise time.

displacement current adds enough to the nMOS trigger current for the SCR to fully trigger and take the discharge current. In the TLP 10 ns and HBM case, there is not enough trigger current to turn on the SCR and clearly the nMOS takes all the current and fails at its normal level.

In Fig. 10, the current I_1 is the main intended current path and I_2 is the trigger current path, not intended to sustain main discharge current. The HBM results correspond to the equivalent stand-alone nMOS ESD performance, indicating that the main protection device, the SCR, did not trigger during HBM testing.

If we re-visit Table III, we see that the HBM and TLP 10 ns rise time have very similar test pulse rise times, and shows excellent correlation. This correlation disappears when the TLP tester rise time is changed to 0.2 ns shown in the TLP 0.2 ns data in column 3. For this device, dV/dt effects did trigger the SCR and would therefore provide the expected 6 to 12 kV HBM protection performance.

Fig. 11 shows TLP data taken on the ggNMOS device with the dots representing the I–V curve. It shows the slower 10 ns rise time where the snapback trigger voltage is at approximately 6.8 V (the voltage across the device), and the resistive line (snapback region) starts at 50 mA (vertical scale), the current through the device. It also shows that the much faster 2 ns rise time produces a lower snapback trigger voltage of approximately 5.8 V and the resistive line (snapback region) starts at a lower 30 mA of current through the device.

Fig. 11 also shows the very much faster 0.2 ns rise time appears not to produce a real snapback. The breakdown occurs at the lowest value (4.2 V) among the three risetimes and shoots straight up the vertical axis. A close look at all three plots of Fig. 11 reveals that for all three risetimes, the vertical portions of the I–V curves are probably all identical.

D. Transient Latch-Up Sensitivity

The reduction of the peak voltage before snapback with faster pulses provides a reason why nanosecond pulses can trigger

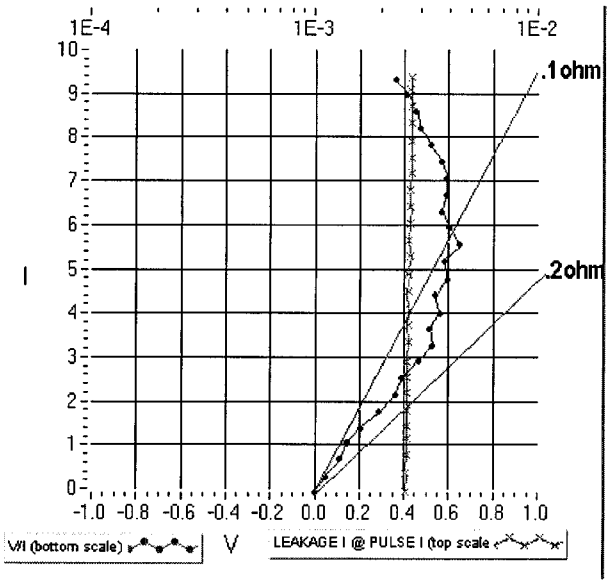

Fig. 12. Measurement using oxidized tungsten needles shorted to a gold disk.

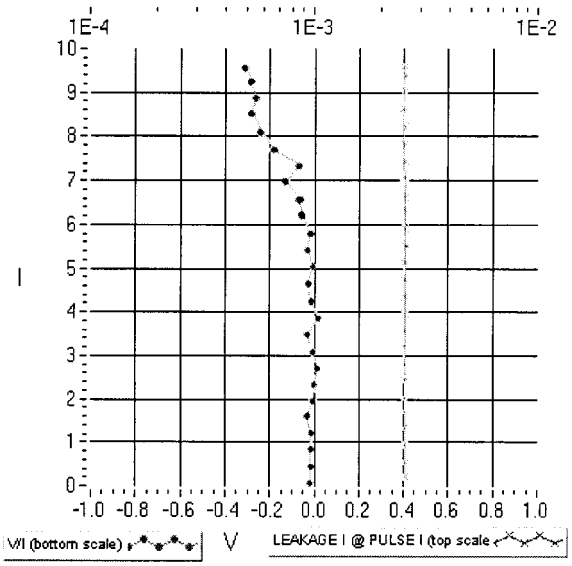

Fig. 13. Measurement of tungsten needles with polished tips shorted to a gold disk.

transient latch-up. If the clamping voltage of a snapback device happens to be below the operating voltage, and the device happens to be sensitive to dV/dt, a fast transient pulse can more readily reach the clamping (or holding) voltage of the protection circuit. With sufficient current, available from power supply circuits, the current can increase and latch-up can occur at a level determined by the internal impedance of both the source and the DUT.

V. Contact Resistance Concerns

When testing on wafer we have found that the oxide on tungsten needles is sufficient to cause a nonlinear I–V error that can be seen on the plot of Fig. 12. This was found because of the ability of an accurate calibrated system to measure fractional ohm parameters with a short pulse curve tracing system. These few ohms of uncontrolled resistance are large errors when trying to measure the protection circuit resistance slope of one to 5 Ω. This error is not seen with metal contacts in sockets and pins of packaged devices. The TLP correction factor described below can be changed depending on the contact resistance, the pad or the internal resistance of the packaged device. The internal short inside a packaged part can be four or more ohms. By using the TLP system to correct for the internal resistance of internal connections (shorts), the bond lead and other internal conductor resistance can be mathematically removed or analyzed. This allows the resistance of the silicon device itself to be measured; the same as if it were still on a wafer and the needles were directly contacting the pads.

Fig. 12 shows such an error from tungsten that has oxidized for about 24 h. Tenacious tungsten oxide on needle points and on their shanks can cause very random increases in contact resistance. Fig. 13 shows the short calibration with tungsten needles contacting a solid gold (10 mil thick) short. The tungsten needles have had their tips polished with a very fine Al_2O_3 abrasive stone, and the shanks cleaned with Carborundum cloth. It still shows some voltage variations from the vertical line that is desired from a good short.

Osmium tip needles on the same 10 mil thick gold disk produce I–V curves that are identical with Fig. 13. These platinum group metal tip needles have not shown any oxide problems when contacting pads on a wafer. Keeping the errors of contact resistance to less than 0.4 volt up to 10 amps is therefore possible with TLP testing on wafer. Osmium tip needles eliminate the variable tungsten oxide resistance that is inevitably present when making short pulse TLP testing. An additional value in using osmium tips is that it is about twice as hard as tungsten and will retain its sharp point much longer.

VI. TLP Standard Test Method

It is becoming obvious that specifying the accuracy of TLP systems is needed to provide better I–V data that the designer can rely on. Because of the tremendous interest in TLP and its growing use, specific calibration information will also be a defining factor of value when TLP data is published. It is our expectation that a "standardized" method of calibrating TLP systems can be instituted for this purpose.

When collecting TLP data, it is important that the pulse width and rise times are specified. We have shown data and made reference to the many publications which have indicated that some measure of correlation can be achieved when the TLP pulse energy is comparable with that of the HBM pulse. We have also shown data and made reference to publications where correlation with HBM depended on the selected TLP rise time. Therefore, the test pulse length and rise time must be specified when collecting TLP data or reporting on TLP test results.

A simple but effective measurement of TLP accuracy and repeatability can be made by calibrating the system with a combination of 0 Ω, $\infty\,\Omega$, and 5 Ω test resistors. This calibration technique is used with high accuracy microwave network analyzers and is called the short, open, load (SOL) method. The

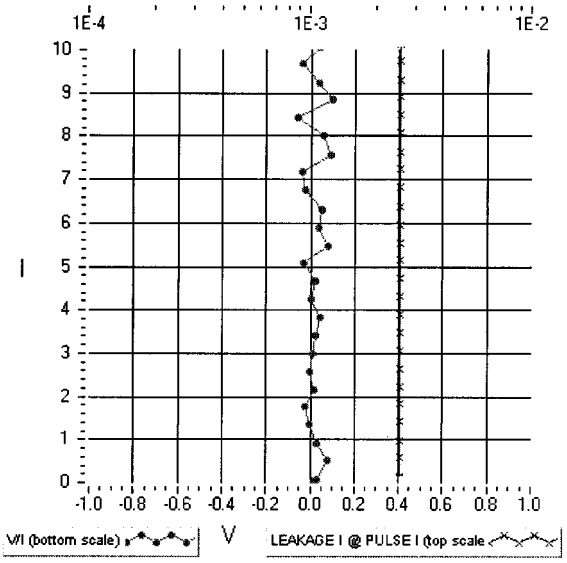

Fig. 14. Short verification for TLP systems.

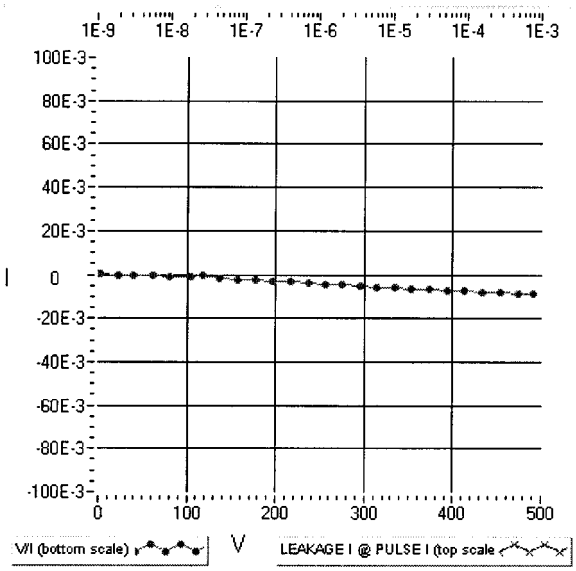

Fig. 15. Open verification for TLP systems.

minimum calibration and verification of the TLP system should use the 0 Ω, and the ∞ Ω resistors. We include a software correction in the analysis software to remove the series resistance losses of the of the test system, including the current probe. This enables an I–V plot of a short circuit for either a socket or a wafer probe to provide the short data as shown in Fig. 14. A perfect short circuit (0 Ω) will have a perfectly vertical line with no voltage variations. The amount of a voltage variation in the plot of a short circuit is a measure of the short circuit measurement error [26].

Including another correction to remove the shunt resistance of the test system in the data presentation and analysis software shows the corrected open circuit plot in Fig. 15. The amount of current variation in the plot of an open circuit is a measure of the open circuit measurement error [26]. A perfect open circuit will have a perfectly horizontal line with zero current.

Once the corrections are applied, any resistor measured with these corrected values will then plot its resistance slope as shown with a 5.09 Ω resistor in Fig. 16. Measuring the slope of a 2 or 5 Ω resistor will provide data for each system near the values expected for many or most ESD protection structures. Any variation from the actual resistance is another measure of the system error. Specifying these calibration characteristics can be an excellent starting point for a TLP standard test method or standard test practice.

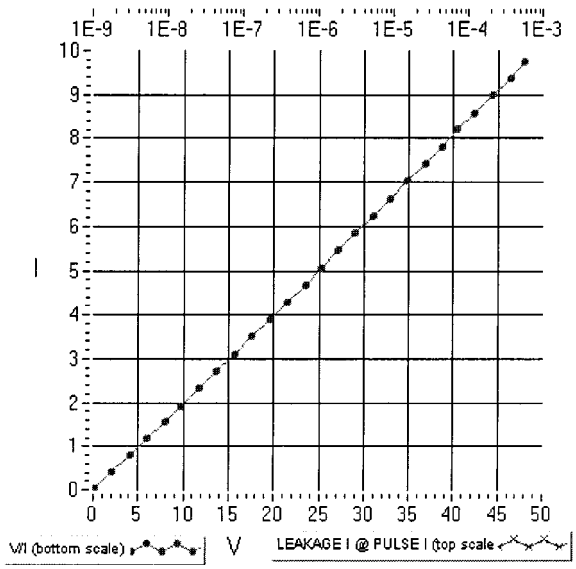

Fig. 16. The 5 Ω verification for TLP systems.

VII. Summary

This paper explained the value of combining into one display, the calibrated TLP I–V plot with the in situ measured leakage current evolution. It explained the benefits of using an integral DC leakage monitor, which measures the in situ leakage current during TLP testing after each test pulse. This allowed the accurate and immediate analysis of both characteristics during the test procedure. We discussed how this in situ leakage measurement data can be used to identify early (soft) failures before the catastrophic failure point I_{t2} occurs.

We have shown that the test pulse rise time is very important when trying to correlate TLP and HBM data especially when ESD protection circuits have dV/dt sensitivities. We reported data showing the correlation between TLP and HBM failure levels. We were able to show that using a range of different TLP rise time test pulses allowed the measurement of the I–V characteristic dv/dt sensitivity. We conclude that while different circuits have different sensitivities to this parameter, it must be considered for each circuit.

We provided information on our discovery of the inherent nonlinear, nonrepeatable contact resistance effect of the oxide that forms on tungsten needles. We have shown that changing from tungsten to oxide free osmium tip needles improves the measurement precision of TLP measurements. This allows greater accuracy when measuring the low dynamic resistance of ESD protection structures.

We described the value of using a pair of balanced wafer probes for accurate TLP testing on wafer. We demonstrated that using dual balanced wafer probes minimizes displacement currents from circuits to the grounded chuck of a wafer probe station. This allows TLP testing on wafer to more closely simulate TLP testing of packaged devices.

We used controlled 0.2 ns, 2.0 ns, and 10.0 ns Gaussian shape rise time pulses, to give a complete rise time range to provide dV/dt information for the designer as well as HBM correlation.

We also provided a simple calibration technique, the SOL test, that can be used for a TLP standard test method or standard practice.

VIII. Conclusions

The calibration of TLP systems provides ESD designers with a better electrical analysis tool because of its improved accuracy. The TLP-50 system been shown to provide improved measurement accuracy characteristics and to provide the addition of in situ leakage current measurements. Including the leakage evolution plot adds another analysis tool to this testing method without which indication of an early failure can be missed. This paper demonstrated how to measure the complete system performance, how to calibrate it, and how to define the accuracy of any TLP system. It is the authors' opinion that the information provided here can be used as a starting point for developing a standard test method or a standard practice for TLP.

IX. Future Work

Controlled dV/dt factors are even more critical in CDM protection. There are CDM type TLP systems under development to study CDM protection design principles. A CDM type TLP test system will benefit greatly from a constant 50 Ω impedance construction because of the ability to transfer test pulses to the DUT with minimum distortion. This will probably be the only construction method capable of providing well defined sub-nanosecond risetime, and short, one to four nanosecond duration, pulses needed for CDM measurements and data analysis. Carefully controlled test pulses are needed for accurate CDM simulation to exercise the protection structures, measure their I–V response, and their immunity to short threat pulses at amplitudes greater than 10 amps

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Jon E. Barth (M'60) received the B.S. degree in electronic engineering from Valparaiso Technical Institute, Valparaiso, IN, in 1959.

After early experience in electronic test equipment design and RF power measurement hardware design at Goodyear Aircraft and Bird Electronics, he founded Barth Electronics, Boulder City, NV, in 1964. As Chief Engineer for 35 years since then, his company has developed over 100 standard products that are in daily use for high voltage, sub-nanosecond pulse diagnostics. Barth products have become known world wide as the standard for reliable HV fast pulse measurements. His attenuators and pulse generators were designed primarily for Livermore, Los Alamos, and Sandia government laboratories and the underground nuclear testing program in Nevada. In 1994, he redirected the efforts of Barth Electronics to transfer the technology developed for weapons testing, into the manufacture of new ESD test equipment, with a goal of manufacturing improved commercial ESD test equipment. He has been a Technical Consultant to the ESD Standards Committees of Working Groups 5 and 14. He has actively assisted in measurement sessions by supplying test equipment and special hardware for fast pulse current and radiation measurements.

Mr. Barth is a member of APS and the EOS/ESD Association.

Koen Verhaege received the M.Sc. degree in electrical and mechanical engineering from the University of Leuven, Belgium, in 1991.

He authored about 20 peer-reviewed published articles in the field of on-chip electro static discharge (ESD) protection and testing and has written about 15 ESD protection design patents (issued, pending and disclosed). He has recently been appointed as Executive Director of Sarnoff's international subsidiary, Sarnoff Europe.

Mr. Verhaege received five international awards for his contributions in the field of ESD.

Leo G. Henry (M'99) received the B.Sc. and M.Sc. degrees in physics from the University of the West Indies and the M.S. and Ph.D. degrees in materials science and engineering from the University of California, Berkeley.

He is presently working in the areas ESD and TLP testing. From 1983 to 2000, he worked in the areas of device failure analysis, reliability, ESD control, and ESD/EOS/latchup. He has authored/published over 21 papers in conferences, symposiums, and refereed journals in the areas of materials science, EOS, ESD, and failure analysis.

Dr. Henry is a member of the ESD Association and the Silicon Valley EOS/ESD Society.

John Richner received the B.S. degree in electronic engineering from Northern Arizona University, Flagstaff, in 1982.

He spent five years performing circuit and software design on engineering development flight simulators at the McDonnell Douglas Aircraft Company where he also chaired a committee for implementation of new electronic production test equipment. Over the past 14 years at Barth Electronics, Boulder City, NV, his work has included the design and manufacture of high reliability, high voltage-high speed pulse generation, and instrumentation products. These products have become standards that are used worldwide for high voltage picosecond pulse generation and diagnostics. Latest efforts include the design and refinement of the Barth Pulse Curve Tracer, Model 4002-TLP.