Tolerance Band Modulation Methods for Modular Multilevel Converters

Arman Hassanpoor, Kalle Ilves, Staffan Norrga, Lennart Ängquist, Hans-Peter Nee
ROYAL INSTITUTE OF TECHNOLOGY (KTH)
Teknikringen 33, 10044
Stockholm, Sweden
Tel.: +46 / (8) – 7906000
Fax: +46 / (8) – 75211793
E-Mail: arman.hassanpoor@ee.kth.se
URL: http://www.kth.se

Keywords

HVDC, Voltage Source Converter (VSC), High voltage power converters, Switching losses

Abstract

Modular multilevel converters (M2C) are increasingly used in the high voltage direct current (HVDC) systems. The efficiency of M2C is highly related to the modulation technique which determines the switching frequency and capacitor voltage ripple in the converter station. A new approach to modulation of M2C is presented in this paper. Tolerance band methods are employed to obtain switching instants and also cell selection. The proposed methods overcome the problem with magnitude modulation for converters with few numbers of cells and also reduce the sorting efforts for cell balancing purposes while maintaining the cell voltage limits. The evaluation is done by time-domain simulation with which the performance of each method is studied in both steady-state and transient cases. It is observed that using tolerance band methods can not only reduces the switching frequency but also handle sever fault cases in a grid connected system. Using this method can reduce the switching losses and also the cell size by optimizing the capacitor design for a fixed ripple.

Introduction

Modular multilevel converters (M2C) are becoming more widely used in power system applications, such as high voltage direct current (HVDC) transmission [1]-[3], flexible alternating current transmission systems (FACTS) and electric railway supply [4]-[5]. Compared with two- and three-level converters, M2C has smoother output voltage and much lower power losses because of reduced switching frequency. However, it requires more a complex control system and more advanced modulation strategies.

Several modulation methods have been presented based on carrier-based pulse width modulation [6], space vector modulation (SVM) [7] and nearest level control (NLC) [8] but ongoing research continuously attempt to introduce more efficient methods to reduce the switching frequency in the system. A modulation method should also balance the cell capacitor voltages. The capacitor voltages can be controlled either by employing a sorting method [7] or cell voltage feedback [6]. Both methods have advantages and disadvantages in different applications. Ranking hundred of cell voltages during a small time-step is problematic, and feedback control may restrict the implementation of advanced modulation methods.

This paper focuses on these contradictory requirements and proposes a novel method based on a tolerance band control. This is a thoroughly new approach in M2C low-level control by which not only the switching frequency is reduced, but also the sorting actions are only performed few times in each cycle. Therefore, the control system requirements are reduced in comparison with the conventional sorting methods.

The paper is divided in four parts. A description of M2C is given in first part. Second part provides a detailed description of the proposed method for voltage tolerance band control, and also cell selection algorithms. Simulation results are presented in third part and finally, conclusions are drawn in last part.

Description of M2C

Modular Multilevel Converter Topology

The schematic three phase M2C topology is shown in Fig. 1a. Three-phase converter is connected to the alternating current (AC) grid through a transformer. The point of common coupling (PCC) is highlighted in Fig. 1a. The Each phase of converter contains two arms and each arm has N number of series connected cells along with a phase inductor. As is shown in Fig. 1a, each cell consists of a capacitor (C) and two semiconductor switches (S_{i1} and S_{i2}). Controlling the turn on/off of the semiconductor switches shapes the AC and DC voltage in the desired way. When S_{i1} is in the on-state and S_{i2} is in off-state, the cell is inserted and the cell capacitor voltage, $V_c(i)$, will vary depending on the arm current. On the other hand, when S_{i1} is in the off-state and S_{i2} is in the on-state, the cell is bypassed and the cell capacitor voltage remains constant. Hence, the generated AC voltage depends on the switching pattern. As discussed in [9], the cell capacitor voltage ripple, the semiconductor switching losses and the output voltage quality are contradictory aspects of M2C operation, which need to be controlled by proper modulation strategies.

Equivalent Circuit

Each converter arm can create discrete voltage levels between zero and V_{dc} in $V_c(i)$ steps. Since each arm includes tens or hundreds of levels, it can be assumed that each arm is corresponding to a variable voltage source. Accordingly, the equivalent circuit of one phase system is defined in Fig. 1b. The voltage V_{arm} is the instantaneous value of the ac-side voltage imposed by the cells. The two parallel connected inductors L_{arm} indicate the arm inductors, which from the ac- side appear to be connected in parallel. L_T is sum of the transformer leakage reactance and any other reactance between the converter and the grid. Resistive losses are also gathered in one resistance, R_T, for transformer and grid side while R_{arm} is the converter arm resistance. Hence, the equivalent circuit consists of two voltage sources that are connected through an inductance L_{eq}, and a resistance R_{eq}, which are given by

$$L_{eq} = \frac{1}{2}L_{arm} + L_T \tag{1}$$

$$R_{eq} = \frac{1}{2}R_{arm} + R_T. \tag{2}$$

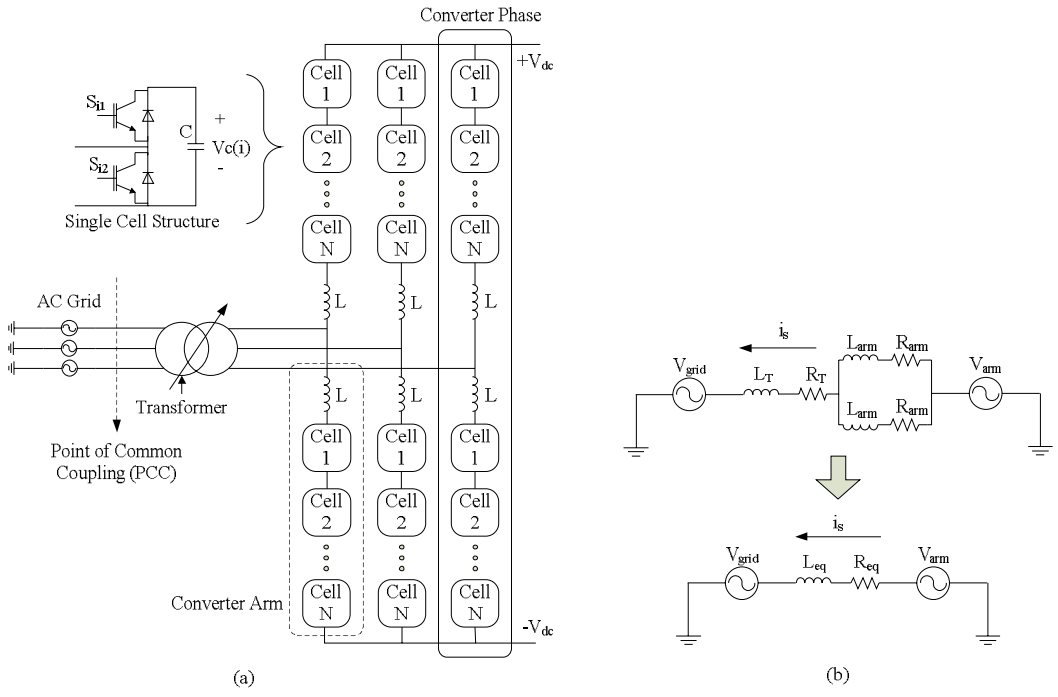

Fig. 1: (a) Three-phase schematic of M2C, (b) Equivalent circuit

Method Description

An overview of the proposed methodology is shown in Fig. 2a. A desired reference voltage (v_{ref}) is generated by the converter high-level control. The low-level control then produces the firing pulse pattern for each individual cell. As proposed in [9], the modulation strategy can be decoupled from the cell selection. The modulation part continuously determines the number of inserted cells (N_{level}) and a cell selection method chooses the cells to insert/bypass to balance the cell capacitor voltages. In this section, novel methods, based on tolerance band control, are proposed for the modulation, as well as the cell selection parts.

Voltage Tolerance Band Control

The calculation in this section is based on the equivalent circuit in the previous part, Fig. 1b. The relation between the voltages and the current, i_s, is then given by

$$v_{arm} - v_{grid} = R_{eq} i_s + L_{eq} \frac{di_s}{dt} \tag{3}$$

consequently,

$$L_{eq} i_s = \int (v_{arm} - v_{grid} - R_{eq} i_s)\, dt \tag{4}$$

that is, the voltage integral (flux) as given by

$$\psi_{eq} = \int (v_{arm} - v_{grid} - R_{eq} i_s)\, dt. \tag{5}$$

The tolerance band should keep the flux within $\pm\delta$ of its desired value, that is

$$\psi_{dif} = \psi_{eq} - \psi_{req} \tag{6}$$

where ψ_{dif} is the differential flux, ψ_{eq} is the equivalent flux and ψ_{req} is the requested flux. The value of ψ_{eq} can be calculated by (5). However, in order to know the value of ψ_{dif}, the requested value ψ_{req} must be known as well. If the reference to the controller is a current, the value of ψ_{req} is given as a reference value. However, if the reference is a voltage, v_{ref}, the corresponding ψ_{req} must be calculated as

$$\psi_{req} = \int (v_{ref} - v_{grid} - R_{eq} i_s)\, dt. \tag{7}$$

Substituting (5) and (7) in (6), instantaneously defines the difference between the desired flux and the actual flux as

$$\psi_{dif} = \int (v_{arm} - v_{ref})\, dt \tag{8}$$

which needs be kept in a tolerance band as

$$-\delta < \psi_{dif} < +\delta. \tag{9}$$

The tolerance band control of the voltage can then be implemented as follows:

1. Choose the nearest voltage level
2. If ψ_{dif} is greater than +δ, switch down one voltage level (nearest level that is lower than the reference).
3. If ψ_{dif} is lower than -δ, switch up one voltage level (nearest level that is greater than the reference).
4. If $-\delta < \psi_{dif} < +\delta$, keep the previous switching states.

The principle of the voltage tolerance band control is shown in Fig. 2b. It shows how the flux error (ψ_{dif}) determines the switching instants. The NLC method can control the flux error over the steep initial region of the reference voltage, but it cannot shape the subsequent peak region of the reference

voltage, in the case that the converter has only a small number of cells. Hence, setting an appropriate value for δ can utilize the advantage of NLC for the steep part of the reference voltage. The shown example in Figure 4 indicates that during the peak part N_{level} stays between two voltage levels which will cause a huge error in ψ_{dif} if no switching is performed. However, the voltage tolerance band method overcomes this problem by shaping the peak part of v_{ref} based on the acceptable flux error of δ. Note that the error ratio will vary based on the arm current magnitude but differences in this ratio are not shown in Fig. 2b.

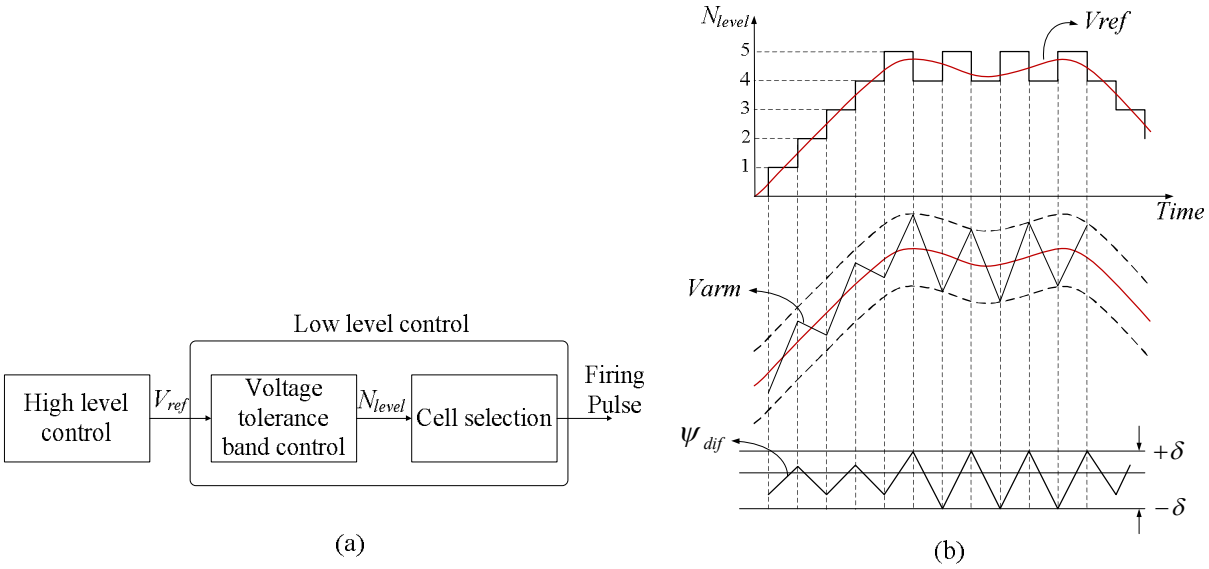

Fig. 2: (a) Control system overview, (b) Voltage tolerance band principle

Cell Selection Methods

As described in the previous section, the required number of levels (N_{level}) is continuously determined by voltage tolerance band control. However, this control does not assign specific cells for insertion or bypassing, and this is the task for a cell selection algorithm. A proper cell selection algorithm keeps the cell capacitor voltages balanced as well as maintaining low switching frequency for each cell. In this paper, three cell selection methods are presented which are also based on tolerance band control. A tolerance band can be set either for each individual cell or for the average of the cell voltages in each arm. Moreover, cell selection methods can either employ a sorting method [7] or a sequential shifting method [10]. Ultimately, all methods generate the switching pulse pattern for a converter arm. Additionally, the cell capacitor voltage is an essential variable which needs to be kept below a certain level; so an upper and lower limit for cell capacitor voltage is defined as V_{max} and V_{min}, respectively.

Tolerance band on cell voltage, employing sorting method (CTBsort)

This method inserts the requested number of cells (N_{level}) according to the sorted list which is created when a cell capacitor voltage goes beyond the upper (V_{max}) or lower (V_{min}) voltage limit. When cell capacitor voltage hits the limit a new sorted list will be generated and this list will be used for the next time steps. The arm current direction decides if the ranking should be done in ascending or descending way. This method reduces the number of sorting actions which is a great advantage from control point of view and also balances the capacitor cell voltages. Fig. 3a illustrates the flowchart for this method. Note that the tolerance band cannot be set less than the peak of the average capacitor voltage. The average capacitor voltage ripple is due to the M2C topology and no switching is involved in this ripple.

Tolerance band on average voltage, employing sorting algorithm (ATBsort)

The average arm voltage can be used as a control criterion for balancing purposes. The sorting action can be performed when cell voltages are exceeding a maximum allowed deviation from the average arm voltage. Cells will be assigned according to the most recent sorted list in each time step. If the current is positive the cell with the lowest voltage gets ranked highest in the sorted list, conversely, if

the arm current is negative, the cell with the highest voltage gets the highest rank. This method ensures that the cell capacitor voltages will not diverge more than δ_r from the average voltage. Fig. 3b shows the ATBsort flowchart. Similar to CTBsort, the tolerance band cannot be set less than the peak of the average capacitor voltage in this method.

Tolerance band on cell voltage, employing sequence reversing method (CTBsequence)

Firstly, two assignment vectors are defined:

$$AM = [\,1, 2, \ldots, N\,] \quad (2)$$

$$AM_r = [\,N, N-1, \ldots, 1] \quad (3)$$

in which N is the number of cells in each arm. The required cells (N_{level}) are selected from the assignment vector AM (1 to N_{level}) or AM_r (1 to N_{level}) while the voltages of all inserted cells are monitored in order to fulfill the cell voltage constraint [V_{max},V_{min}]. If a cell capacitor voltage reaches the upper/lower limit, that cell will be substituted with the first bypassed cell from the assignment vector AM (N_{level} +1 to N) or AM_r (N_{level} +1 to N). Moreover, reversing the assignment vector in every second cycle is proposed for this method, which ensures balanced cell capacitor voltages. Note that this method is only suitable for steady-state operation while transient conditions are not supported. A flowchart of this method is displayed in Fig. 3c. This sequence is carried out by the low level control system in each time step.

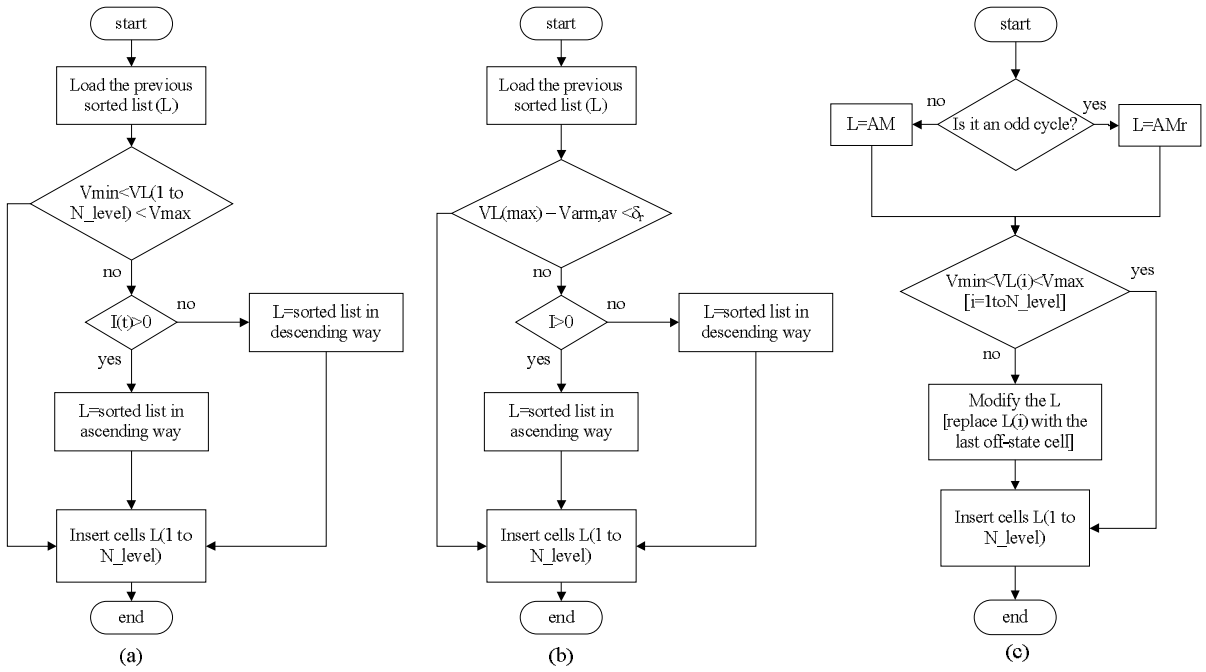

Fig. 3: Tolerance band (a) on cell voltage (CTBsort), (b) on average arm voltage (ATBsort) employing sorting method, (c) Tolerance band on cell voltage employing sequence reversing (L: sorted list, VL(i): voltage level of i^{th} cell, I(t): instantaneous corresponding arm current, δ_r: voltage deviation limit from the average arm voltage)

Simulation Study

Verification of the proposed method has been made through a detailed PSCAD/EMTDC simulation. The simulated system configuration corresponds to Fig. 1a and the parameters are found in Table 1. A third-harmonic zero sequence component was included in the reference voltage waveform to obtain maximum voltage capability. The converter operated with variable switching frequency, depending on the tolerance band, the converter operating point and also the mode of operation (inverter/rectifier). Initially, the performance of voltage tolerance band control is studied and the result is demonstrated in Fig. 5a. It shows how the actual arm voltage follows the reference voltage. Moreover, steady state

simulations were done for the operating points which demands maximum active and reactive power. The steady-state operation results are shown in Fig. 5. Additionally, the dynamic performance of each method is studied through three different transient cases and the results are demonstrated in Fig. 6 and 7.

Table I: Circuit parameters used for the simulations

Number of cells in each arm	N	40
Rated active power	P	1 GW
Rated reactive power	Q	300 MVAR
Direct voltage	V_{dc}	320 kV
Alternating voltage	V	400 kV
Rated frequency	f	50 Hz
DC capacitance (equal)	C	N*28 μf
Specified modulation index	M	0.8

Steady-state Operation

Converter stations are normally working in a steady-state condition. In this case, the operating point is almost fixed and there is no significant change in the load current. A normal operating point is used in this study for active power and reactive power equal to 1GW and 300MVAR, respectively. On the other hand, using tolerance band modulation enables the control of cell capacitor voltage which consequently dictates a varying switching frequency. The dependency of switching frequency on tolerance band magnitude is shown in Fig. 4 which includes three different proposed tolerance band methods.

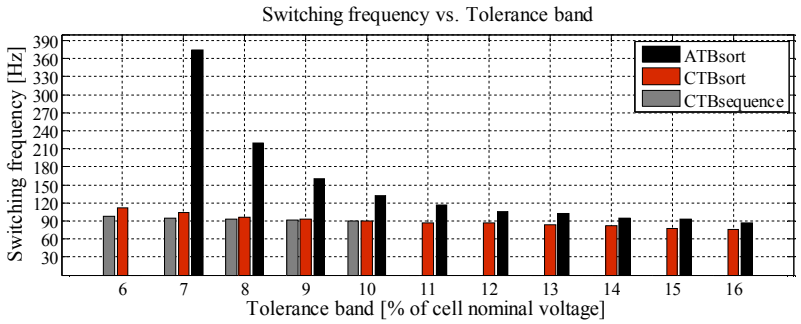

Fig. 4: Switching frequency vs. tolerance band.

Tolerance band on cell voltage, employing sorting algorithm (CTBsort):

As Fig. 5d shows, the capacitor voltages are perfectly balanced with the average switching frequency equal to 90Hz. The maximum allowed cell voltage, V_{max}, is set to 10% above the cell capacitor nominal voltage and the converter is working in inverter mode. Since this method shows very promising results even for dynamic performance tests, a closer shot over the switching frequency vs. tolerance band is shown in Fig. 5c. This figure shows that allowing more ripple in the capacitor voltage ripple can reduce the switching frequency significantly.

Tolerance band on average voltage, employing sorting algorithm (ATBsort):

A tolerance band δ_r equal to 4% of cell nominal voltage is set for this method study. Capacitor voltage ripples are shown in Fig. 5e. It is observed that the resulting average switching frequency is 135Hz for this method. Fig. 5b shows more detail of capacitor voltage ripple around the average cell voltage. As mentioned, there is an inherent capacitor voltage ripple for the M2C topology which is related to the macroscopic power exchange of a phase arm. The peak value of this ripple depends on the converter operating point and the tolerance band cannot be set lower than this value. Consequently, the inherent voltage ripple is 5.5% of the nominal cell voltage even for infinite switching frequency. So, setting

4.5% of tolerance band for δ_r brings a total ripple of 10% which is similar to the tolerance band for other methods studied in this paper.

Tolerance band on cell voltage, employing sequence reversing algorithm (CTBsequence):

The simulation results for CTBsequence method are presented in Fig. 5f. Although capacitor voltages are more distributed with this method, still an acceptable spread is maintained while the average switching frequency is around 90Hz. The tolerance band is set to 10% of the nominal cell voltage. This method does not balance cell voltages actively, hence, if the cell voltages diverge more than 10% of the nominal value, balancing will be lost.

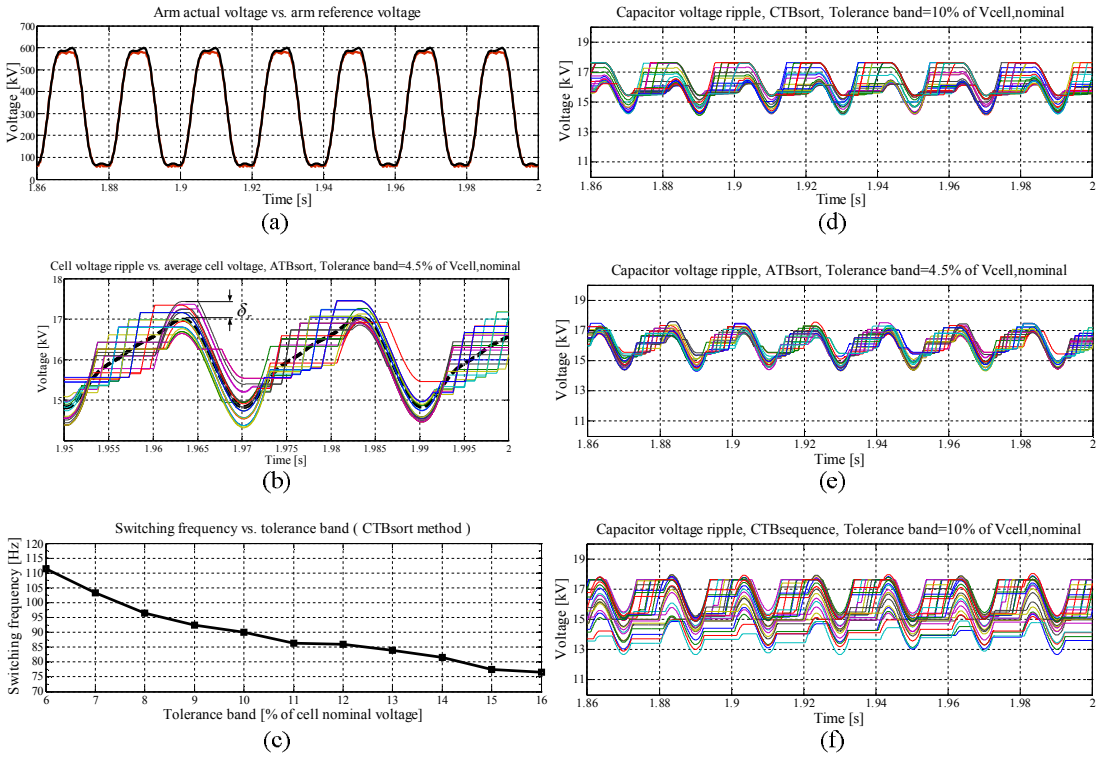

Fig. 5: (a) Actual arm voltage vs. arm reference voltage, (b) Capacitor voltage ripple vs. average voltage ripple for ATBsort, (c) Switching frequency vs. tolerance band for CTBsort method, Capacitor voltage ripple (d) CTBsort, (e) ATBsort, (f) CTBsequence.

Transient operation

Although the converter stations are usually working in normal operating points but they need to tolerate different type of faults such as single/three phase to ground fault, DC faults and etc. on the other hand, the power orders can be changed regarding to the grid requirements and the converter should be able to provide the demanded power. The modulation technique is affecting the performance of the system during all abovementioned transient cases. Hence, the dynamic performance of proposed methods is evaluated in three different cases in this part.

Case 1: Active/reactive power step

A step of -50% is exposed to the active and reactive power order at time equal to 1s. The converter is initially delivering 600MW active power and 200MVAR reactive power while the 50% reduction in order is introduced at time t_1=1s. Fig. 6a demonstrates the step in the active/reactive power. The resulted converter current is shown in Fig. 6b. It is observed that the switching frequency for ATBsort and CTBsequence method simply reduces to 85 Hz while there is a small jump in the switching frequency for the CTBsort method, see Fig. 6c. However, according to the capacitor voltage ripples, shown in Fig. 6d to 6f, all methods are able to maintain the balanced capacitor voltages with a

relatively low switching frequency. The CTBsequence method is not actively maintaining the capacitor voltage balancing, therefore, the V_{max} should be adjusted carefully at step time.

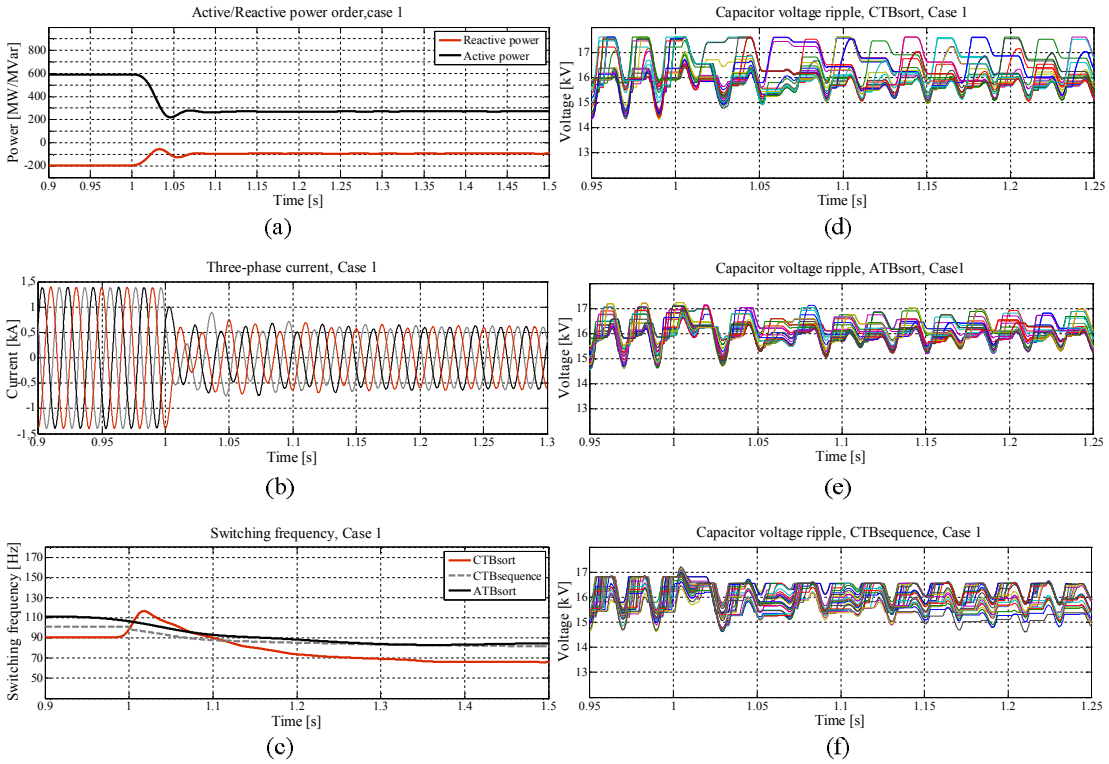

Fig. 6: Transient case 1 (a) Active/reactive power order, (b) Three-phase converter current, (c) Switching frequency, Capacitor voltage ripple (d) CTBsort, (e) ATBsort, (f) CTBsequence.

Case 2: DC-bus voltage step

The DC-bus voltage is initially set to 640kV while a reduction of 5% is introduced at time equal to 1s. The DC-bus voltage reduces to 608kV at this time as is shown in Fig. 7a. It is observed that no changes in switching frequency is applied, Fig. 7b, while the capacitor voltages are still balanced inside the tolerance band. There is an offset change in the capacitor voltage ripples which is shown in Fig. 7c to 7e.

Case 3: Three-phase to ground fault at PCC

A three-phase to ground fault at point of common coupling (AC side) is simulated in this part. The fault is exposed at t_1=1s for 100ms. The fault impedance is selected in a way to have 10% remaining voltage at PCC; Fig. 7f shows the three-phase AC voltage during the fault time. The significant increase in the switching frequency is noticeable for ATBsort and CTBsort method while CTBsequence is not responding to this fault case. This overshoot in the switching frequency is required to maintain the capacitor voltage balancing. The resulted capacitor voltages are demonstrated in Fig 7h to 7j. It shows that active balancing is needed to handle the fault cases otherwise the capacitor voltages diverge, see Fig. 7j. Note that the high level control in this simulation study is not designed for fault cases and the current orders are not responding to the fault current. Although the reference voltage is oscillating significantly, the capacitor voltages can follow the references in CTBsort and ATBsort methods. This primitive high level control explains the high oscillation in the capacitor voltages during the fault interval.

Discussion

Different tolerance band methods are compared for a specific operating point (P=1GW, Q=300MVAR) with respect to the average switching frequency. The trade-off is shown in Fig. 4. Expectedly, setting a tolerance band over the average capacitor voltage (ATBsort) will cause higher switching frequency in comparison to the methods in which a fixed tolerance band is set for each

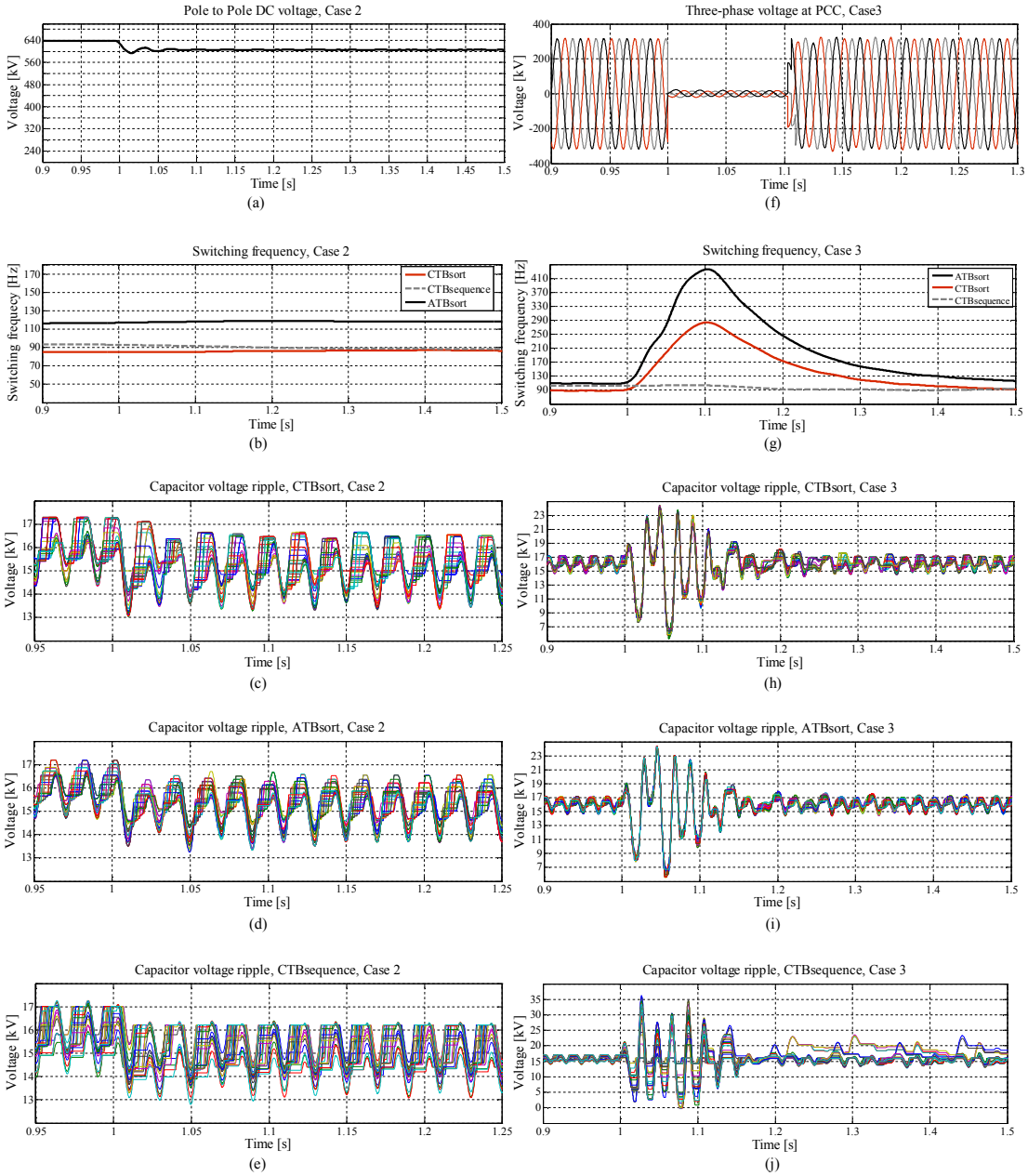

Fig. 7: Transient case 2 (a) pole-pole DC voltage, (b) switching frequency, Capacitor voltage ripple (c) CTBsort, (d) ATBsort, (e) CTBsequence; Transient case 3 (f) PCC three-phase voltage, (g) switching frequency, Capacitor voltage ripple (h) CTBsort, (i) ATBsort, (j) CTBsequence.

individual cell voltage (CTBsort). CTBsort allows more spread in cell voltages in each arm whereas ATBsort will force cell voltages to not differ more than δ from the average cell voltage, so more switchings are needed in order to keep all cell voltages around the cell average voltage. However, the switching frequency is decreasing by increasing the tolerance band for all proposed methods. Notably, the tolerance band modulation technique is routinely adjusting the switching frequency based on the converter operating point. It tries to use the available capacitance of the cell capacitor and consequently reduces the switching actions. Setting a fixed tolerance band over the nominal cell voltage (e.g. CTBsort) allows all cell capacitors to be charged and discharged to a pre-determined level, so, a full capacitance are used in all instances for this method. As a result, the average switching frequency is not affected for CTBsort method in the case of un-evenly distributed capacitors through the cells. If the capacitance of the cell capacitor is reduced due to the aging, that cell will be charged and discharged relatively faster that other cells but the average switching frequency and system performance is not affected. However, setting a tolerance band over the average cell voltage (e.g.

ATBsort) keeps track of the capacitor voltage range not the individual cell voltage. It means that the full capacitance of the cell capacitor is not used in all instances. Therefore, in the case of capacitor aging, the cells with lower capacitance are charging/discharging faster and introduce more sorting actions which will cause higher switching frequency.

Conclusion

This paper presents a new approach to M2C modulation based on the tolerance band concept. A voltage tolerance band method is proposed to determine the number of inserted cells. Furthermore, three methods are introduced for cell selection, labeled CTBsort, ATBsort and CTBsequence. The tolerance band methods lead to variable switching frequency operation of the converter. The switching frequency varies depending on the converter operating point, the conversion mode and the tolerance band. For the selection methods it is found that, the ATBsort method brings excellent voltage balancing by updating the sorted list more frequently, but consequently requires a more complex control system. On the other hand, CTBsequence demands a less complex control system since no sorting action is employed, but it can only be applied in steady-state operation. Finally, the CTBsort method can reduce the average switching frequency to 90Hz for P=1GW, Q=-300MVAR and 70Hz for P=300MW and Q=-100MVAR, while the capacitor voltage ripple is limited to 10% of the nominal cell voltage. This represents a significant improvement in the converter performance by having a relatively low switching frequency, few sorting actions in each cycle, and keeping the cell capacitor ripple in a fixed range. A detailed study on the dynamic performance of the proposed methods also shows how CTBsort and ATBsort methods can handle the transient cases such as power step, DC-bus voltage step and fault cases. Furthermore, the performance of the proposed method of CTBsort is not affected by un-even distributed capacitor through the arm cells which is a prominent benefit from practical point of view.

References

[1] R. Marquardt, “Modular multilevel converter: a universal concept for HVDC-Networks and extended dc bus-applications,” Proc. of IEEE International Power Electronics Conference, IPEC ECCE Asia, Japan, June 2010.

[2] N. Ahmed, A. Haider, D. Van Hertem, L. Zhang, and H.-P. Nee, “Prospects and challenges of future HVDC SuperGrids with modular multilevel converters,” Proc. of EPE 2011, Birmingham, UK, 30 Aug.-1 Sept. 2011.

[3] S. Allebrod, R. Hamerski, and R. Marquardt R, “New transformerless, scalable modular multilevel converters for HVDC transmission,” Proc. of IEEE Power Electronics Specialists Conference (PESC), Rhodes, Greece, June 15-19, 2008.

[4] M. Winkelnkemper, A. Korn, and P. Steimer, “A modular direct converter for transformerless rail interties,” in *Proc. IEEE ISIE*, 2010, pp. 562–567.

[5] L. Ängquist, A. Haider, H.-P. Nee, and H. Jiang, “Open-loop approach to control a modular multilevel frequency converter,” Proc. of EPE 2011, Birmingham, UK, 30 Aug.-1 Sept. 2011.

[6] M. Hagiwara and H. Akagi, “Control and experiment of pulsewidth-modulated modular multilevel converters,” *IEEE Transactions on Power Electronics*, Vol. 24, Issue 7 2009, pp. 1737-1746.

[7] A. Lesnicar and R. Marquardt, “An innovative modular multilevel converter topology suitable for a wide power range,” Proc. of IEEE PowerTech, Bologna, Italy, June 23-26, 2003.

[8] S. Kouro, R. Bernal, H. Miranda, C. A. Silva, and J. Rodriguez,“High-performance torque and flux control for multilevel inverter fed induction motors,” *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2116–2123, Nov. 2007.

[9] A. Hassanpoor, S. Norrga, H.-P. Nee, L. Angquist, "Evaluation of different carrier-based PWM methods for modular multilevel converters for HVDC application," *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society* , vol., no., pp.388,393, 25-28 Oct. 2012.

[10] K. Ilves, A. Antonopoulos, S. Norrga, H.-P. Nee, “A new modulation method for the modular multilevel converter allowing fundamental switching frequency,” *International Conference on Power Electronics - ECCE Asia 2011*, Jeju, Korea, June 2011.