# Top–Down Fabrication of Gate-All-Around Vertically Stacked Silicon Nanowire FETs With Controllable Polarity

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***Abstract*—As the current MOSFET scaling trend is facing strong limitations, technologies exploiting novel degrees of freedom at physical and architecture level are promising candidates to enable the continuation of Moore's predictions. In this paper, we report on the fabrication of novel ambipolar Silicon nanowire (SiNW) Schottky-barrier (SB) FET transistors featuring two independent gate-all-around electrodes and vertically stacked SiNW channels. A top–down approach was employed for the nanowire fabrication, using an e-beam lithography defined design pattern. In these transistors, one gate electrode enables the dynamic configuration of the device polarity (n- or p-type) by electrostatic doping of the channel in proximity of the source and drain SBs. The other gate electrode, acting on the center region of the channel switches ON or OFF the device. Measurement results on silicon show $I_{on}/I_{off} > 10^6$ and subthreshold slopes approaching the thermal limit, SS $\approx$ 64 mV/dec (70 mV/dec) for p(n)-type operation in the same physical device. Finally, we show that the XOR logic operation is embedded in the device characteristic, and we demonstrate for the first time a fully functional two-transistor XOR gate.**

***Index Terms*—Ambipolar transistor, Bosch process, double-gate, dual-gate, e-beam lithography, gate-all-around (GAA), polarity control, silicon nanowire (SiNW), top-down fabrication, XOR logic gate.**

## I. Introduction

BULK CMOS technologies are predicted to face crucial technological challenges in the next decade. At the same time, novel devices such as Silicon nanowire field-effect transistors (SiNWFETs) and Carbon nanotube field-effect transistors (CNTFETs), which do not suffer from the same constraints, are receiving increasing attention due to their promising characteristics, such as quasi-ballistic transport, steep subthreshold slopes and 1-D channel geometry [1], [2].

Manuscript received November 5, 2013; revised May 2, 2014 and August 25, 2014; accepted September 30, 2014. Date of publication October 14, 2014; date of current version November 6, 2014. The review of this paper was arranged by Associate Editor I. O'Connor.

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Digital Object Identifier 10.1109/TNANO.2014.2363386

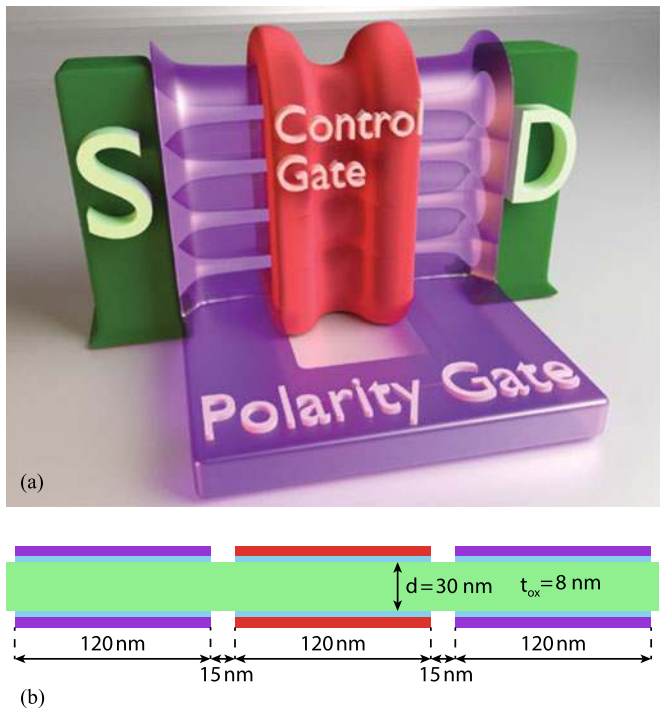


Fig. 1. (a) 3-D view of the complete device. S/D pillars supporting a vertical stack of nanowires are shown in green. The GAA polarity gate, covering the side regions of the channel is shown in violet, while the central control gate is shown in red. (b) Fabricated device dimensions.

Specifically, this paper extends our work on the fabrication of vertically stacked double-gate (DG) Silicon nanowire (SiNW) FETs [3], featuring two gate-all-around (GAA) electrodes (see Fig. 1). Vertically stacked GAA SiNWs represent a natural evolution of FinFET structures, providing the best geometry for electrostatic control over the channel, and consequently, superior scalability properties [4], [5]. In the described device, one gate electrode, the control gate (CG), acts conventionally by bulk switching ON and OFF the channel. The other electrode, the polarity gate (PG), acts on the side regions of the channel, in proximity to the source / drain (S/D) Schottky junctions, switching the device polarity dynamically between n- and p-type. Measured devices show subthreshold slopes of 64 mV/dec and 70 mV/dec, respectively, for the p-type and n-type conduction branches in the same physical device. Moreover, $I_{on}/I_{off}$ values range from $10^6$ to $10^7$, respectively, for the

p-type and n-type conduction branches still in the same device. The applied voltage ranges for the PG and CG are comparable.

Thanks to the compatible CG and PG threshold voltages, these devices can exploit both gates as logic inputs, enabling the design of compact cells that implement XOR more efficiently than in CMOS [6], [7]. Recent works on logic design have shown that using ambipolar DG devices requires fewer resources than the conventional CMOS both using static [8], [9] and dynamic logic [10] approaches. Moreover, implementation of Sea-of-Gate architectures with DG-SiNW devices [11] can reduce fabrication costs by providing efficient circuit implementations and maintaining a high level of regularity in circuit layouts.

Early transistors demonstrating polarity control employed bottom–up fabricated SiNWs [12], [13] and carbon nanotubes [14] as channel material. However, researchers are still encountering difficulties in selection and placement of these structures on the final substrate, these techniques still requiring a technological breakthrough to be employed in current ultralarge-scale circuit integration (ULSI). In this paper, we use a top–down approach to fabricate the SiNWs from a lithographically defined mask, enabling large-scale fabrication of arrays of vertical stacks of nanowires, without requiring complex transfer procedures of pregrown nanowires on a final substrate.

This paper is organized as follows: Section II is an overview on the transition from bulk MOSFETs to GAA-NWFET devices. Section III presents the proposed device structure and details on its fabrication. Section IV presents characterization results and introduces a TCAD model of the device. Section V shows some measured logic circuits built with our devices and presents some performance evaluation using the device TCAD model. Finally, Section VI discusses some future improvements and directions of this paper and Section VII concludes the paper.

## II. Background

In recent years, the trend toward device miniaturization, aimed at increasing performance while reducing variability and circuit power consumption, has led to the introduction of 3-D device channel structures, such as the two-gate, Ω-gate, and FinFET transistors [15]. These increasingly sophisticated channel geometries enhance the electrostatic control of the gate over the device channel, reducing short channel effects (SCEs) [1], [16] and allowing more aggressive scaling of the device dimensions. If we further optimize the channel geometry, we obtain the nanowire FET, with a GAA electrode wrapped around the nanowire surface. This geometry maximizes the surface to volume ratio of the channel to gate interface, thus optimizing the channel electrostatics [17], [18]. Devices with this geometry reach high $I_{\rm on}/I_{\rm off}$ ratios and steep subthreshold slopes ($SS$) approaching the thermal limit of $\sim 60$ mV/dec.

However, another challenge at and below the 22-nm technology node is the fabrication of abrupt chemical doping profiles. Specifically, devices' active regions at these technology nodes may contain 100 or less dopant atoms, and variations of even small percentages may result in faulty circuit applications. As an alternative to chemically doped transistors, silicide-based

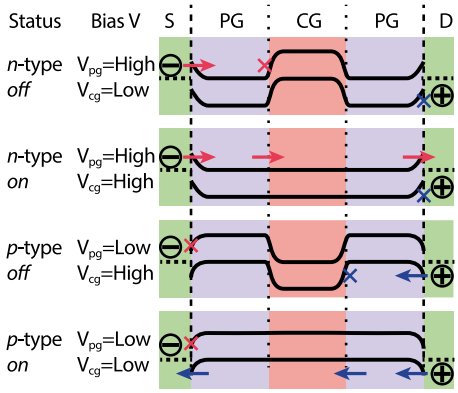


Fig. 2. Conceptual band diagrams for the ambipolar double gate device. Four cases are shown, describing the four combinations of high / low bias for the polarity gate and control gate of the device. Electron paths are shown with red arrows / crosses, hole paths are shown with blue arrows / crosses.

Schottky barrier (SB) CNTFETs [19], [20] and SiNWFETs [21] have been proposed due to their relatively low-temperature processing, simpler fabrication and sharp S/D silicide to channel interfaces [22], [23]. These devices are fabricated by creating two metal or silicide S/D contacts at the sides of a lowly doped or intrinsic channel. Due to the presence of S/D SBs, these devices typically have an ambipolar behavior, showing a superposition of hole and electron transport characteristics. Moreover, $SS$ values in SB devices are very degraded due to the carrier injection through the S/D barriers.

In order to overcome these limitations, devices exploiting a second gate structure (polarity gate) have been proposed [12]–[14]. This second gate acts on the channel band structure in proximity of S/D contacts. Fig. 2 shows a conceptual band diagram of such device for different regions of operation (see Section IV-A). The effect of the PG is to induce an electrostatic doping of the side regions of the channel, allowing only one carrier type through the channel at any given time. As we will further explain in the following sections, this feature not only improves device characteristics and performance, but provides an additional degree of freedom at circuit design level by providing a transistor, which can be polarized at runtime. Specifically, the same transistor structure can be replicated in an array and used to produce logic circuits without the need of separate p and n wells in the circuit layouts. Table I gives an overview of the state-of-the-art of controllable polarity devices. Note that we define *symmetric* a device whose n-type characteristic matches its p-type characteristic in $I_{\rm d}$ current ranges and SS values.

Stimulated by the demonstration of devices which could perform as n- or p-type depending on their bias configuration, various works at circuit design level have focused on exploiting this added configurability. Static [6], [8], [24] and dynamic logic [10], [25] architectures based on configurable devices have shown an advantage with respect to the conventional CMOS by implementing circuits with reduced area occupation and lower delay. Static logic design using DG-FET is particularly attractive, as it is based on the robust complementary logic typical of CMOS, while exploiting the increased expressive power given by DG-FETs, which enable the construction of XOR logic gates

TABLE I
STATE-OF-THE-ART FOR NANOWIRE / NANOTUBE DEVICES WITH FULL / PARTIAL POLARITY CONTROL BY MEANS OF A POLARITY GATE

| Ref. | Device Type | Approach | Device length | Wire diameter | $V_{pg}$ range | $V_{cg}$ range | $I_{on}/I_{off}$ | Subthreshold Slope |
|---|---|---|---|---|---|---|---|---|
| [12] | Single SiNWFET, Ω-gate (CG), Substrate (BG) | Bottom–up | 500 nm (gate) | 40 – 100 nm | −15 V (p-type) −5 V (OFF) | −2 – 2V | ≈$10^7$ (*p*-type) | ≈140 mV/dec (*p*-type) |
| [26] | Single SiNWFET, Ω-gate (CG), Substrate (BG) | Top–down | 28 $\mu$m (channel) 2 $\mu$m (gate) | 60 nm | −10 V – 10 V | −4V (*p*-type) 4V (*n*-type) | ≈$10^6$ (*n*-type) ≈$10^4$ (*p*-type) | ≈80 mV/dec (*n*-type) >2000 mV/dec (*p*-type) |
| [27] | Single SiNWFET, Ω-gate (CG), Ω-gate (BG) | Bottom–up | ≈1 $\mu$m (channel) 220 nm (gate regions) | 20 nm | $V_{pg}=2$ V, $V_d=2$ V (n-type) $V_{pg}=-2$ V, $V_d=-2$ V (p-type) | −2 – 2V | ≈$10^7$ (*n*-type) ≈$10^9$ (*p*-type) | ≈150 mV/dec (*n*-type) ≈150 mV/dec (*p*-type) |
| [14] | Single CNTFET, Ω-gate (CG), Substrate (BG) | Bottom–up | 300 nm (channel) | ≈1.4 nm | $V_{pg}=1.6$ V, $V_d=0.6$ V (n-type) $V_{pg}=-2$ V, $V_d=-0.6$ V (p-type) | −2 – 2V | ≈$10^3$ (*n*-type) ≈$10^4$ (*p*-type) | ≈63 mV/dec (*p*-type) |
| This study | Stacked SiNWs, GAA (CG), GAA (BG) | Top–down | 400 nm (channel) 100 nm (gate regions) | 20 – 30 nm | −1V – 4V (n-type) −4V – 0V (p-type) | −1 – 4V | ≈$10^7$ (*n*-type) ≈$10^6$ (*p*-type) | ≈70 mV/dec (*n*-branch) ≈64 mV/dec (*p*-branch) |

Our device shows a high level of symmetry between n and p operation in terms of $SS$, $I_{on}/I_{off}$ and input voltages, combined with a top–down fabrication approach enabling large-scale integration.

with only four transistors instead of the eight transistors required in the CMOS implementation.

An additional note concerns the fine tuning of device channel width in these novel devices (based on fin or nanowire structures), which is more challenging than in bulk MOSFET technologies. For example, in commercial FinFETs, two full fins have to be employed to obtain a $W = 2$ device. As further explained in Section V-B, DG-FET devices enable shorter *pull-up(down)* network transistor series in the case of binate functions (e.g., XOR), thus further reducing the need of large transistor sizing. Moreover, technology tuning to obtain symmetric p- and n-type characteristics in the same device is also beneficial to the width sizing constraint, producing logic gates with symmetrical output characteristics even when using the same geometrical transistor sizing in *pull-up(down)* networks.

## III. DEVICE STRUCTURE AND FABRICATION

Fig. 1(a) shows the conceptual structure of the fabricated devices. A vertical stack of horizontal nanowires is first fabricated by dry etching of an SOI device layer (shown in green in the figure). These nanowire stacks are sustained by two silicon pillars at the two extremities. The nanowire stacks can be built in a regular and compact fashion by sharing pillars between adjacent transistors (see Section III-B). Note that the presence of two gate contacts along for each device may increase circuit routing complexity. As described in [11], however, this back-to-back transistor structure effectively minimizes routing congestion in complex logic cells. As described in the next section, GAA polarity and control gates (respectively, violet and red in the Fig. 1) are then added to the structure. Finally, nickel is intruded by controlled thermal annealing in the source and drain pillar structures in order to form SBs partially overlapping the side PG regions. In order to enable large scale integration of the devices, the process flow is fully implemented in a top–down fashion, using three e-beam lithography steps.

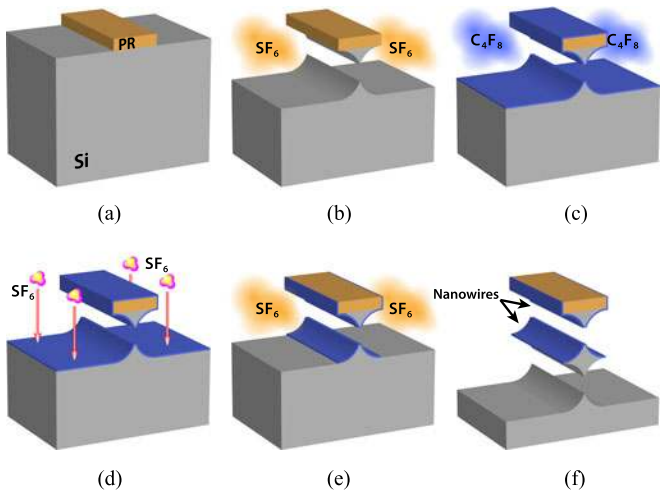


Fig. 3. DRIE applied to nanowire fabrication. (a) Photoresist (PR) mask is applied on crystalline silicon; (b) physical/chemical $SF_6$ etching is applied, creating an undercut below the mask pattern; (c) conformal thin passivation is applied using $C_4F_8$ gas; (d) vertically accessible surface passivation is readily removed by the partly anisotropic $SF_6$ etching; (e) finally, a new undercut is produced by chemical etching by the $SF_6$, leading to (f) new nanowire.

### A. Nanowire Fabrication

The nanowires were fabricated in a top–down fashion, exploiting a single adapted deep reactive ion etching (DRIE) processing step [28], [29] to form the device channels. Originally developed to produce high aspect ratio vertical structures, the DRIE process provides a fast and ULSI compatible method to fabricate nanowire stacks. The process is illustrated in Fig. 3. A Si dry etching step ($SF_6$ plasma) is interleaved with a passivation step ($C_4F_8$ plasma). These two steps are cycled a number of times, ultimately creating a number of horizontal grooves reproducing a photoresist pattern. If the pattern consists of a thin line, around $50 \div 100$ nm in width, the grooves descending from the two sides of the pattern meet, and a vertical stack

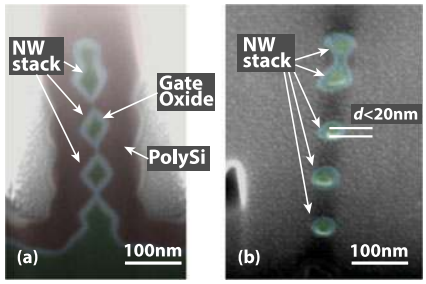


Fig. 4. SEM/FIB cross sections of fabricated devices, showing the (a) nanowire stack with 8-nm gate oxide and 50-nm thick conformal polysilicon GAA structure; and (b) optimized $d < 20$-nm stacked nanowires.

of horizontal nanowires is formed. By changing the number of etching cycles, therefore, the number of nanowires in the stack can be customized. Specifically, in our process, we designed channels consisting of $\sim 350$ nm long vertical stacks of four nanowires on a slightly p-doped ($\sim 10^{15}$ atoms/cm$^3$) SOI substrate. Note that these dimensions were chosen to relax constraints in the subsequent process steps. No process-specific physical constraints would limit device scaling differently than in similar state-of-the-art devices such as FinFETs. Finally, the wires are sustained by pillar structures at both ends, produced by photoresist squares. The pillars act as source and drain contacts for the transistors [in green in Fig. 1(a)] Fig. 4 shows two SEM/FIB cross sections of the nanowire stacks. In Fig. 4(a), rhombohedral shape wires are shown, surrounded by the 50-nm conformal polysilicon gate material. In Fig. 4(b), the DRIE process was optimized to obtain thinner, more round nanowires. Specifically, lower $C_4F_8$ gas flow rate will produce more round wires [29], while the nanowire thickness can be tuned by accordingly reducing the original photoresist pattern. Although the DRIE process has to be tuned for different cases (e.g., to reduce notching when using a SOI substrate), nanowire fabrication reliability is high. We estimate the number of damaged/broken wires to be $\ll 1\%$.

### B. Polarity and Control Gate Formation

After the stacks were formed, a first gate oxide ($\sim$8 nm) was produced by self-limiting oxidation [30] of the nanowires followed by a 50-nm conformal polysilicon layer deposition. A rather thick oxide was deliberately chosen to reduce risk of leakage after the final silicidation step in this first device demonstration. At this point, the polarity gate was patterned all-around the nanowires after e-beam lithography. Fig. 5(a) shows an SEM image of the devices after patterning of the first gate structure. The transistors are fabricated in couples, sharing a S/D pillar. This design was chosen due to its increased mechanical stability in comparison with an isolated device, and its low area occupation when employed to build regular circuit architectures [31]. Hence, a second 8-nm oxidation and 50-nm polysilicon deposition was performed. The CG structure is self-aligned to the PG, and acts on the uncovered center region of the nanowires of Fig. 5(a). As shown in the SEM image in Fig. 5(b), three gated regions are obtained, each approximately $100 \div 120$ nm long and electrically isolated by the CG gate oxidation.

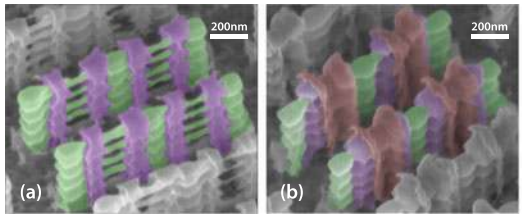


Fig. 5. Tilted SEM views of an array of fabricated devices (a) before creation of the control gates and (b) after addition of the control gates. S/D pillars and nanowires (green), PG (violet) and CG (red) are shown.

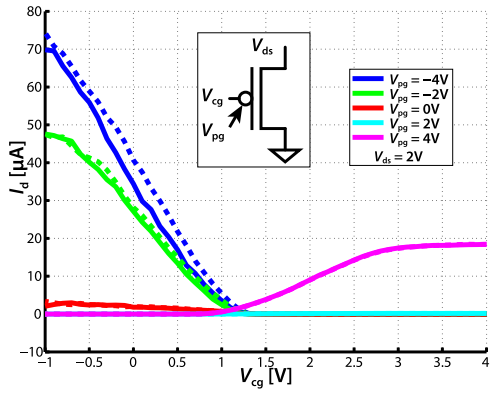


Fig. 6. Linear plot of a measured device. The device connections are shown in the inset. n- and p-type conduction is selected by different $V_{\rm pg}$ biases. Currents in the p-type and n-type branch are comparable. Asymmetry is due to the nonperfectly midgap contact workfunction.

After the formation of the gates, a 25-nm low-stress silicon nitride spacer was deposited conformally and etched anisotropically to isolate the structures. A nickel layer was deposited by evaporation; subsequently, annealing (20′ at 200 °C + 20′ at 300 °C + 20′ at 200 °C) was performed to produce NiSi at the S/D and gate contacts. As further described in Section IV-B, NiSi was chosen as it features a near midgap workfunction with respect to silicon, further providing low interface defects at the NiSi to silicon channel junctions. Finally, unreacted nickel was removed by selective wet etching in hot piranha solution.

## IV. Device Characterization

This section presents electrical measurements showing the device operation at different gate biases. SB height for the nickel silicide contacts at the sides of the nanowire channels is extracted. Finally, a TCAD model of the fabricated devices is introduced and validated against the measured data.

### A. Polarity Control Operation

Polarity control by means of the PG is illustrated in Figs. 6 and 7. Linear and semilogarithmic $I_{\rm d} - V_{\rm cg}$ plots of the same device are provided at different PG biases. As introduced earlier, Fig. 2 presents a band diagram along the device channel, showing the carriers involved in device operation at different CG and PG biases. A positive PG bias allows electron conduction at the S/D SBs, setting the device to n-type, while low PG bias makes holes become the majority carriers, producing a p-type conduction

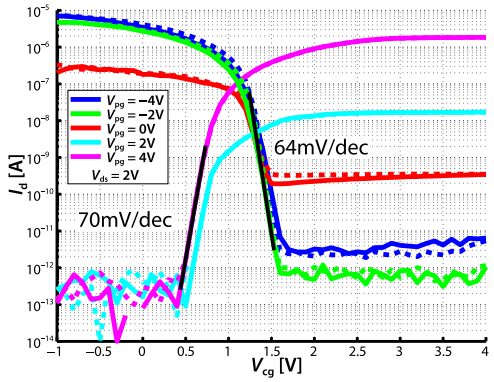


Fig. 7. Logarithmic plot for the same device conditions of Fig. 6. Both n- and p-type device branches show subthreshold slopes $SS \leq 70$ mV/dec. $I_{\rm on}/I_{\rm off}$ ratios of $\approx 10^7$ ($\approx 10^6$) are obtained, respectively, for the n-type (p-type) conduction branches.

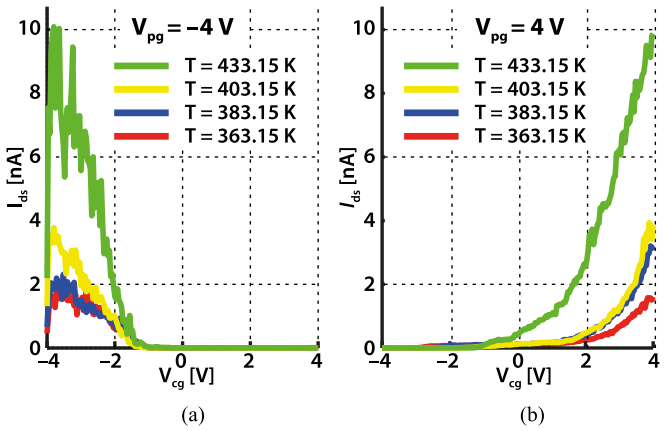


Fig. 8. Selection of the performed measurements at different temperatures, used for SB height extraction, at $V_{\rm ds} = 100$ mV and for (a) $V_{\rm pg} = -4$ V and (b) $V_{\rm pg} = 4$ V. Quasi-symmetric device operation can be observed.

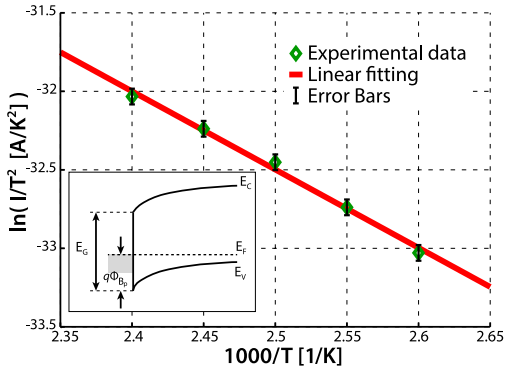


Fig. 9. Arrhenius plot extracted from measurements, some of which are represented in Fig. 8. The linear decreasing slope of the plot, fitted within 5% error in experimental data, indicates thermionic emission regime. $q\Phi_{\rm B_p}$ barrier height of 0.45 eV is observed, confirming that the type of Silicide is compatible with the expected NiSi, whose barrier height value on $p$-Si is ∼0.4 eV. In the inset, energy-band diagram of metal on p-type semiconductor at thermal equilibrium, showing the $q\Phi_{\rm B_p}$ barrier.

scheme. Specifically, in Fig. 2, band bending at the S/D contacts is shown for weakly p-doped silicon nanowires. Subthreshold slopes of 64 mV/dec and 70 mV/dec were obtained, respectively, for the p-type and n-type conduction branches in the same physical device. Moreover, $I_{\rm on}/I_{\rm off}$ values range from $10^6$ to $10^7$, respectively, for the p-type and n-type conduction branches still in the same device. Note that, in this device, we employed materials (NiSi S/D) and low p-doped channel, in order to obtain a crossing between n- and p-type characteristics at $V_{\rm pg} > 0$ V. Specifically, we wanted to obtain a device, which behaves already as p-type for $V_{\rm pg} = 0$ V, while switching to n-type for a low positive $V_{\rm pg}$ (e.g., $V_{\rm pg} = 1$ V to $V_{\rm pg} = 2$ V).

### *B. SB Height Extraction*

Schottky contact barrier height extraction was performed on the device of Fig. 6. Among different techniques used to measure the SB height (i.e., capacitance–voltage, current–voltage, photoelectric method, etc.), we selected the activation energy approach, both for its accuracy and for its independence from the electrically active area. This second aspect makes it particularly well suited to study silicide–semiconductor interfaces. Assuming negligible parasitics resistances, the thermionic emission theory can be applied to the barrier extraction

$$I = I_0 \left[\exp\left(\frac{qV}{\eta k_{\rm BT}}\right) - 1\right]$$

$$I_0 = AA_{0T}^2 \exp\left(\frac{-q\Phi_{\rm B}}{k_{\rm B}T}\right)$$

where $A$ is the contact area of the source to channel junction, $A_0$ the Richardson constant, $q$ the elementary electron charge, $\phi_{\rm B}^0$ the effective SB height, $T$ the temperature, $V$ the applied voltage across the Schottky junction, $k_{\rm B}$ the Boltzmann constant, and $\eta$ the ideality factor.

In Fig. 8, some of the experimental results of $I_{\rm DS}$ current measurements at different temperatures are shown. The linear decreasing slope of the Arrhenius plot in Fig. 9, fitted within 5% error in experimental data with a measured ideality factor $\eta = 1.84$, indicates thermionic emission regime. Near-midgap Schottky ($q\Phi_{\rm B_p}$) barrier height of 0.45 eV is observed, confirming that the type of silicide is compatible with the expected NiSi, whose barrier height value on $p$-Si is $\sim 0.4$ eV. This value is consistent both with the literature and simulation results. In the inset of Fig. 9, the energy-band diagram of metal–p-type semiconductor junction at thermal equilibrium is represented, showing the $q\Phi_{\rm B_p}$ barrier. Compared to previous art (see Table I), our device shows excellent $I_{\rm on}/I_{\rm off}$ and subthreshold slopes, combined with a high degree of symmetry between the n and p conduction branches. Moreover, the device shows a normally p-type ON state, when $V_{\rm pg} = V_{\rm cg} = 0$ V. This is due to the alignment of the S/D metal workfunction to the conduction band of the SiNWs, as shown in the bottom case of Fig. 2, and is achieved using weakly p-doped nanowires. As described in the following sections, this feature enables the fabrication of cascadable logic gates.

### *C. Device Simulation*

After measuring the fabricated devices, we built a TCAD model using the same device architecture. The model was fitted

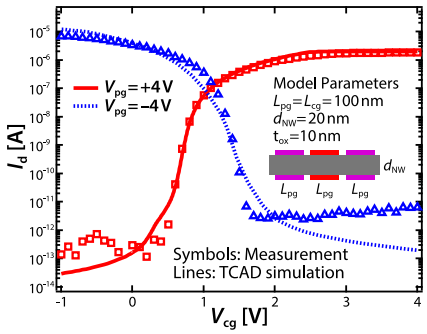


Fig. 10. Comparison between measurement and TCAD simulation by using Synopsys Sentaurus. Good agreement shows the validity and prediction ability of the simulated model and parameters.

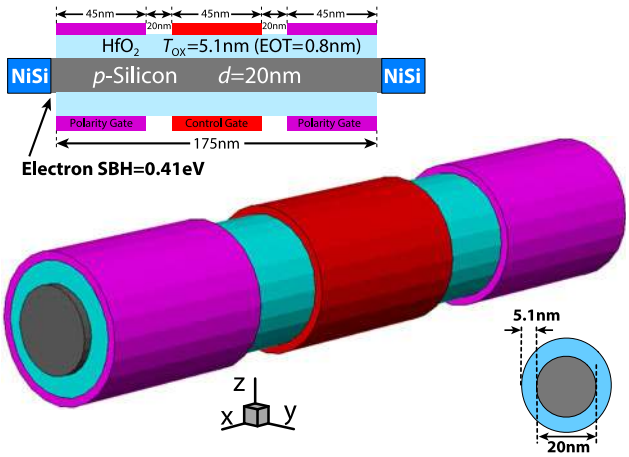


Fig. 11. Structure of the optimized ambipolar Silicon Nanowire device structure with three, 45-nm-long gate regions. High-$\kappa$ gate dielectric and metal gate with midgap workfunction are introduced to predict device performance after tuning of dimensions and materials. SB height $q\Phi_{B_p}$ for electrons is fixed at 0.41 eV at both source and drain.

with experimental results and data from the SB height extraction. Fig. 10 shows the model-based device characteristic in comparison with the characteristic of an experimental device. Good agreement with the measured data is shown. In Fig. 10, the p-type device branch (blue color) shows substantial leakage when $V_{\rm cg} > 2$ V. We attribute this leakage to the lowering of the PG barrier to electron injection at the source electrode due to coupling of the very positively biased CG to the very negative $V_{\rm pg} = -4$ V. This effect can be observed in Fig. 7, where the measurement with $V_{\rm pg} = -2$ V (green line) shows significantly less leakage than the case for $V_{\rm pg} = -4$ V (blue line).

After validating this first model, we built an optimized one by scaling dimensions and introducing technological adjustments to the device structure. The optimized structure includes high-$\kappa$ gate dielectric, metal gates with midgap workfunction and 45-nm-long gate regions. The structure geometry is shown in Fig. 11. SB height $q\Phi_{B_n}$ for electrons is fixed at 0.41 eV at both source and drain junctions. The *I–V* characteristics of the optimized device are shown in Fig. 12, obtained with hydrodynamic transport and quantization models. Tunneling masses for electrons and holes are set to $0.19\,m_0$ and $0.16\,m_0$ respectively, consistent with theory and measurement fitting [32]. Note that

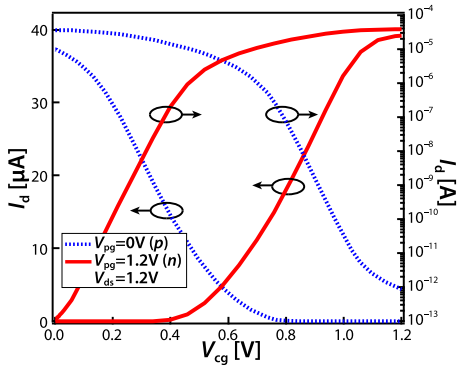


Fig. 12. *I–V* characteristics of the optimized device predicted by TCAD simulation. Symmetric characteristics for n- and p-type operation are observed, respectively, at $V_{\rm pg} = 1.2$ V and $V_{\rm pg} = 0$ V.

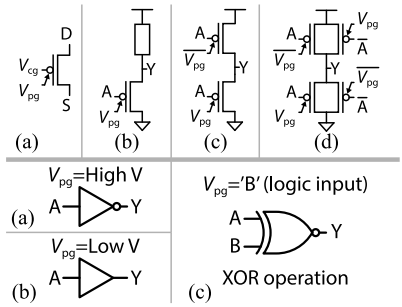


Fig. 13. Logic cell design with DG-SiNWFETs. (a) Circuit symbol for the device. (b) Pseudologic gate with a single device in the pull-down network. (c) Complementary design and (d) complementary design with full-swing output. (A) Operation as an inverter, (B) as a buffer and (C) as an XOR gate.

the cross point between n- and p-type characteristics shifted to a lower $V_{\rm pg} \sim 0.6$ V compared to the nonoptimized model of Fig. 10. In logic circuit design, this would allow the devices to be polarized to n-type at lower $V_{\rm pg}$, consequently allowing the use of lower $V_{\rm dd}$ biases. Section V-C describes a few simulations we performed with this optimized model in order to roughly estimate performance at device and circuit level.

## V. Logic Circuit Demonstration and Simulation

Exploiting dynamic polarity control, reconfigurable logic gates [8] with high expressive logic capability [6] can be implemented with these devices.

### A. Inverter / Buffer Operation

Fig. 13 presents the possible configurations of a logic gate comprising a single transistor in the *pull-down* network [see Fig. 13(b)] or its complementary logic equivalents [see Fig. 13(c and (d)]. Fig. 13(a)–(c) shows how the gate can behave as an inverter or a buffer, whether the *pull-down* transistor is set as n-type or p-type. For example, the measured output signal of an inverter circuit is shown in Fig. 14, where the circuit schematic and applied bias voltages are shown in the figure inset. $V_{\rm dd} = 1$ V is used in this circuit, that presents correct 0–1 V full swing output, with the output transition perfectly centered around $V_{\rm cg} = V_{\rm dd}/2 = 0.5$ V. A slightly negative PG

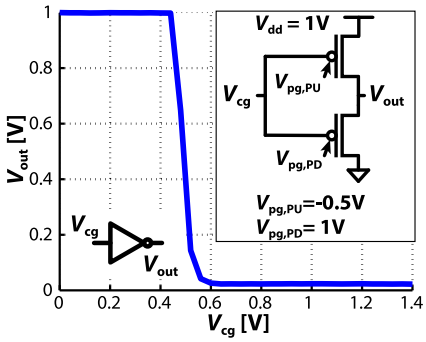


Fig. 14. Measured inverter characteristic obtained by connecting two transistors as shown in the inset. The polarity gates are biased so as to obtain a CMOS-like inverter, with a p-type transistor in the *pull-up* network and a n-type transistor in the *pull-down* network.

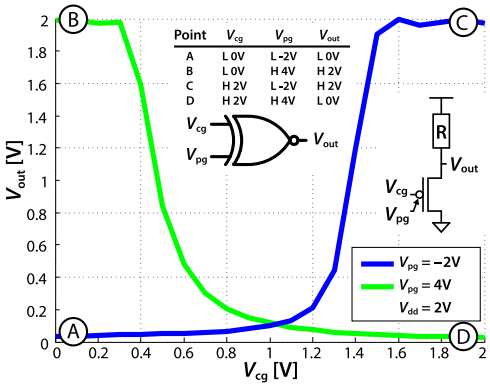


Fig. 15. Pseudologic XOR characteristic obtained using a single ambipolar double gate FET. The device in the *pull-down* network is polarized by means of the PG. In the case of the n-type, the characteristic of a pseudologic inverter is obtained (green). In the p-type polarization, a buffer is obtained (blue). As shown in the inset truth table, overall an XOR function can be implemented with a single transistor.

bias voltage $V_{\rm pg} = -0.5\,{\rm V}$ was chosen to polarize the *pull-up* transistor to p-type. This value results from a tradeoff between using a strongly negative voltage (for better polarization) and a lower voltage, showing that the device is functioning almost in the correct range for multilevel logic circuit compatibility. Note that this value is required to balance the performance of our proof of concept devices. $V_{\rm pg} = 0\,{\rm V}$ can be reached with more optimized transistors, as shown in Section V-C.

### *B. Two-Transistor XOR Operation*

Instead of using the PG bias as a preset configuration signal, this input can be utilized as a second logic variable. In this case, the transistor polarity would be dynamically defined by a logic signal during the circuit operation. As shown in the previous section, such logic gate could act as an inverter or buffer depending on the PG input. Fig. 15(inset) shows a simple pseudologic circuit schematic and truth table produced using a single DG-SiNWFET, where the inverter and buffer operations are activated by different PG input values, ultimately obtaining a XOR logic operator.

However, in order to enable multilevel static logic synthesis with this technology, PG and CG input biases are required to

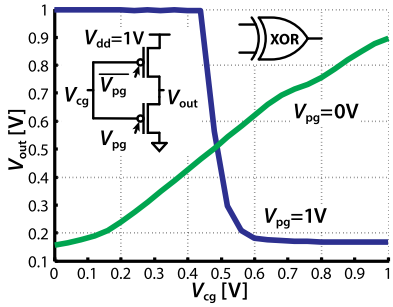


Fig. 16. Output characteristic of a two-transistor complementary XOR logic gate. The functionality of this logic gate is similar to that of Fig. 15. Similar to a two-transistor noninverting gate, the buffer characteristic is degraded due to the presence of poorly polarized n-type FET in the *pull-up* network and p-type FET in the *pull-down* network. Note, however, that control and polarity gate input voltages are compatible with $V_{\rm dd}$ (range from 0 to 1 V), making this gate fully functional for implementing multilevel static logic.

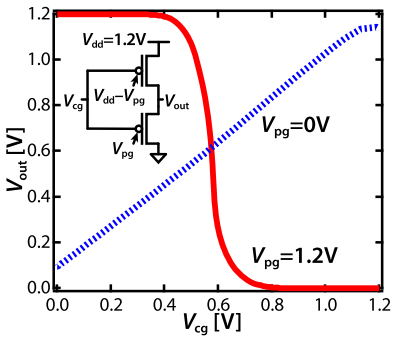


Fig. 17. TCAD simulation of the two-transistor XOR gate built with optimized devices corresponding to the measurement in Fig. 16.

be compatible with $V_{\rm dd}$, i.e., all voltages have to range between 0 V and $V_{\rm dd}$. Fig. 16 shows a measured complementary gate exhibiting this feature. In this case, the output characteristic of the buffer branch is degraded; this is due to the presence of the poorly polarized n-type FET in the *pull-up* network and the p-type FET in the *pull-down* network. Note that this limitation is due to the logic gate circuit topology, and not to an intrinsic device limitation. Moreover, in this measurement, the inverter characteristic does not reach 0 V. This is due to the *pull-up* transistor not switching OFF completely. Nonetheless, control and polarity gate input voltages both range from 0 V to $V_{\rm dd} = 1$ V, making this gate fully functional for implementing multilevel static logic. As described in [8], the degraded output characteristic of the measurement of Fig. 16 can simply be restored using pairs of transistors with opposite polarities, as shown in Fig. 13(d). As noted in Section II, this final XOR gate is not only built with four transistors instead of eight for the standard CMOS implementation, but no transistor series are present in the *pull-up* and *pull-down* networks, thus all transistors can be implemented with minimum sizing.

### *C. Circuit Performance Simulation*

Using the optimized device model described in Fig. 11, we produced a few more complex circuit simulations. In Fig. 17, the simulation of the same circuit shown in Fig. 16 was performed

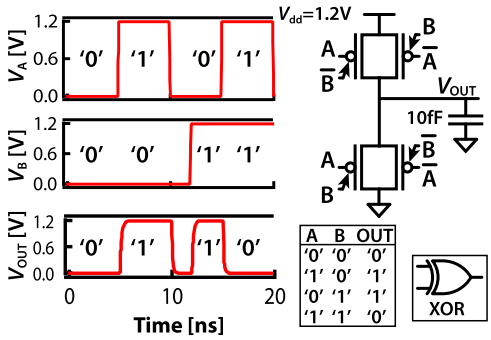


Fig. 18. Four-transistor XOR gate is built and simulated by using a table model for the optimized device based on the data extracted from TCAD simulations.

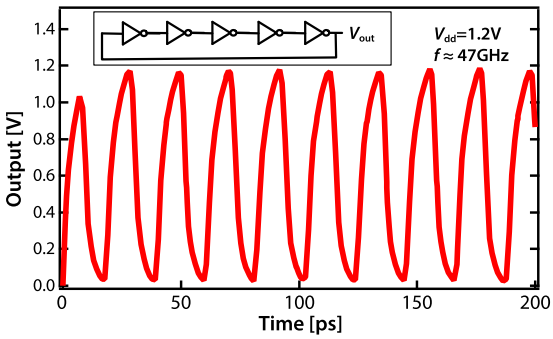


Fig. 19. Transient simulation of a five-stages ring oscillator. The number of vertically stacked nanowires is 6 per device. 0.3 fF load capacitance is included in each stage to explicitly account for parasitics. Frequency reaches 47 GHz.

using the optimized device model. This simulation shows no output degradation for the inverter configuration and demonstrates that the output signal degradation for the buffer configuration of the circuit is due to early switching OFF of the transistors in the *pull-up* and *pull-down* networks, as would be expected in an equivalent MOSFET circuit. As mentioned in Section V-B, full-swing XOR operation can be obtained by coupling transistors of opposite polarity in the XOR circuit. Simulation of the four-transistor schematic of Fig. 13(d) is shown in Fig. 18, showing full-swing output. Finally, in Fig. 19, we show a transient simulation of a five-stage ring oscillator, forecasting operating frequencies for this circuit reaching 47 GHz.

## VI. Opportunities and Discussion

In the recent years, transistor size reduction is facing serious physical challenges, demonstrated by scaling slow-down compared to the predictions of Moore's law. Most of the research trying to overcome these difficulties is focusing on novel device materials and geometries. In this study, we envision the development of a novel device structure together with a paradigm shift at circuit design level. In this framework, we lessen constraints at the physical level while adding the degree of freedom of in-field polarity control.

We consider this study as a proof of concept for the use of DG devices in future circuit design. However, numerous improvements could be implemented in order to improve the device characteristics and reduce dimensions. First, at the technology level, high-$\kappa$ gate dielectric materials and metal gates, together with channel strain techniques can be directly applied to the presented structure. As shown in the simulations of Section IV-C, these elements would provide further degrees of freedom to better tune device symmetry and control of polarization thresholds. Recent works have indeed utilized these technology enablers in similar DG-SiNWFET architectures to enhance the symmetry of n- and p-branches [27], to the advantage of more reliable and efficient logic circuits.

Moreover, the presented architecture is highly configurable, and transistors with three or more independent GAA regions can be fabricated. This can be done using the gate-to-gate self-alignment technique employed in this study, and different transistor types can be fabricated at the same time on a substrate. Specifically, in [33], an evaluation of the same transistor architecture exploiting the added configurability of three independent gates is presented.

More degrees of freedom at device level directly enable more compact and efficient logic gate designs with respect to standard CMOS technologies [6], [34], and finally, our top–down fabrication approach can implement CMOS-compatible, highly regular and dense arrays of nanowire stacks. Specifically, device regularity is an extremely important feature to reduce design constraints in current ULSI scaled devices, where double or triple-patterning techniques are employed to minimize device dimensions.

## VII. Conclusion

The ability of a single double-gate SiNW FET with in-field polarity control to implement the XOR function enables several applications and advantages in logic circuit design. At the same time, the top–down stacked SiNW fabrication with GAA electrodes presents an approach with great potential in terms of scalability, large-scale integration and compatibility with current CMOS fabrication processes. Moreover, the simplicity of the proposed fabrication process opens the possibility to a number of potential technological improvements, which can be implemented to further tune the symmetry and efficiency of the devices. The p- and n-branch threshold voltages can be adjusted by engineering of the gate material, of the S/D contact workfunction and doping of the device channel. Our fabricated devices are the first demonstrated so far to combine remarkable device characteristics with sufficient symmetry and compatible operating voltages to enable complementary multilevel logic synthesis and fully exploit the advantages of the efficient DG-SiNWFET XOR implementation.

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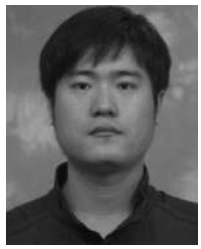

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