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Top-gated chemical vapor deposited MoS_2 field-effect transistors on Si_3N_4 substrates

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We report the electrical characteristics of chemical vapor deposited (CVD) monolayer molybdenum disulfide (MoS_2) top-gated field-effect transistors (FETs) on silicon nitride (Si_3N_4) substrates. We show that Si_3N_4 substrates offer comparable electrical performance to thermally grown SiO_2 substrates for MoS_2 FETs, offering an attractive passivating substrate for transition-metal dichalcogenides (TMD) with a smooth surface morphology. Single-crystal MoS_2 grains are grown via vapor transport process using solid precursors directly on low pressure CVD Si_3N_4, eliminating the need for transfer processes which degrade electrical performance. Monolayer top-gated MoS_2 FETs with Al_2O_3 gate dielectric on Si_3N_4 achieve a room temperature mobility of 24 cm^2/V s with I_{on}/I_{off} current ratios exceeding 10^7. Using HfO_2 as a gate dielectric, monolayer top-gated CVD MoS_2 FETs on Si_3N_4 achieve current densities of 55 $\mu A/\mu m$ and a transconductance of 6.12 $\mu S/\mu m$ at V_{tg} of -5 V and V_{ds} of 2 V. We observe an increase in mobility at lower temperatures, indicating phonon scattering may dominate over charged impurity scattering in our devices. Our results show that Si_3N_4 is an attractive alternative to thermally grown SiO_2 substrate for TMD FETs. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4907885]

Graphene as a two-dimensional material has been thoroughly studied for its remarkable electrical, mechanical, and optical properties. However, a large roadblock to potential graphene-based CMOS devices is the absence of a bandgap, due to graphene's Dirac cone band structure. As a result, other two-dimensional (2D) materials such as transition-metal dichalcogenides (TMDs) are being studied. Of the TMDs, molybdenum disulfide (MoS_2) has particularly attracted a lot of attention. MoS_2 is a 2D semiconductor with a bulk indirect bandgap of ~1.3 eV, and a direct bandgap of ~1.8 eV for single layers.[1–3] Its bandgap allows for high I_{on}/I_{off} metal-oxide semiconducting field-effect transistors (MOSFETs). In principle, the confinement of channel charge carriers to nearly atomic thicknesses (~0.65 nm) allows for improved gate control, leading to reduced short-channel effects. Top-gated FETs based on exfoliated monolayer MoS_2 flakes on SiO_2 have shown room temperature mobilities >80 cm^2/V s, with I_{on}/I_{off} ratios exceeding 10^8.[4] However, exfoliated MoS_2 flakes are typically small and cannot be easily scaled to large areas.

Recent studies have shown that the substrate can play a large role in the performance of MoS_2 FETs. Multi-layer MoS_2 back-gated FETs on 50 nm Al_2O_3 substrates have shown back-gated mobilities >100 cm^2/V s,[5] while multi-layer MoS_2 FETs on 50 nm thick spin-coated poly(methyl methacrylate) (PMMA) substrates have achieved back-gated mobilities >400 cm^2/V s.[6] Furthermore, the mobility can be engineered by applying an appropriate top gate dielectric, such as HfO_2, Al_2O_3, or polymer dielectrics.[7–9] Applying a high-*k* dielectric as either a substrate or superstrate increases the screening of charged impurities in the MoS_2 layer, which may enhance the mobility.[10] The substrate may affect FET performance by introducing long range or short range charge disorder. It has been shown that the MoS_2 follows the morphology of the substrate surface, whereby a rough surface may affect long range and short range scattering parameters.[6,11] Graphene was reported to have a smooth surface morphology when transferred on Si_3N_4 substrates.[12] As a result, graphene on Si_3N_4 showed comparable mobility to SiO_2 due to lower long and short range scattering parameters. Additionally, various substrates can cause carrier fluctuations due to extrinsic doping, which can be a contributing factor to the mobility.

We report on the fabrication and characterization of top-gated chemical vapor deposition (CVD)-grown MoS_2 FETs on Si_3N_4 insulating substrates. We see comparable electrical performance of MoS_2 FETs on these substrates as compared to conventional thermally grown SiO_2-Si substrates. Silicon nitride substrates offer superior passivating qualities over thermal oxide, such as better diffusion barriers against water molecules and ions, and a higher dielectric constant leading to increased electric field screening.[13] Additionally, Si_3N_4 can function better as an etch stop layer than SiO_2 while etching the gate dielectric from the source/drain and other regions. Silicon nitride substrates were grown by low pressure chemical vapor deposition (LPCVD) at 800 °C on highly doped silicon. In this study, the MoS_2 atomic films on Si_3N_4 (90 nm)/Si substrates were prepared by the sulfurization of MoO_3, a process similar to those described in Refs. 14–16. The starting materials were MoO_3 (15 mg) and sulfur (1 g) powder that were loaded in alumina crucibles and placed inside a quartz tube. The temperature of the furnace was raised to 850 °C with temperature of sulfur end of the furnace at roughly 350 °C. The growth continues for 5 min at 850 °C, after which the heater in the furnace was turned off and the N_2 flow rate was set to 200 sccm for cooling down. A combination of atomic force microscopy (AFM) (Figure 1(a)), Raman spectroscopy (Figure 1(b)), and photoluminescence spectroscopy (PL) (Figure 1(c)) was used to ascertain

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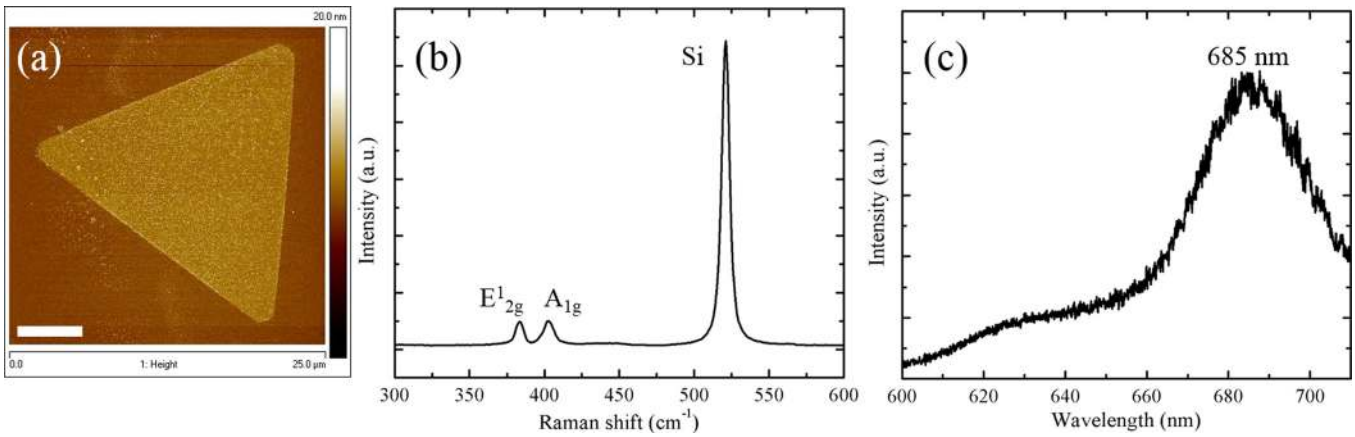

FIG. 1. (a) AFM image of an isolated triangular monolayer MoS_2 domain on Si_3N_4. The CVD MoS_2 domains were typically 0.8 nm in thickness and did not show surface contamination before any fabrication steps. (b) Raman map of the same isolated monolayer MoS_2 domain with the Raman and photoluminescence spectra shown below. The E_{2g1} peak is at 383.4 cm^{-1} with the A_{1g} at 402.9 cm^{-1}. This corresponds to a Δ of 19.5 cm^{-1}. (c)The photoluminescence spectrum of the CVD MoS_2 also shows a strong peak at around 685 nm (1.81 eV). The scale bar is 5 μm.

the single-layer thickness of the isolated as-grown CVD MoS_2 domains used for electrical characterization. As shown in Figure 1(a), the CVD MoS_2 domains were typically 0.8 nm in thickness and did not show surface contamination before any fabrication steps. The E^1_{2g} peak is at 383.4 cm^{-1} with the A_{1g} at 402.9 cm^{-1}. This corresponds to a peak separation delta (Δ) of 19.5 cm^{-1}, which is characteristic of single-layer MoS_2.[17,18] The full width at half maximum (FWHM) of the E^1_{2g} and A_{1g} peaks can indicate the quality of the film. The CVD MoS_2 grown on Si_3N_4 shows a FWHM of 6.69 cm^{-1} for the A_{1g} peak and 5.3 cm^{-1} for the E^1_{2g} peak, similar to reports of CVD MoS_2 on SiO_2 substrates.[14] The PL spectrum of the CVD MoS_2 also shows a strong peak at around 685 nm (1.81 eV) which is widely reported as the band gap of monolayer MoS_2.[14]

Top-gated MoS_2 FETs were fabricated as follows. Suitable CVD grown MoS_2 flakes were identified using a combination of optical contrast, Raman spectroscopy, and AFM images. Device active regions were defined using e-beam lithography. Excess MoS_2 was etched using Cl_2 plasma. Next, metal electrodes were defined with a second e-beam lithography step. A stack of Ag/Au (20 nm/30 nm) was deposited as a low-work function (4.26 eV) source/drain metal electrodes to enhance n-type conduction of the MoS_2 FET. Following a metal liftoff in acetone, atomic layer deposition (ALD) was used to deposit a 25 nm thick layer of Al_2O_3 or HfO_2 as a top gate dielectric. The top gate electrode was then defined using a final e-beam lithography step. The top gate metal was deposited as a 50 nm stack of Ni/Au. A final metal liftoff in acetone completed device fabrication. An optical image of the final device structure used for temperature dependence and mobility extraction is shown in the inset of Figure 2(b). Measurements presented in this paper were taken in vacuum ($\sim 10^{-6}$ Torr), and in the dark. The back-gate was grounded in all top-gated measurements.

Figure 2(a) is the I_{ds}-V_{gs} transfer characteristics of a MoS_2 transistor with a top gate dielectric of Al_2O_3. For all DC measurements, the device gate length (L_g) is 300 nm and the widths (W) vary from 10 μm to 25 μm, depending on the size of the CVD MoS_2 domain. The top gate voltage (V_{tg}) is swept from -7 V to 7 V with the drain voltage (V_d) varying from 0.1 V to 2.0 V. The device exhibits a threshold voltage (V_{th}) around -4.0 V, indicating unintentional n-type doping of the MoS_2 during the fabrication or growth. This is common for both CVD and exfoliated MoS_2 devices, intrinsically caused by sulfur vacancies in the MoS_2 and extrinsically by doping sources such as PMMA and acetone. With Al_2O_3 as the top gate dielectric, the I_{on}/I_{off} ratios exceed 10^7 at a V_{ds} of 2.0 V with off-state currents less than 10^{-7} μA/μm. Using the slope of the I_{ds}-V_{gs} curve in the linear region, the intrinsic field-effect mobility is calculated using $\mu_{fe} = [dI_{ds}/dV_{gs}][L/WC_{ox}V_{ds}]$. Operating at a low-field V_{ds} of 0.1 V, we extract a maximum mobility of 24 cm^2/V s. This mobility agrees with reported values for CVD MoS_2 FETs on thermally grown SiO_2.[19–21] Figure 2(b) shows the I_{ds}-V_{ds} output curves. Figure 2(c) is the I_{ds}-V_{gs} transfer characteristics and Figure 2(d) is the I_{ds}-V_{ds} output characteristics of a monolayer MoS_2 transistor with a top gate dielectric of HfO_2. The current densities for HfO_2 are much larger than that of Al_2O_3, exceeding 55 μA/μm at a V_{ds} of 2.0 V. As shown in the inset of Figure 2(c), the devices with HfO_2 gate dielectric on Si_3N_4 substrates achieve a maximum transconductance (g_m) of 6.17 μS/μm at a V_{ds} of 2.0 V. These figures exceed previous reports of current density and transconductance in top-gated CVD grown monolayer MoS_2 devices with equivalent gate lengths.[20,22] We can see the output curves tending more towards current saturation with HfO_2. Recent reports have shown that Si_3N_4 can be used to n-type dope TMDs.[23,24] Positive fixed charge centers within the nitride films can act as charge transfer doping centers, which forms a possible explanation for the large V_{th} shifts in our devices. Additionally, oxygen vacancies at the MoS_2 to gate dielectric interface can function as shallow charge traps, which would increase the I_{off}.[25] A possible source for these uncompensated atoms is improper surface temperature ramping before ALD growth. The substrate leakage for all Si_3N_4 substrate devices is low, averaging less than 0.25 fA/cm^2.

Figure 3 shows the four point conductance (G) at different temperature (T) values ranging from 300 K to 77 K. As shown in the inset of Figure 2(b), the device dimension used for this measurement was a L_g of 5 μm and a W of 10 μm. The MoS_2 FETs used for low-temperature measurements

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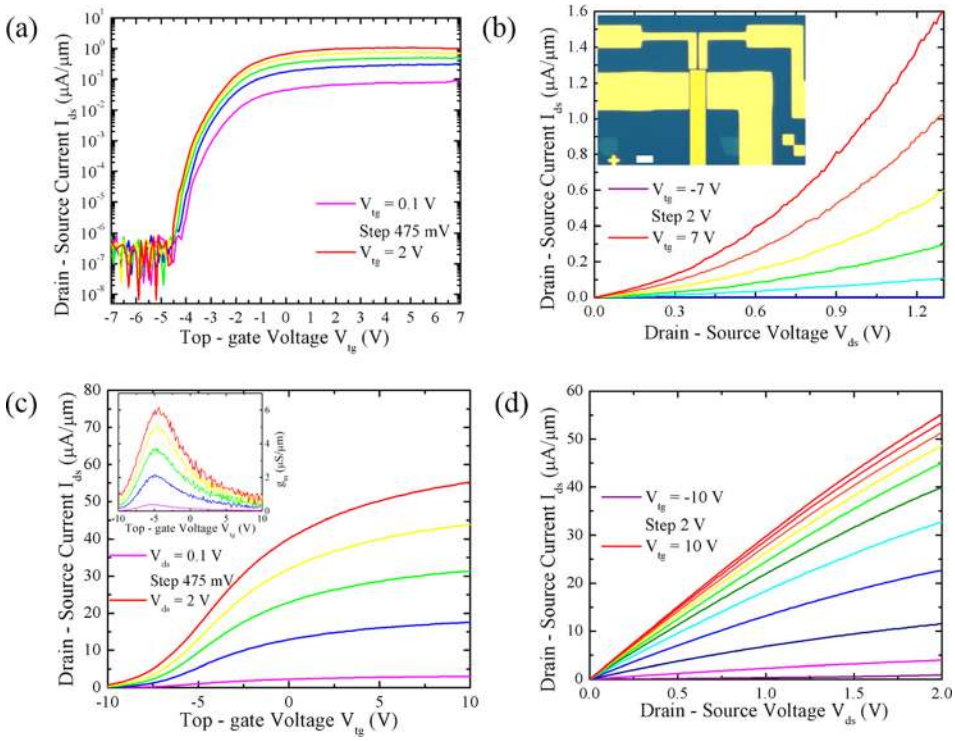

FIG. 2. (a) Drain-to-source current I_{ds} vs. top gate voltage V_{tg} for different drain voltages V_d on an Al_2O_3 top-gated device. The threshold voltage V_t is around -4.0 V indicating unintentional n-type doping of the MoS_2. The I_{on}/I_{off} ratio reaches 10^7 at $V_d = 2.0$ V. (b) Drain-to-source current I_{ds} vs. drain voltage V_d for different top gate voltages V_{tg}. Note the device shows negligible currents until a V_{tg} of -2 V. Inset: Optical image of a top-gated MoS_2 FET. (c) Drain-to-source current I_{ds} vs. top gate voltage V_{tg} for different drain voltages V_d on an HfO_2 top-gated device. With HfO_2 as a gate dielectric, current drives are much larger and saturation is observed. Inset: Transconductance g_m vs. top gate voltage V_{tg}. (d) Drain-to-source current I_{ds} vs. drain voltage V_d for an HfO_2 top-gated device. The scale bar is 5 μm.

were gated with Al_2O_3, as they possessed a higher fabrication yield over HfO_2 gated devices. As temperatures are reduced, the V_{th} shifts towards higher voltages. This is because a larger bias voltage is required to overcome the larger potential barrier that less energetic electrons face at lower temperatures. To offset the V_{th} shift, Figure 3 plots G vs. V_{tg}–V_{th} for different temperatures. The inset of Figure 3 shows the four point intrinsic mobility vs. temperature. The mobility increases with decreasing temperature to a value of 58 cm^2/V s at 77 K, suggesting a decrease in ionized impurity scattering in the top gate configuration. In the phonon-limited region of 100 K to 300 K, the mobility vs. temperature data can be fit to $\mu \sim T^{-\nu}$ to gain some insight into the scattering mechanisms of the device. A functional fit of the highest mobility device yields $\nu \approx 0.65$, which is significantly less than the predicted theoretical value ($\nu = 1.52$). This predicted theoretical value takes into account the quenching of the homopolar phonon modes of monolayer MoS_2, suggesting that other temperature-dependent scattering mechanisms are involved in our devices.[26] Previous reports of mobility dependence on temperature have extracted a coefficient as low as $\nu = 0.3$ for top-gated MoS_2 with HfO_2 ($k = 19$) as a gate dielectric.[27] Our devices for this measurement were gated with Al_2O_3 in a significantly lower-k top gate environment, suggesting the high-k Si_3N_4 substrate may also contribute to screening phonons. This is also supported by the fact that Si_3N_4 has a higher surface polar optical phonon energy than SiO_2, which leads to less remote phonon scattering in the MoS_2 channel.[28]

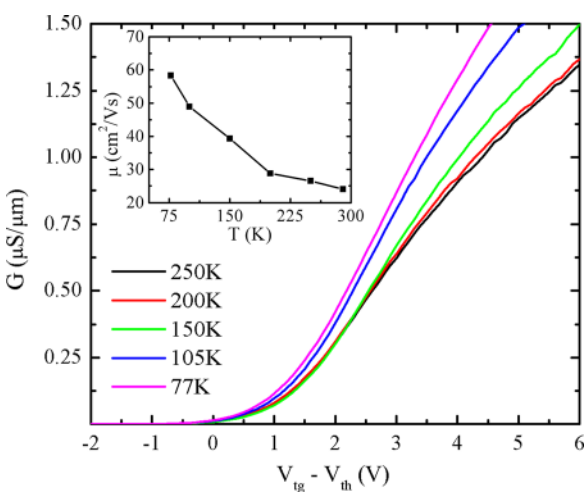

FIG. 3. Channel conductance (G) vs. (V_{tg}-V_{th}) for temperatures ranging from 250 K to 77 K. The threshold voltage (V_t) shifts to higher voltages at lower temperatures due to the temperature dependence of the surface potential. A clear increase in the slope of the conductance curve can be seen with a decrease in temperature. Inset: μ vs. T for a top-gated MoS_2 device.

In summary, we demonstrate top-gated CVD MoS_2 FETs on Si_3N_4 with comparable electrical performance to SiO_2 substrates. We achieve a mobility of 24 cm^2/V s with I_{on}/I_{off} ratios exceeding 10^7. Using HfO_2 as a top gate dielectric, devices achieve current densities of 55 μA/μm and a max transconductance of 6.12 μS/μm. Temperature dependence of mobility in MoS_2 on Si_3N_4 shows a strong suppression of charged impurity scattering and a weaker than expected dependence on phonon scattering, suggesting the Si_3N_4 may play a role in screening remote phonons. We show that Si_3N_4 substrates are viable for TMD-based logic devices and potential radio frequency applications.

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