



Topological Insulator Bi_2Se_3 Nanowire High Performance Field-Effect Transistors

SUBJECT AREAS:

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NANOWIRES

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Topological insulators are unique electronic materials with insulating interiors and robust metallic surfaces. Device applications exploiting their remarkable properties have so far been hampered by the difficulty to electrically tune the Fermi levels of both bulk and thin film samples. Here we show experimentally that single-crystal nanowires of the topological insulator Bi_2Se_3 can be used as the conduction channel in high-performance field effect transistor (FET), a basic circuit building block. Its current-voltage characteristics are superior to many of those reported for semiconductor nanowire transistors, including sharp turn-on, nearly zero cutoff current, very large On/Off current ratio, and well-saturated output current. The metallic electron transport at the surface with good FET effective mobility can be effectively separated from the conduction of bulk Bi_2Se_3 and adjusted by field effect at a small gate voltage. This opens up a suite of potential applications in nanoelectronics and spintronics.

Topological insulators (TI) are characterized as a new class of materials which have insulating band gaps in the bulk but gapless surface states topologically protected by time-reversal symmetry^{1,2}. Recently discovered three-dimensional (3D) TI materials, such as Bi_2Se_3 , Bi_2Te_3 and Sb_2Te_3 , have been intensively investigated both theoretically and experimentally^{3,4}. The gapless surface states featuring helical Dirac electrons have been observed by angle-resolved photoemission spectroscopy^{5–7} and scanning tunneling microscopic techniques^{8–10}. Thin films and nanoribbons of TI show anomalous high-field magnetoresistance^{11–13}, coherent surface transport induced by Aharonov-Bohm interference¹⁴, and optoelectronic properties due to the spin-polarized surface states¹⁵.

Bi_2Se_3 , a well-known thermoelectric material, is a 3D TI with a bulk band gap of 0.35 eV and a single Dirac cone on the surface^{2,3}. Most current experimental research focusses on the surface states of thin TI samples exfoliated from bulk material^{6,16}. A few groups have reported modification of the surface conduction of such exfoliated TI samples by doping, applying a vertical electric field or polarized light^{15,17–19}. Yet, up to now, no high-performance microelectric devices based on topological insulators such as the analog of metal oxide semiconductor field effect transistors (MOSFETs) have been reported. The MOSFET is the basic building block in complementary metal oxide semiconductor (CMOS) technology, the fundamental basis for digital and analog circuits. For conventional CMOS devices, the surface conduction of Si is protected by thermal SiO_2 to optimize its inversion properties for good transistor performance. This is one of the primary reasons why Si is preferred over other semiconductor materials for CMOS technology. For a topological insulator material, the gapless surface state is derived from its inherent material properties, and maintains a robust surface conduction. Therefore the integration of TI as the active conduction channel in MOSFETs is very attractive because it will leverage the advantages afforded by the novel TI materials with the vast infrastructure of current semiconductor technology.

In this work, we fabricated and measured surrounding-gate Bi_2Se_3 nanowire field-effect transistors. The nanowires were grown from Au catalyst and integrated by using a self-alignment technique. The FET current-voltage (I–V) characteristics were measured at different temperatures, exhibiting excellent performance. We have studied the separation of surface metallic conduction from bulk semiconductor conduction with gate electric field at different temperatures. The activation energy of bulk conduction was found to be very close to the band gap of bulk Bi_2Se_3 . We have also studied the effective electron mobility and scattering mechanism in the devices.

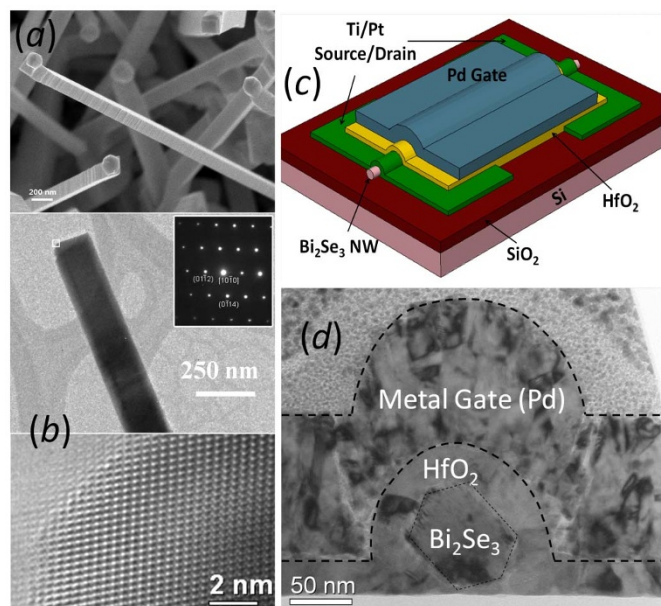


Figure 1 | (a) SEM image of Bi_2Se_3 nanowires; (b) HRTEM image of Bi_2Se_3 nanowires showing that the nanowire growth direction is close to $[11\bar{2}0]$, the inset above shows a magnified region of the nanowire; (c) Schematic of a Bi_2Se_3 nanowire FET and (d) TEM image of the cross-section of a Bi_2Se_3 nanowire FET.

Results

Figure 1 (a) shows a scanning electron microscopy (SEM) image of the as-synthesized Bi_2Se_3 nanowires which are about 50 nm to 150 nm wide and 10 μm long. Au nanoparticles (NPs) were found at the top-end of each nanowire. This indicated that Bi_2Se_3 vapor was first absorbed by Au catalyst to form a Bi_2Se_3 and Au eutectic; then Bi_2Se_3 diffused through Au to form the single-crystal nanowires. This

process is similar to the growth of Si nanowires governed by vapor-liquid-solid (VLS) mechanism. Bi_2Se_3 has a layered rhombohedral crystal structure with five covalently bonded atoms in one unit cell. These quintuple layers are linked by van der Waals interactions²⁰. The high-resolution transmission electron microscopy (HRTEM) image shown in Figure 1 (b) demonstrates that the Bi_2Se_3 nanowires are in a well-defined single-crystal rhombohedral phase and the growth direction is close to $[11\bar{2}0]$. A schematic of the Bi_2Se_3 nanowire FET is shown in Figure 1(c) and a TEM image of the cross-section in Figure 1 (d). The hexagonal nanowire core is surrounded first by the insulating HfO_2 layer and then by the Omega-shaped top gate.

The electrical characterization was carried out on a probe station inside a vacuum chamber. As shown in Figure 2 (a), the transistor has excellent drain current (I_{DS}) vs. top gate voltage (V_{GS}) transfer characteristics: cutoff current close to zero, strong-inversion-like on-state current and current on/off ratio larger than 10^8 at a V_{GS} swing of 1.0 V. The backside Si was grounded during all the measurements. The transistor has unipolar current dominated by electron conduction. This is similar to a conventional long-channel Schottky-barrier MOSFET with either electron or hole conduction determined by the unipolar Schottky junctions at the source and drain. No hysteresis was observed in the $I_{\text{DS}}-V_{\text{GS}}$ curves at 77 K. A hysteresis shift was observed at higher temperatures ($T > 240$ K), most likely due to the activation of traps in the HfO_2 . Very similar device characteristics were observed for the drain voltage (V_{DS}) in the range 0.05 V to 4.0 V used in the study.

As shown in Figure 2 (b) and (c), the Bi_2Se_3 nanowire FET exhibits well-saturated, smooth I_{DS} vs. V_{DS} curves with negligible contact resistance. The transistor output characteristics clearly demonstrate cutoff, weak, moderate and highly conductive regions at different V_{GS} , similar to the cutoff (leakage), weak, moderate and strong inversion regions of conventional MOSFETs. I_{DS} saturates roughly at $V_{\text{DS}} = V_{\text{GS}} - V_{\text{th}}$ in the highly conductive region but does not saturate at $V_{\text{DS}} \approx 3\phi_t$ in the weak/moderate conductive regions ($\phi_t = kT/q$). I_{DS} keeps increasing significantly after $3\phi_t$. This means that the Bi_2Se_3

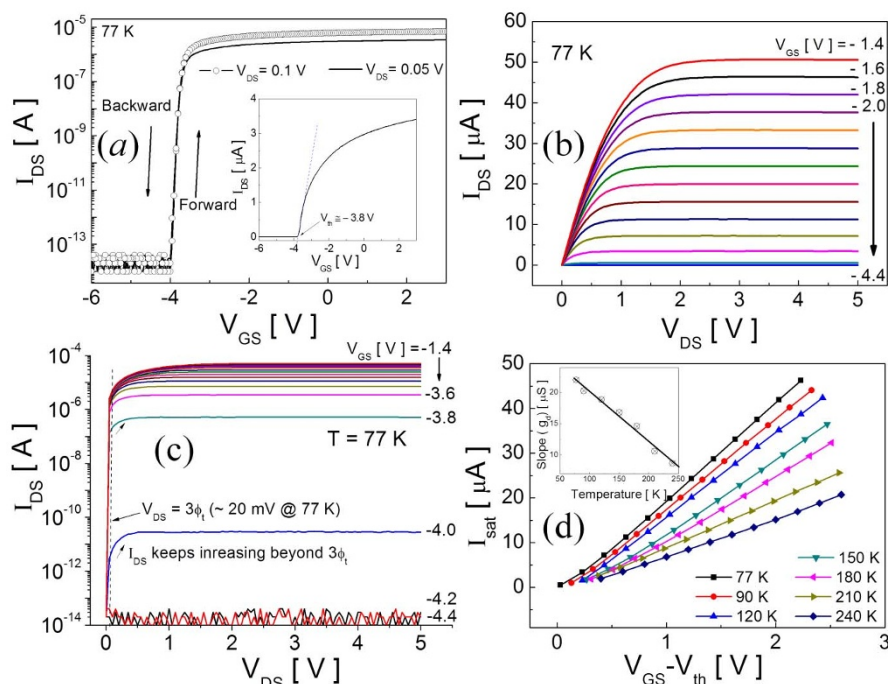


Figure 2 | (a) Transfer characteristics ($I_{\text{DS}}-V_{\text{GS}}$) of Bi_2Se_3 nanowire FET at 77K; inset is the linear-scale plot showing $V_{\text{th}} = -3.8$ V. (b) and (c) are linear-scale and log-scale $I_{\text{DS}}-V_{\text{DS}}$ for V_{GS} from -4.4 V to -1.4 V at 77 K. (d) I_{DS} as a function of over-threshold voltage ($V_{\text{GS}}-V_{\text{th}}$) and inset: its linear fit slope vs. temperature.



nanowire FET does not follow the diffusion current model as described for conventional MOSFETs. We believe I_{DS} in the weak/moderate conductive regions is also dominated by drift current.

Similar I_{DS} - V_{DS} characteristics have been obtained at different temperatures. We observed that the saturation current I_{DSat} at various V_{GS} does not follow the quadratic law which predicts that I_{DSat} varies linearly with $(V_{GS}-V_{th})^2$ as it does in conventional long-channel MOSFETs. Rather, as shown in Figure 2(d), I_{DSat} varies linearly with the over-threshold voltage $(V_{GS}-V_{th})$ at different temperatures for V_{GS} in the range -3.8 V to -1.4 V. The saturation current can be expressed by the drift current model as a product of the number of electrons and their velocity at the source end of the nanowire:

$$I_{DSat} = Aqn_s v_s = \frac{Cox}{L} (V_{GS} - V_{th}) v_s$$

where A , n_s , C_{ox} , L and v_s are nanowire cross-section area, electron concentration at source end, gate capacitance, channel length and electron velocity at the source end of Bi_2Se_3 -nanowire, respectively. Therefore this linear relationship suggests that the saturation of I_{DS} is due to electron velocity saturation at the source end of the channel instead of pinch-off at the drain end of the nanowire channel²¹. The slope of each I_{DSat} vs. $(V_{GS}-V_{th})$ curve is saturation channel conductance (g_{dsat}); its value at different temperatures is extracted from Fig. 2 (d) and plotted in the inset, showing that the electron velocity at the source end increases linearly with decreasing temperature. The capacitance per unit length $C_{ox}/L = 1.3 \times 10^{-9}$ F/m was given by numerical calculation using a Synopsis TCAD program based on the cross-section size of the TEM image in Figure 1 (d). The calculated value of v_s is from 1×10^6 cm/s to 2×10^6 cm/s for temperatures from 240 K to 77 K, which is of the same order of magnitude as the Fermi velocity of Ti^{22} in the source and drain contacts.

Figure 3 (a) shows the electron effective mobility (μ_{eff}) of Bi_2Se_3 nanowire FET as a function of applied gate voltage at different temperatures. The field effect mobility extracted from the I_{DS} - V_{GS} curves shows a similar result. The effective mobility values were extracted from the linear region of I_{DS} - V_{DS} curves by using the following equation:

$$\frac{\partial I_{DS}}{\partial V_{DS}} = \mu_{eff} \frac{Cox}{L^2} (V_{GS} - V_{th})$$

The electron effective mobility decreases with increasing gate voltage in the range $200 \text{ cm}^2/\text{Vs}$ to $1300 \text{ cm}^2/\text{Vs}$ at 77 K. It should be noted that the precision of effective mobility estimation can be affected by the numerically calculated gate capacitance due to the top and bottom gate coupling. In Figure 3 (b), electron effective mobility as a function of temperature at different gate voltages is plotted and fitted using $\mu_{eff} \sim T^\alpha$. The value of α is about -1.85 at small over-threshold voltage and increases to -1.0 at large over-threshold voltage. Larger

over-threshold voltage will induce higher vertical electric fields. These mobility-temperature relationships suggest that electron-phonon scattering is a dominating factor in low-field conduction (optical phonon scattering for $-2.0 > \alpha > -1.5$, acoustic phonon scattering for $\alpha \approx -1.5$), and as the gate electric field increases, interface charge Coulomb scattering limits electron mobility in the Bi_2Se_3 nanowire FETs with $\alpha = -1^{23}$.

Figure 4 (a) compares the transfer characteristics (I_{DS} - V_{GS}) of a Bi_2Se_3 nanowire FET at different temperatures, all of which show unipolar, n-type, field effect behaviors. The I_{DS} - V_{GS} curves obtained at temperatures lower than 240 K show a clear cutoff region ($I_{DS} \approx 0$) in the subthreshold region ($V_{GS} < V_{th}$) and a large On/Off current ratio reaching 10^8 . The Off-state current for temperatures > 240 K flattens and saturates at negative voltages much below V_{th} . The temperature dependence of currents in the On and Off states are summarized in Figure 4(b). The Off-state current for temperatures above 240 K was taken from the flat region while the On-state current was taken at $V_{GS} = 2.0$ V. The Off state current starts increasing rapidly as the temperature increases above 240 K, while the On-state current keeps decreasing as the temperature increases. Such temperature dependence indicates metallic conduction in the On state and insulating behavior in the Off state. Figure 4(c) shows a fitting of the strongly activated temperature-dependent current to $I_{DS,Off} = I_0 e^{-E_a/kT}$ where E_a is the activation energy, k is Boltzmann's constant, and I_0 is a constant prefactor. The fit shows that E_a is about 0.33 eV with uncertainty = 0.01 eV which is very close to reported bandgap value of bulk $\text{Bi}_2\text{Se}_3^{2,3}$.

Discussion

These results can be interpreted phenomenologically as follows. In the Off state, the gate voltage is large enough to deplete the electrons from the nanowire. The small, temperature dependent Off-state current is due to thermal excitations across the energy band gap of the bulk of Bi_2Se_3 . It also indicates that the electric field generated by the gate voltage below the threshold is likely to be strong enough to modify the spectrum of the nanowire and destroy the surface conduction channels. Numerical simulation²⁴ has demonstrated that electric field could drive a topological insulator across a quantum phase transition to become a trivial band insulator. In contrast to conventional semiconductor nanowires, the saturated current in the On-state is linear in gate voltage, indicating metallic conduction, and is most likely flowing at the surface of the nanowire. This interpretation is also consistent with the temperature dependence of the saturated conductance. These two regimes, the surface metallic conduction and the insulating switch-off, can be controlled by a surprisingly small gate voltage (a few Volts). Our data cannot unambiguously confirm or rule out the presence of Helical Dirac fermions.

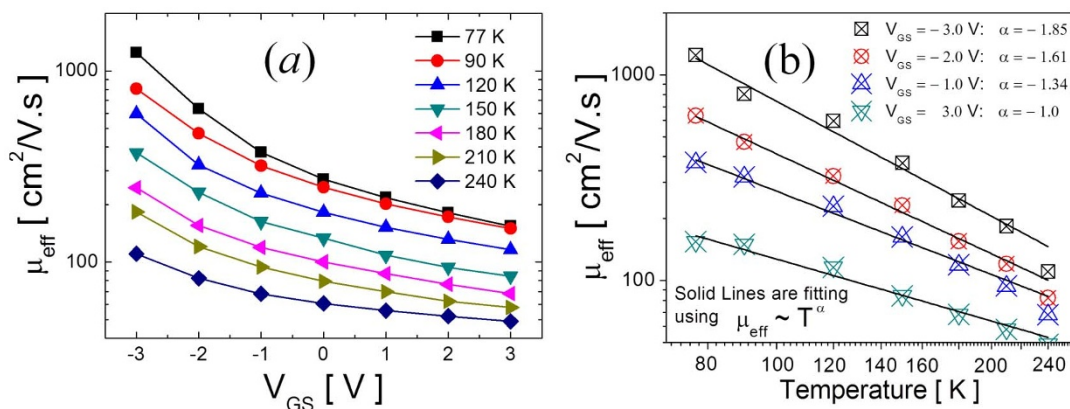


Figure 3 | (a) Electron effective mobility vs. gate voltage at different temperatures in a range 77 K to 240 K. (b) Electron effective mobility as a function of temperature in different device operation regions and the fits to $\mu_{eff} \sim T^\alpha$.

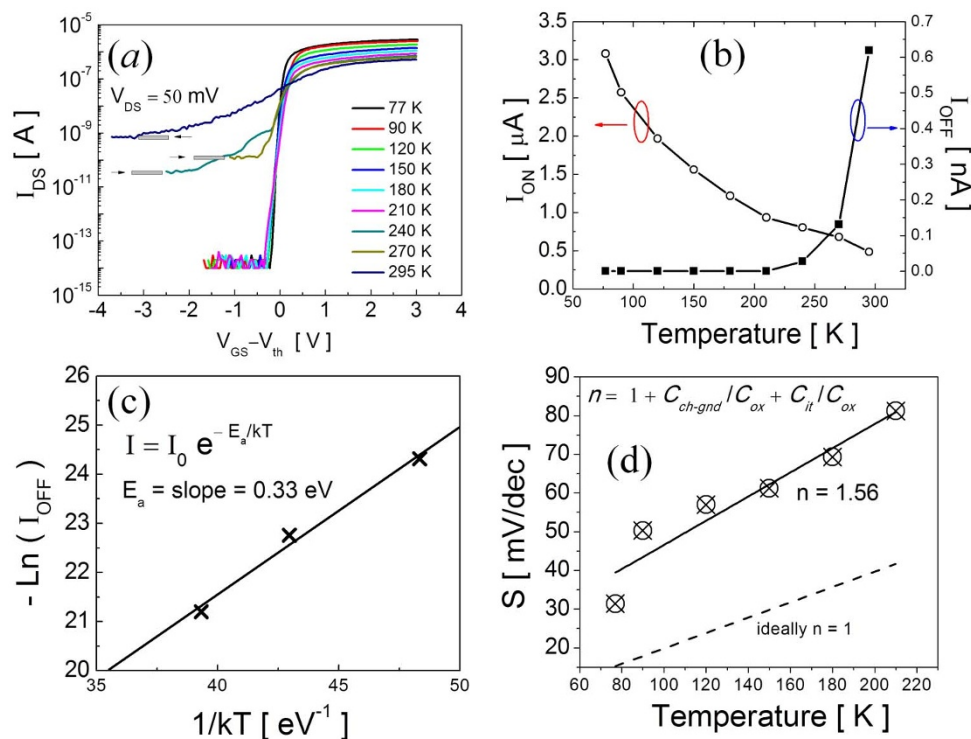


Figure 4 | (a) I_{DS} - V_{GS} at different temperature from 77 K to 295 K with $V_{DS} = 50$ mV. (b) Data extracted from (a): On-state and Off-state current as a function of temperature. (c) $\ln(I_{OFF})$ at Off state vs. $1/kT$ above 240 K and its fit to $I_{DS,Off} = I_0 e^{-E_a/kT}$. (d) Subthreshold slope as a function of temperature, its fit to $S = \ln 10 \frac{kT}{q} \left(1 + \frac{C_{ch-gnd}}{C_{ox}} + \frac{C_{it}}{C_{ox}} \right)$ and ideal subthreshold slope $S = \ln 10 \frac{kT}{q}$ which is defined by thermal emission.

Future spectroscopic experiments and theoretical simulations on the spectrum and transport properties of Bi_2Se_3 nanowire FETs will shed more light on the phenomena reported here.

The switching performance of a FET is characterized by its subthreshold swing (S) which is defined as the V_{GS} swing to achieve 10 time increase of I_{DS} in the subthreshold region. While these Bi_2Se_3 nanowire FETs have a larger S value than the ideal thermodynamic limit, it is still much smaller than those often reported for nanowire-FETs based on conventional semiconductors. Figure 4 (d) shows the subthreshold swing of the Bi_2Se_3 nanowire FET at different temperatures and its fit to:

$$S = \ln 10 \frac{kT}{q} n = \ln 10 \frac{kT}{q} \left(1 + \frac{C_{ch-gnd}}{C_{ox}} + \frac{C_{it}}{C_{ox}} \right)$$

where C_{ch-gnd} is the capacitance between the nanowire surface and ground, and C_{it} is interface state capacitance^{21,25}. It should be noted that the effect of dielectric interface states is negligible at low temperature because I_{DS} - V_{GS} has almost zero hysteresis (see Fig. 2a). From the fitting which assumes C_{ch-gnd}/C_{ox} has no temperature dependence, C_{ch-gnd} is about $0.56C_{ox}$ or 7.3×10^{-10} F/m for the Bi_2Se_3 nanowire.

In summary, we have fabricated Bi_2Se_3 nanowire field-effect transistors by using a self-alignment technique and observed excellent device characteristics. The FETs show unipolar, n-type behavior with a clear cutoff in the Off state with only thermally activated conduction at relatively high temperatures, and a well-saturated output current indicating surface metallic conduction. The effective mobility extracted for different gate voltages and temperatures indicates phonon scattering at low electric fields and surface Columbic scattering at larger electric fields. The achievement of sharp switching from Cutoff to surface conduction and saturation current by a gate voltage of a few volts is neither expected nor has been previously reported. The different scaling behavior of the saturation current versus gate voltage in these devices relative to most conventional semiconductor

nanowire FETs may lead to novel circuit applications. Finally, since the spin and momentum are locked in the surface states of topological insulators³, our results open up the possibility of electric manipulation of spin current using gate voltage.

Methods

Bi_2Se_3 nanowire FETs were fabricated by using a self-alignment process, similar to the one used in our previous research on Si nanowire FETs^{26,27}. The essential steps are as follows: first, a layer of thermal SiO_2 (300 nm) was grown by dry oxidation on a Si wafer. On the top of the wafer, the Bi_2Se_3 nanowires were grown from Au catalyst deposited by sputtering in pre-defined locations. The nanowire growth followed a solid-vapor-solid route. The wafers (with Au) were loaded at the downstream end in a horizontal tube furnace while Bi_2Se_3 source powder was located at the heat center of the furnace. Then the furnace is heated to a temperature in a range of 500°C to 550°C and kept in that temperature for 2 h under a flow of 50 standard cubic centimeters (sccm) Ar as carrier gas. The as-grown Bi_2Se_3 nanowires were about 20 μm in length and 150 nm in diameter. Then Ti(3 nm)/Pt(100 nm) source/drain (S/D) electrodes were patterned on the nanowires at the growth location by photolithography, forming Pt/ Bi_2Se_3 Schottky junctions at both source and drain. The channel length was defined to be 2 μm . A layer of 30-nm HfO_2 was then deposited at 250°C by atomic layer deposition (ALD) with precursors of Tetrakis(ethylmethylamino)hafnium and water covering the nanowire channel and also part of S/D electrodes. The last step was the formation of a 100 nm Pd top gate by a lift-off process. Unlike the traditional nanowire harvesting and alignment methods, our self-alignment approach not only enables simultaneous batch fabrication of reproducible and homogeneous nanowire devices of high quality, but also limits the contamination of the nanowire during the fabrication process.

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Author contributions

H.Z. fabricated and measured the devices. H.Z. and Q.L. wrote the paper. H.Z., E.Z., H.-J.J., H.Y., H.L., O.K., C.A.R., D.E.I. and Q.L. contributed to the data analysis. J.E.B. carried out the TEM measurement. W.A.K. and J.E.M. contributed to the gate dielectric preparation. A.A. did the device simulation. C.A.R., E.Z., D.E.I. and Q.L. revised the manuscript. The project was designed by Q.L.

Additional information

Competing financial interests: The authors declare no competing financial interests.

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