Total Dose and Bias Temperature Stress Effects for HfSiON on Si MOS Capacitors

D. K. Chen, F. E. Mamouni, X. J. Zhou, R. D. Schrimpf, D. M. Fleetwood, K. F. Galloway, S. Lee, H. Seo, G. Lucovsky, B. Jun, and J. D. Cressler

***Abstract*—We have performed an experimental study of the effects of ionizing radiation and bias-temperature stress on Si MOS devices with HfSiON gate dielectrics. We compare the responses of homogeneous high-Si_3N_4 films and low-Si_3N_4 films that contain crystalline HfO_2. We observe that the low-Si_3N_4 films are more sensitive to ionizing radiation than the high-Si_3N_4 films. In particular, the low-Si_3N_4 film that includes crystalline HfO_2 is especially vulnerable to electron trapping due to substrate injection under positive irradiation bias. Both film types exhibit reduced radiation-induced charge trapping relative to previous Hf silicates. The high-Si_3N_4 film exhibits$\sim 16\times$ less radiation-induced net oxide-trap charge density than earlier Hf silicate films processed without nitride. We also find that these devices are relatively robust against bias-temperature stress instabilities. Consistent with the radiation response, the low-Si_3N_4 devices also display elevated levels of charge trapping relative to the high-Si_3N_4 devices during bias-temperature stress.**

***Index Terms*—Alternative dielectrics, bias-temperature instability, HfSiON, nitridation, total-dose irradiation.**

I. Introduction

ALTERNATIVE gate dielectrics are rapidly becoming necessary to the future of advanced semiconductor technology as the SiO_2 MOSFET reaches scaling limits. Gate leakage current becomes unmanageable as the gate oxide shrinks to the 10-Å regime. High-k dielectrics permit a physically thicker gate insulator, thereby reducing the gate leakage [1]. Hafnium oxide has emerged as a strong candidate due to its thermal stability and higher dielectric constant relative to other high-k transition metal atom dielectrics. On the other hand, other Hf alloys with lower dielectric constants, e.g., Hf silicates and Hf Si oxynitrides, offer improved interface qualities, but in the case of the silicates display a chemical phase separation that limits processing temperatures. The incorporation of nitrogen in Hf silicate films improves thermal stability and blocks dopant diffusion [2], [3]. However, metallic Hf-N bonding can decrease the band gap and reduce band offsets, thereby increasing gate leakage current [3], [4]. Various studies on HfSiON films conclude that these devices are suitable for low power applications [5]–[7].

Total-dose irradiation data on HfSiON films are at present very limited. For example, previous work by Felix *et al.*. [6], [8] focused on Hf silicates with no nitride processing, and Felix *et al.*. [9] and Zhou *et al.*. [10]–[12] reported on HfO_2 based devices where nitride processing was confined to a thin silicon oxynitride surface layer. Here we present results for HfSiON films that exhibit different trapping characteristics when exposed to ionizing radiation than either of these two previous types of dielectrics. Films with a high concentration of Si_3N_4 exhibit significantly less radiation-induced charge trapping than the films discussed in the previous work.

Bias-temperature instability also is an important reliability concern for MOS devices. The applied bias at elevated temperatures induces interface traps and oxide trapped charges that affect the device threshold voltage and long term reliability [13]. Negative bias temperature instability (NBTI) is especially a concern for pMOS devices [14]. Previous experiments on SiO_2 and HfO_2 on Si MOS devices show positive interfacial and oxide charge generation [10], [11]. The mechanism for NBTI is still under debate [15]. However, a widely accepted model that is especially relevant for relatively low fields and thin oxides [13], [16] involves the release and movement of hydrogen species to the interface. The negative bias pulls H^+ into the bulk oxide, resulting in net positive charge in the oxide. Here we evaluate the differences in charge trapping of devices with homogeneous HfSiON films and ones that contain crystalline HfO_2.

II. Device Details

The devices considered in this study are MOS capacitors with aluminum front and back contacts, Hf Si oxynitride dielectrics, and p-type silicon substrates. The device cross section is shown schematically in Fig. 1. The devices were fabricated at North Carolina State University. The Hf/Ti source gases, 2% SiH_4 in He, and Hf(IV)/Ti(IV) t-butoxide were deposited using remote plasma enhanced chemical vapor deposition (RPECVD). Two different Hf Si oxynitride pseudoternary alloys were integrated into these devices on nitrided, plasma-oxidized interfaces (e.g., SiON). These SiON interfacial layers are $\sim$0.6 nm. After deposition, rapid thermal annealing (RTA) for $\sim$1 minute in Ar was performed at 900°C. The samples were packaged in 28-pin dual inline packages at Georgia Tech. The dielectric constant (k) for the low-Si_3N_4 ($Hf_{0.6}SiO_{0.2}N_{0.2}$) and high-Si_3N_4 ($Hf_{0.3}SiO_{0.4}N_{0.4}$) content alloy films are $k = 14.6$ and $k = 12.7$, respectively [17]. The low-Si_3N_4 content film contains

Manuscript received July 20, 2007; revised September 19, 2007. This work was supported in part by the Air Force Office of Scientific Research through the AFOSR MURI program.

D. K. Chen, F. E. Mamouni, X. J. Zhou, R. D. Schrimpf, D. M. Fleetwood, and K. F. Galloway are with the Department of Electrical Engineering and Computer Science, Vanderbilt University, Nashville, TN 37235 USA (e-mail: dakai.chen@vanderbilt.edu).

S. Lee, H. Seo, and G. Lucovsky are with the Department of Physics, North Carolina State University, Raleigh, NC 27695 USA.

B. Jun and J. D. Cressler are with the Department of Electrical Engineering and Computer Science, Georgia Institute of Technology, Atlanta, GA 30332 USA.

Digital Object Identifier 10.1109/TNS.2007.910862

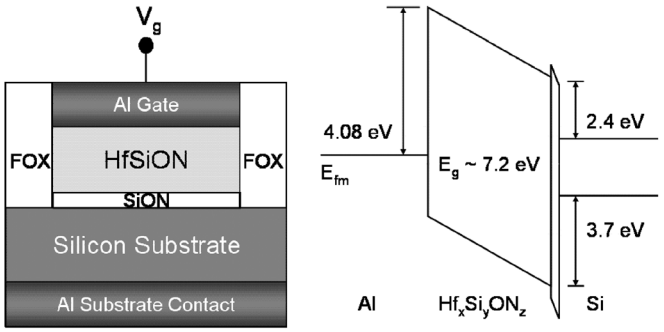

Fig. 1. Device structure and energy band schematic diagrams for Al/HfSiON/Si MOS capacitors.

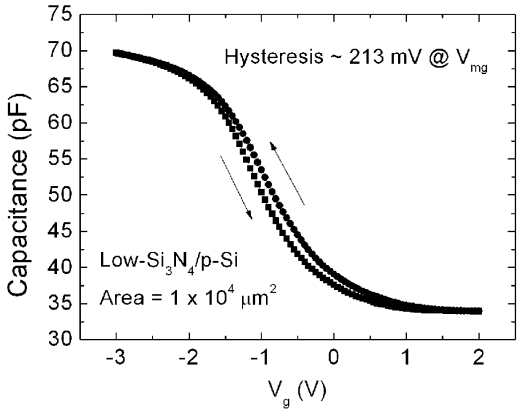

Fig. 2. 1-MHz capacitance-voltage characteristics for a 15-nm low-Si_3N_3 ($Hf_{0.6}Si_{0.2}ON_{0.2}$) film p-substrate MOS capacitor swept from accumulation to inversion and inversion to accumulation. The hysteresis is$\sim$213 mV at midgap.

crystalline HfO_2, while the high-Si_3N_4 content film is homogeneous [17]. The devices in this study have physical oxide film thicknesses of $\sim$15 nm (EOT$\sim$4 nm) and 2 nm (EOT $\sim$0.5 nm).

III. Experimental Details

Irradiation experiments were performed with an ARACOR 10-keV X-ray source at a dose rate of 31.5 krad(SiO_2)/min. The devices were irradiated incrementally to 5 Mrad(SiO_2). For comparison of responses, nominally identical devices were electrically stressed for the same times required to reach each total dose increment. Bias temperature stress (BTS) experiments were done on the packaged samples in a Delta Design 9039 oven. An Agilent 4156 B Semiconductor Parameter Analyzer was used to apply biases and to monitor the currents during the experiments.

Devices were characterized via 1 MHz capacitance-voltage (CV) measurements at sweep rates from 0.02 to 0.05 V/s using the midgap method of Winokur *et al.* [18]. CV measurements were swept from accumulation to inversion after each stress interval or total dose. We note that there is a transitional period between the stress/radiation and measurement, during which no bias is applied. A fraction of the trapped charges may recombine and/or detrap during this time. High-k dielectrics are especially susceptible to electron trapping/detrapping [19]. Conventional DC measurement techniques may not account for the trapped electrons that are quickly discharged after the stress is released. A detailed study of the stress-induced threshold voltage instabilities in high-k dielectrics requires transient measurement techniques such as the pulse current-voltage $I-V$ characterization [20]. Nevertheless conventional CV and $I-V$ characterization methods are adequate for the total dose irradiation analysis of high-k devices. A large number of devices were used for the irradiation and stress experiments. Each data set represents results from at least 5 devices that showed similar responses.

IV. Results and Discussion

A. Pre-Irradiation Characterization

The pre-irradiation CV characteristics showed considerable hysteresis in the thicker devices ($\Delta V_{\rm mg} \sim 200$ mV and 150 mV for the low- and high-Si_3N_4 films, respectively). The hysteresis for a 15 nm low-Si_3N_4 content device is shown in Fig. 2. The hysteresis indicates a relatively high density of process-induced border traps [21]. The effective border trap density, $\Delta N_{\rm bt}$, can be calculated by integrating the difference in forward and reverse C–V curves [22]

$$\Delta N_{\rm bt} \sim (1/{\rm qA}) \int |{\rm C}_r - {\rm C}_f| {\rm dV} \tag{1}$$

Here-q is the electron charge, A is the capacitor area, and C_r and C_f are the reverse and forward capacitance values. The estimated $\Delta N_{\rm bt}$ values are $\sim 2.7\times10^{11}$ cm^{-2} and 3.3×10^{11} cm^{-2} for the high- and low-Si_3N_4 devices respectively. There is no measurable hysteresis in the 2 nm devices.

There is also significant pre-irradiation interface trap charge density ($N_{\rm it} \sim 4\times10^{12}$ cm^{-2}) in the 15 and 13 nm gate oxide devices. The pre-irradiation $N_{\rm it}$ is much smaller ($N_{\rm it} \sim 5\times10^{11}$ cm^{-2}) in the 2 nm devices.

Fig. 3 illustrates the gate leakage current densities at $V_{\rm fb}+1$ V for the low- and high-Si_3N_4 devices of various film thicknesses. The gate leakage for films of EOT $=$ 2 nm is approximately 5 orders of magnitude less than in SiO_2 devices of equivalent electrical thickness. This demonstrates the main advantage of these devices relative to SiO_2 devices. Also, the low- and high-Si_3N_4 films exhibit similar levels of gate leakage current for the thicker oxide devices. However, the low-Si_3N_4 film shows slightly higher leakage for thinner films. The higher density of defect states in the low-Si_3N_4 devices produces higher trap-assisted tunneling current [23], which is more significant in the thinner oxide devices.

B. X-ray Irradiation

Neither the hysteresis nor the gate leakage current changes significantly with irradiation. Fig. 4 shows the CV characteristics of the 15 nm low-Si_3N_4 device with irradiation bias $V_g = 0$ V. The flatband voltage shifts ($\Delta V_{\rm fb}$) and midgap voltage shifts ($\Delta V_{\rm mg}$) were nearly identical for all bias conditions and all devices. Thus, radiation-induced changes in the CV characteristics were predominantly due to radiation-induced oxide-trapped charge. The lack of significant change in interface trap density with irradiation most likely is due to the large pre-irradiation interface trap density in the 13 and 15 nm gate oxide devices.

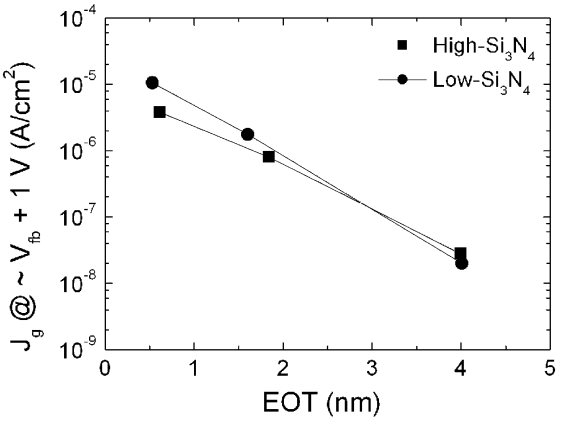

Fig. 3. Gate leakage current density ($\mathrm{J_g}$) at $\mathrm{V_{fb}} + 1$ V for low- and high-Si_3N_4 HfSiON devices with physical film thicknesses$\sim 15, 6$, and 2 nm.

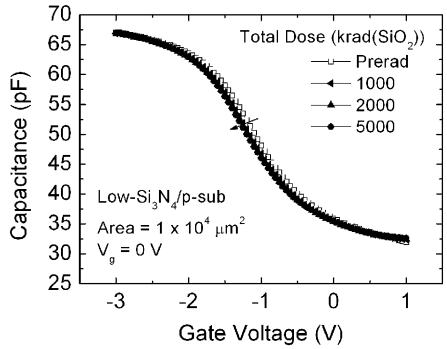

Fig. 4. 1-MHz capacitance–voltage characteristics for a p-substrate low-Si_3N_3 ($Hf_{0.6}Si_{0.2}ON_{0.2}$) film MOS capacitor irradiated with $\mathrm{V_g} = 0$ V to 5000 krad(SiO_2).

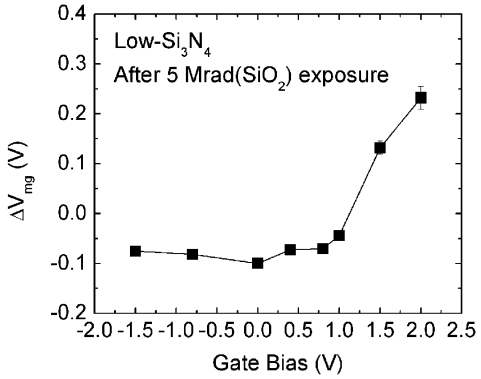

Fig. 5. ΔV_{mg} as a function of gate bias during irradiation for 15 nm low-Si_3N_4 ($Hf_{0.6}Si_{0.2}ON_{0.2}$) Si MOS devices irradiated to 5 Mrad(SiO_2).

Fig. 5 shows ΔV_{mg} as a function of dose for the 15 nm low-Si_3N_4 devices irradiated to 5 Mrad(SiO_2) under various bias conditions. We observe similar changes in ΔV_{mg} for gate biases ranging from -1.5 to 1 V, with larger positive shifts occurring for gate biases of 1.5 and 2 V. The lack of significant bias dependence at moderate gate biases suggests a relatively uniform distribution of bulk charge traps, similar to previous work on hafnium silicate films [8]. The charge centroid is not affected significantly at low electric fields due to the low mobility of holes in hafnium silicate and/or high bulk oxide-trap density [24]. The similar levels of ΔV_{mg} for devices irradiated

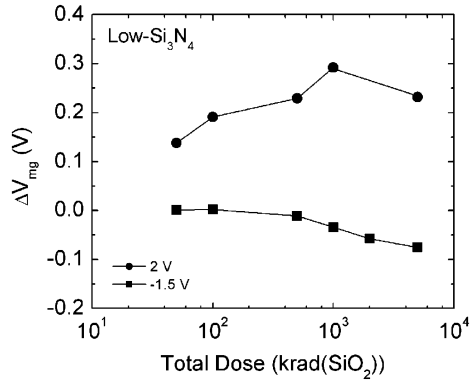

Fig. 6. ΔV_{mg} versus total dose for 15 nm low-Si_3N_4 ($Hf_{0.6}Si_{0.2}$ $ON_{0.2}$) Si MOS devices irradiated to 5 Mrad(SiO_2), with$V_g = 2$ and -1.5 V during irradiation.

with different biases may also be the consequence of a balance of electron and hole trapping in these nitrided Hf silicates. Previous work has shown that HfO_2 dielectric films are more susceptible to electron trapping than SiO_2 due to the large pre-irradiation bulk trap density [12]. Also, nitrided SiO_2 is known to contain both electron and hole traps [25], [26].

The exceptions to the lack of bias dependence occur only at higher positive bias conditions (1.5 and 2 V). Fig. 6 shows ΔV_{mg} versus total dose for positive and negative bias conditions. The value of ΔV_{mg} decreases monotonically for the negatively biased device, indicating net positive charge in the oxide. In contrast, the positively biased device shows primarily electron trapping, although the turnaround at higher doses shows that the net positive shift reflects an increasing amount of hole trapping relative to electron trapping at the highest doses.

At the higher positive voltages during irradiation, the Si surface layer is in inversion, and significant electron tunneling occurs. Constant voltage stress (CVS) experiments revealed that electron injection during irradiation causes significant amounts of electron trapping at the higher dose levels, due to the additional time under bias for these (but not lower) bias conditions. As we show below, the net electron trapping in Fig. 6 under large positive bias is a combination of electron injection and radiation-induced charge trapping. These combined effects are increasingly important in thin high-k dielectric layers [9], [12].

Figs. 7 and 8 compare the total-dose responses of the low- and high-Si_3N_4 films with positive and negative irradiation biases. The radiation responses of the films are similar for the negative bias case; the low-Si_3N_4 films show slightly enhanced levels of charge trapping relative to the high-Si_3N_4 film. However, the positively biased devices behaved differently: the high-Si_3N_4 film did not exhibit significant levels of electron trapping after irradiation, so the midgap voltage shift was negative due to net positive charge trapping.

C. Constant Voltage Stress

As demonstrated from the irradiation results, a significant amount of electron trapping occurs in the low-Si_3N_4 films only at relatively high positive gate biases during irradiation. CVS tests show that the positive gate bias induces considerable electron trapping via electron injection from the substrate. Fig. 9

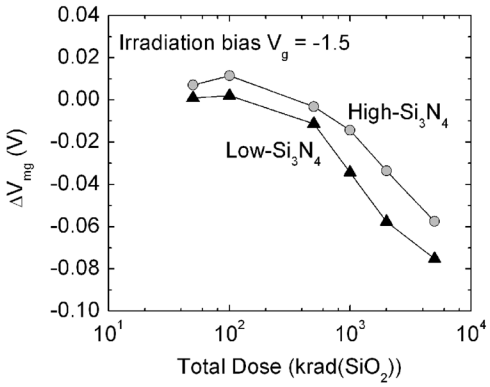

Fig. 7. $\Delta V_{\rm mg}$ versus total dose for 15 nm low-Si_3N_4 ($Hf_{0.6}Si_{0.2}ON_{0.2}$) and 13 nm high-Si_3N_4 ($Hf_{0.3}Si_{0.4}ON_{0.4}$) Si MOS devices irradiated to 5 Mrad(SiO_2) with$V_g = -1.5$ V.

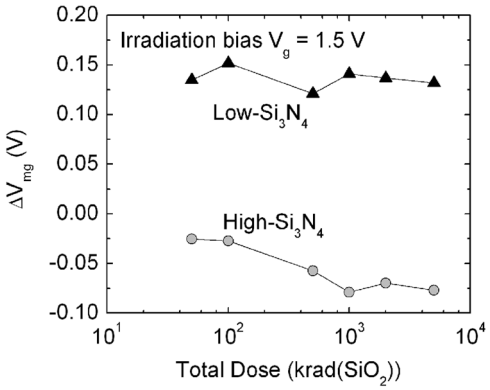

Fig. 8. $\Delta V_{\rm mg}$ versus total dose for 15 nm low-Si_3N_4 ($Hf_{0.6}Si_{0.2}ON_{0.2}$) and 13 nm high-Si_3N_4 ($Hf_{0.3}Si_{0.4}ON_{0.4}$) Si MOS devices irradiated to 5 Mrad(SiO_2) with $\mathrm{V_g} = 1.5$ V.

shows $\Delta V_{\rm mg}$ for the low-Si_3N_4 film stressed with various positive biases for times similar to irradiation times. Clearly, the amount of electron trapping is larger for higher stress voltages. In addition, the initial increase in $\Delta V_{\rm mg}$ makes up the majority of the total shift, consistent with the positive bias irradiation results. The sudden increase in $\Delta V_{\rm mg}$ after the initial stress interval of $\sim$100 s is followed by more gradual increases with stress time. This may be due to the presence of a higher density of defects near the high-k/Si interface. The HfSiON/Si MOS structure contains a thin interfacial layer of SiON between the high-k film and Si substrate. High densities of defects such as O vacancies are ideal trap sites for electrons/holes in these nitride-rich oxynitride layers [27], [28]. Electrons fill these traps before reaching the trap sites located deeper in the bulk oxide. The band diagram in Fig. 10 illustrates the electron trapping from substrate injection under positive gate bias. Negative gate voltages did not cause hole injection since the barrier height for hole tunneling is higher than for electrons. The valence band offset for HfSiON and Si is $\sim$3.7 eV, whereas the conduction band offset is $\sim$2.4 eV.

Fig. 11 demonstrates the CVS data of the high- and low-Si_3N_4 devices stressed for times varying from 1 to 10^5 seconds. We observe large initial $\Delta V_{\rm mg}$ even after 1 s. There is also a large increase in $\Delta V_{\rm mg}$ after 10^4 s, as the injected electrons fill the bulk oxide traps. These results are consistent

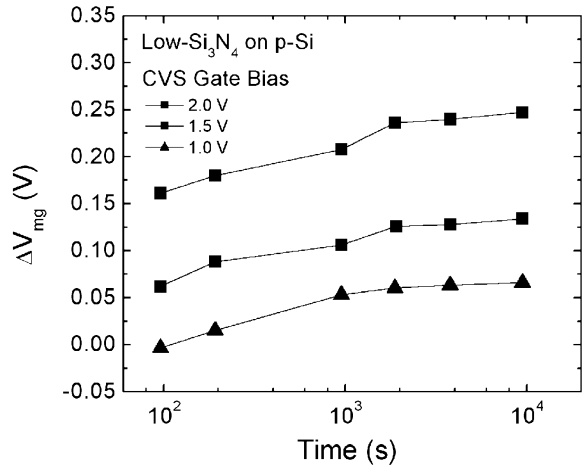

Fig. 9. $\Delta V_{\rm mg}$ versus stress time for 15 nm low-Si_3N_4 ($Hf_{0.6}Si_{0.2}$ ON $_{0.2}$) Si MOS devices stressed with $\mathrm{V_g} = 1, 1.5$, and 2 V at room temperature.

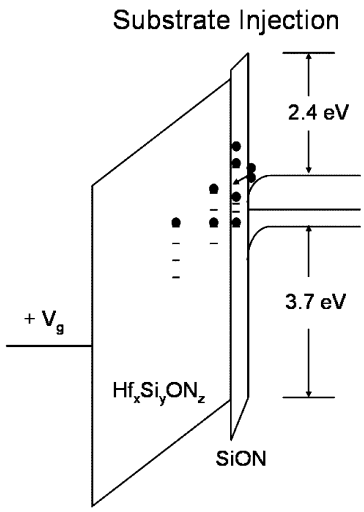

Fig. 10. Energy band diagram illustrating substrate electron injection for a p-substrate device under positive gate bias.

with the injected electrons filling the traps near the oxynitride interfacial layer before reaching the bulk oxide traps.

Additionally the CV characteristics showed no significant change in interface trap densities after CVS. This result differs from previous work on p-substrate HfO_2 capacitors that showed significant interface trap formation after CVS [12]. However the HfO_2 devices in that work had much lower pre-irradiation interface trap charge density ($N_{\rm it} < 1 \times 10^{11}$ cm^{-2}) than the devices here [12]. The nitride layers prevent H diffusion into the interfacial transition regions, thereby inhibiting interface trap formation; however, this may also limit one's ability to passivate Si dangling bonds at the interface during processing [3], [29].

The differences in the chemical structures of the two films evidently cause the differences in the radiation and CVS results. The "The low-Si_3N_4 content film chemically phase separates after 900°C annealing, containing crystalline HfO_2 and noncrystalline SiO_2 [17]. Crystalline HfO_2 contains grain boundaries that behave as electron trap sites [24]. The increased electron trapping in crystalline HfO_2 is primarily associated with O vacancies, which are clustered at internal grain boundaries

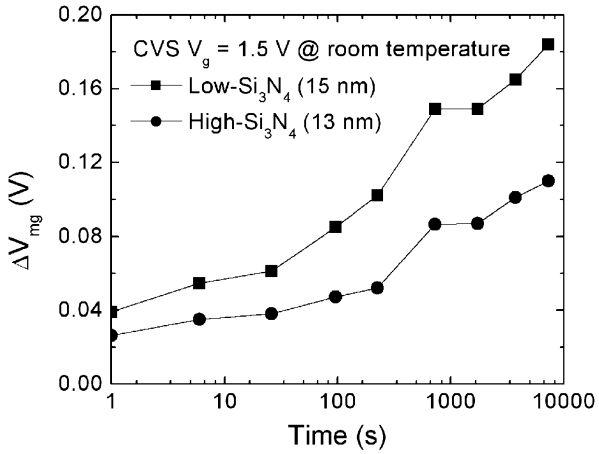

Fig. 11. $\Delta V_{\rm mg}$ versus stress time for 15 nm low-Si_3N_4 ($Hf_{0.6}Si_{0.2}$ $ON_{0.2}$) and 13 nm high-Si_3N_4 ($Hf_{0.3}Si_{0.4}ON_{0.4}$) Si MOS devices with $V_g = 1.5$ V during constant voltage stress at room temperature.

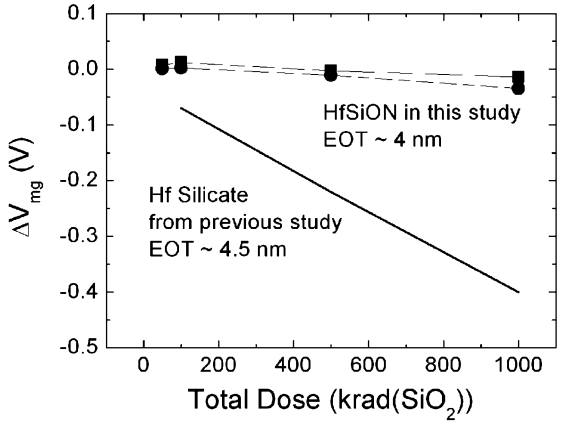

Fig. 12. $\Delta V_{\rm mg}$ versus total dose for the HfSiON devices ($\rm EOT = 4$ nm) in this report and Hf silicate devices from a previous study [12] ($\rm EOT = 4.5$ nm) with the same capacitor areas.

[27]. Conversely, the high-Si_3N_4 content film remains non-crystalline after the 900°C anneal and contains fewer trap sites due to the absence of grain boundary defects. The reduced defect generation rate under X-ray irradiation is similar to SiO_2, consistent with a chemical self-organization that minimizes percolation of bond-strain preventing chemical phase separation [17]. Thus, the high-Si_3N_4 content film exhibits reduced charge trapping even at high positive bias conditions.

D. Comparison With HF Silicate

Fig. 12 compares the worst-case irradiation results for the HfSiON devices in this study with Hf silicate devices from a previous study [8]. The $\Delta V_{\rm mg}$ curves of the Hf silicate devices in Fig. 12 are linear fits from data reported in [8]. They have similar dimensions (area $= 1 \times 10^{-4}$ cm^2 and $\rm EOT = 4.5$ nm) as the devices in this work. The Hf silicate devices also had a high pre-irradiation interface trap density ($N_{\rm it} \sim 2 \times 10^{12}$ cm^{-2}). They displayed large CV hysteresis (> 100 mV) after baking at 150°C [8]. These similar qualities allow for a fair comparison of their radiation responses.

The radiation-induced net oxide-charge densities ($\Delta N_{\rm ot}$) as projected to the Si/SiO_2 interface were estimated from [28]:

$$\Delta N{\rm ot} = -\frac{C{\rm ox}\Delta V{\rm mg}}{qA} \tag{2}$$

where $\Delta N_{\rm ot}$ is the change in oxide-trap charge density, $C_{\rm ox}$ is the oxide capacitance, $-q$ is the electron charge, and A is the capacitor area. After exposure to a total dose of 1000 krad(SiO_2) with $V_g = -1.5$ V, $\Delta N_{\rm ot} = 7.7 \times 10^{10}$ cm^{-2} and 2.1×10^{11} cm^{-2} for the high- and low-Si_3N_4 content devices, respectively, while $\Delta N_{\rm ot} = 1.2 \times 10^{12}$ cm^{-2} for the Hf silicate devices [8]. Hence, the amorphous high-Si_3N_4 film displays ~16× less $\Delta N_{\rm ot}$ relative to the Hf silicate devices in [8]. With the exception of electron trapping at the highest applied electric fields, the low-Si_3N_4 content film still demonstrates improved charge trapping characteristics relative to the Hf silicate films, with $\Delta N_{\rm ot} \sim 5.7\times$ less, despite the presence of nano-crystalline HfO_2 grains. The high-Si_3N_4 content film is similar to an Hf silicate film due to its amorphous structure. However, the improvement exhibited by the low-Si_3N_4 content films relative to the Hf silicate films is noteworthy, since crystalline HfO_2 has higher defect density and greater charge trapping than high quality Hf silicates [27]

The large pre-irradiation interface-trap density likely influences the irradiation results in both the HfSiON devices here and the Hf silicate devices from [8]. The effects of the high pre-irradiation $N_{\rm it}$ are similar to the saturation of interface traps at higher doses in SiO_2 due to the exhaustion of precursor defects [28]. Nevertheless the sizeable reduction in the radiation-induced net oxide-trap charge indicates the advancement in fabrication processes of Hf alloy MOS devices since 2002, when results for an earlier generation of Hf silicate devices were reported [8]. The results indicate the promise of nitrided Hf silicates for potential future use in radiation environments.

E. Bias-Temperature Stress

We further investigate the reliability of these films with bias-temperature stress experiments. The 2 nm films displayed larger shifts in midgap voltage relative to the thicker films. Therefore, the following discussion focuses on results of these thinner films. Bias-temperature stress tests were performed on n-type substrate devices with applied gate biases ranging from -2 to 2 V (~ -11 to 9 MV/cm). The oxides break down quickly for positive biases > 1 V. Fig. 13 illustrates $\Delta V_{\rm mg}$ as a function of stress temperature for both types of film compositions. Both types of films exhibited electron trapping under negative bias-temperature stress (NBTS) and hole trapping under positive bias-temperature stress (PBTS).

The NBTI results are unlike behavior typically found in thin HfO_2 devices, where positive interface and oxide trapped charge generation dominate [10], [11]. NBTS induces electron trapping that is likely caused by electron injection from the gate for the devices in this report. The electric fields applied during NBTS here are significantly higher than the values used in previous experiments on HfO_2/SiON devices that produced negative shifts in $\Delta V_{\rm mg}$, where V_g varied from ±1–3 MV/cm [10], [11]. However we found no measurable change in $\Delta V_{\rm mg}$ for smaller values of gate bias. Moreover CVS performed at room temperature with similar gate biases and stress times as in the NBTS tests

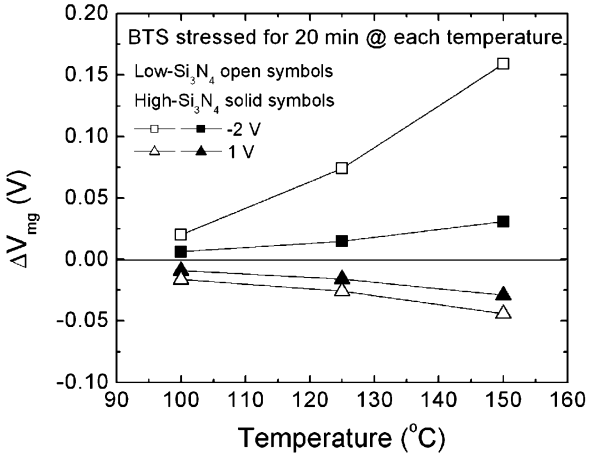

Fig. 13. $\Delta V_{\rm mg}$ versus stress temperature for 2 nm low-Si_3N_4 ($Hf_{0.6}Si_{0.2}ON_{0.2}$) and high-Si_3N_4 ($Hf_{0.3}Si_{0.4}ON_{0.4}$) Si MOS devices with BTS bias $V_g = -2$ and 1 V. Each device was stressed for 20 min at each temperature. C–V characteristics were measured after each stress interval when the device returned to room temperature.

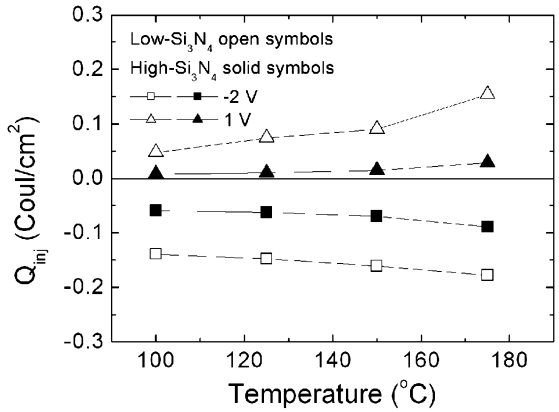

Fig. 14. $Q_{\rm inj}$ as a function of temperature for the low- and high-Si_3N_4 devices with BTS bias $V_g = -2$ and 1 V. The $Q_{\rm inj}$ represents injected charge after 20 min stress at each temperature.

produced negligible change in $\Delta V_{\rm mg}$ (not shown here). Therefore the amount of charge trapping depends strongly on temperature.

The amount of charge trapping depends on how much charge is injected during the stress. The gate injection current is likely caused by Fowler-Nordheim (F-N) and trap-assisted tunneling. The F-N current results in electron trapping via gate injection in SiO_2 -based MOS capacitors at high electric fields (> 6 MV/cm) [31]. Studies also show that the F-N emission rate increases with increasing temperature (in the range of 25–400°C) [32]. Fig. 14 illustrates the injected charge from each temperature stress for the HfSiON devices. We observe increasing charge injection with increasing temperature. Fig. 15 shows the F-N plot for a 2 nm low-Si_3N_4 content device at room temperature and at 150°C. The devices exhibit F-N tunneling at the higher gate biases (approaching -2 V). The higher magnitude of the curve for the device at 150°C also indicates the higher F-N emission rate at elevated temperature.

The enhanced levels of charge trapping and current levels observed in the low-Si_3N_4 film, which contains more defect states than the high-Si_3N_4 film, also suggest that trap-assisted

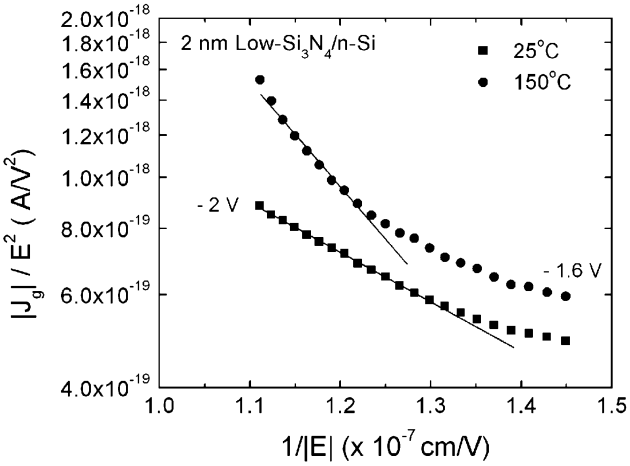

Fig. 15. $|J_g|/E^2$ versus $1/|E|$ for a 2 nm low-Si_3N_4/n-Si device at room temperature and 150°C.

tunneling is an additional mechanism for the charge trapping. Trap-assisted tunneling contributes to the total leakage current in high-k dielectrics more substantially than in SiO_2 due to the higher density of post-process defect states in high-k materials [23].

The results indicate that these HfSiON/Si devices are less sensitive to bias temperature stress than previous HfO_2 devices [10]–[12]. Very large electric fields that exceed typical operating voltages are required to cause charge injection from the gate. While the charge trapping depends strongly on temperature, the sources of bias-temperature stress degradation observed here are different than typical NBTI mechanisms. Unlike the HfO_2 devices in [10]–[12], the HfSiON devices in this study were not treated with a hydrogen-containing (e.g., forming gas) anneal, which is reflected by the larger post-process interface trap density ($N_{\rm it} \sim 5 \times 10^{11}$ cm^{-2}) for the devices used here. Because NBTI is sensitive to hydrogen [10]–[16], this may account for at least some of the difference in response. The challenge in device processing is to introduce enough hydrogen to passivate the dangling bonds at the interface, without introducing so much that one sees radiation-induced interface-trap buildup and NBTI [10]–[16].

V. Conclusion

We have examined the total-dose irradiation response of low- and high-Si_3N_4 content Hf Si oxynitride on Si MOS devices. We found significant electron trapping in the low-Si_3N_4 content devices, but the high-Si_3N_4 content devices exhibited relatively little electron trapping. CVS experiments showed that positive bias caused considerable electron injection (from the substrate), especially in the low-Si_3N_4 content devices. Furthermore, by comparing the radiation response and CVS results of the low- and high-Si_3N_4 content devices, we conclude that electron trap sites originate from the grain boundary-induced defect states in the HfO_2 nano-grains in the chemically phase-separated low-Si_3N_4 film. Both types of devices showed considerable reduction in total-dose-induced net oxide charge relative to Hf silicate devices, with $\Delta N_{\rm ot}$ approximately 16× less for the high-Si_3N_4 content device after 1 Mrad(SiO_2) exposure.

High electric fields (-11 and 4 MV/cm) were required to induce electron/hole trapping via gate injection. Furthermore, the

charge trapping only occurred for stress at elevated temperatures (100–175°C). Consistently, the charge injection increases with increasing temperature. Low-Si_3N_4 content devices exhibit enhanced degradation from bias-temperature stress relative to the high-Si_3N_4 content devices. Both types of HfSiON films exhibit improved radiation hardness relative to previous Hf silicate devices [8]. They also show improvement in bias-temperature reliability with respect to HfO_2 based devices [10]–[12]. However the reduced instability possibly comes at the expense of higher post-process $N_{\rm it}$. Thus with further improvements to reduce the post-process interstate densities, HfSiON is a promising alternative to SiO_2 as the gate dielectric in advanced MOS devices.

ACKNOWLEDGMENT

The authors would like to thank Prof. L. Feldman and Prof. S. Pantelides for insightful discussions, and D. Loveless for his assistance in designing the test board.

REFERENCES

[1] G. Ribes, J. Mitard, M. Denais, S. Bruyere, F. Monsieur, C. Parthasarathy, E. Vincent, and G. Ghibaudo, "Review on high-k dielectrics reliability issues," *IEEE Trans. Dev. Mater. Reliab.*, vol. 5, no. 1, pp. 5–19, Mar. 2005.

[2] P. Punchaipetch, T. Okamoto, H. Nakamura, Y. Uraoka, T. Fuyuki, and S. Horii, "Effect of nitrogen on electrical and physical properties of polyatomic layer chemical vapor deposition $HfSi_xO_y$ gate dielectrics," *Jpn. J. Appl. Phys.*, vol. 43, pp. 7815–7820, 2004.

[3] M. Saitoh, M. Terai, N. Ikarashi, H. Watanabe, S. Fujieda, T. Iwamoto, T. Ogura, A. Morioka, K. Watanabe, T. Tatsumi, and H. Watanabe, "1.2 nm HfSiON/SiON stacked gate insulators for 65-nm-node MISFETs," *Jpn. J. Appl. Phys.*, vol. 44, pp. 2330–2335, 2005.

[4] S. Sayan, N. V. Nguyen, J. Ehrstein, J. J. Chambers, M. R. Visokay, M. A. Quevedo-Lopez, L. Colombo, D. Yoder, I. Levin, D. A. Fischer, M. Paunescu, O. Celik, and E. Garfunkel, "Effect of nitrogen on band alignment in HfSiON gate dielectrics," *Appl. Phys. Lett.*, vol. 87, 2005, article no. 212905.

[5] M. R. Visokay, J. J. Chamber, A. L. P. Rotondaro, R. Kuan, L. Tsung, M. Douglas, M. J. Bevan, H. Bu, A. Shanware, and L. Colombo, "Properties of Hf-based oxide and oxynitride thin films," in *Proc. Int. Conf. Microelectron. Interf.*, 2002, pp. 127–129.

[6] J. A. Felix, J. R. Schwank, D. M. Fleetwood, M. R. Shaneyfelt, and E. P. Gusev, "Effects of radiation and charge trapping on the reliability of high-k gate dielectrics," *Microelectron. Reliab.*, vol. 44, pp. 563–575, 2004.

[7] T. Watanabe, M. Takayanagi, R. Iijima, K. Ishimaru, H. Ishiuchi, and Y. Tsunashimd, "Design guideline of HfSiON gate dielectrics for 65 nm CMOS generation," *VLSI Tech. Dig.*, pp. 19–20, 2003.

[8] J. A. Felix, D. M. Fleetwood, R. D. Schrimpf, J. G. Hong, G. Lucovsky, J. R. Schwank, and M. R. Shaneyfelt, "Total-dose radiation response of hafnium-silicate capacitors," *IEEE Trans. Nucl. Sci.*, vol. 49, no. 6, pp. 3191–3196, Dec. 2002.

[9] J. A. Felix, M. R. Shaneyfelt, J. R. Schwank, P. E. Dodd, D. M. Fleetwood, X. J. Zhou, and E. P. Gusev, , E. Gusev, Ed., "The Effects of Radiation and Charge Trapping on the Reliability of Alternative Gate Dielectrics," in *Defects in Advanced High-κ Dielectric Nano-Electronic Semiconductor Devices*. Amsterdam, The Netherlands: Springer-Verlag, 2006, pp. 299–322.

[10] X. J. Zhou, L. Tsetseris, S. N. Rashkeev, D. M. Fleetwood, R. D. Schrimpf, S. T. Pantelides, J. A. Felix, E. P. Gusev, and C. D'Emic, "Negative bias-temperature instabilities in Metal—Oxide—Silicon devices with SiO_2 and SiO_xN_y/HfO_2 gate dielectrics," *Appl. Phys. Lett.*, vol. 84, pp. 4394–4396, 2004.

[11] X. J. Zhou, D. M. Fleetwood, J. A. Felix, E. P. Gusev, and C. D'Emic, "Bias-temperature instabilities and radiation effects in MOS devices," *IEEE Trans. Nucl. Sci.*, vol. 52, pp. 2231–2238, 2005.

[12] X. J. Zhou, D. M. Fleetwood, L. Tsetseris, R. D. Schrimpf, and S. T. Pantelides, "Effects of switched-bias annealing on charge trapping in HfO_2 gate dielectrics," *IEEE Trans. Nucl. Sci.*, vol. 53, pp. 3636–3643, 2006.

[13] K. O. Jeppson and C. M. Svennson, "Negative bias stress of MOS devices at high electric fields and degradation of NMOS devices," *J. Appl. Phys.*, vol. 48, pp. 2004–2014, 1977.

[14] D. M. Fleetwood, X. J. Zhou, L. Tsetseris, S. T. Pantelides, and R. D. Schrimpf, R. E. Sah, M. J. Deen, J. Zhang, J. Yota, and Y. Kamakura, Eds., "Hydrogen model for negative-bias temperature instabilities in MOS gate insulators," in *Proc. Silicon Nitride and Silicon Dioxide Thin Insulating Films and Other Emerging Dielectrics VIII*, 2005, pp. 267–278.

[15] D. K. Schroder and J. A. Babcock, "Negative bias temperature instability: A road to cross in deep submicron CMOS manufacturing," *J. Appl. Phys.*, vol. 94, pp. 1–18, 2003.

[16] L. Tsetseris, X. J. Zhou, D. M. Fleetwood, R. D. Schrimpf, and S. T. Pantelides, "Physical mechanisms of negative-bias temperature instability," *Appl. Phys. Lett.*, vol. 86, 2005, art. no. 142103.

[17] G. Lucovsky, H. Seo, S. Lee, L. B. Fleming, M. D. Ulrich, J. Lüning, P. Lysaght, and G. Bersuker, "Intrinsic electronically-active defects in transition metal elemental oxides," *Jpn. J. Appl. Phys.*, vol. 46, pp. 1899–1909, 2007.

[18] P. S. Winokur, J. R. Schwank, P. J. McWhorter, P. V. Dressendorfer, and D. C. Turpin, "Correlating the radiation response of MOS capacitors and transistors," *IEEE Trans. Nucl. Sci.*, vol. 31, no. 6, pp. 1453–1460, Dec. 1984.

[19] R. Choi, S. J. Rhee, J. C. Lee, B. H. Lee, and G. Bersuker, "Charge trapping and detrapping characteristics in hafnium silicate gate stack under static and dynamic stress," *IEEE Electron Dev. Lett.*, vol. 26, no. 3, pp. 197–199, Mar. 2005.

[20] C. D. Young, Y. Zhao, M. Pendley, B. H. Lee, K. Matthews, J. H. Sim, R. Choi, G. A. Brown, R. W. Murto, and G. Bersuker, "Ultra-short pulse current-voltage characterization of the intrinsic characteristics of high-k devices," *Jpn. J. Appl. Phys.*, vol. 44, pp. 2437–2440, 2005.

[21] D. M. Fleetwood, M. R. Shaneyfelt, W. L. Warren, J. R. Schwank, T. L. Meisenheimer, and P. S. Winokur, "Border traps: Issues for MOS radiation response and long-term reliability," *Microelectron. Reliab.*, vol. 35, pp. 403–428, 1995.

[22] D. M. Fleetwood and N. S. Saks, "Oxide, interface, and border traps in thermal, N_2O, and N_2O-nitrided oxides," *J. Appl. Phys.*, vol. 79, pp. 1583–1594, 1996.

[23] M. Houssa, M. Tuominen, M. Naili, V. Afanas'ev, A. Stesmans, S. Haukka, and M. M. Heyns, "Trap-assisted tunneling in high permittivity gate dielectric stacks," *J. Appl. Phys.*, vol. 87, pp. 8615–8620, 2000.

[24] M. R. Shaneyfelt, D. M. Fleetwood, J. R. Schwank, and K. L. Hughes, "Charge yield for 10-keV X-ray and cobalt-60 irradiation of MOS devices," *IEEE Trans. Nucl. Sci.*, vol. 38, no. 1, pp. 1187–1194, Dec. 1991.

[25] S. L. Miller and P. J. McWhorter, "A predictive model of electron and hole decay in SiN-SiO_2 nonvolatile memory transistors experiencing arbitrary thermal environments," *J. Appl. Phys.*, vol. 70, pp. 4569–4576, 1991.

[26] V. A. K. Raparla, S. C. Lee, R. D. Schrimpf, D. M. Fleetwood, and K. F. Galloway, "A model of radiation effects in nitride-oxide films for power MOSFET applications," *Solid State Electron.*, vol. 47, pp. 775–783, 2003.

[27] G. Lucovsky, D. M. Fleetwood, S. Lee, H. Seo, R. D. Schrimpf, J. A. Felix, J. Lüning, L. B. Fleming, M. Ulrich, and D. E. Aspnes, "Differences between charge trapping states in irradiated nano-crystalline HfO_2 and non-crystalline Hf silicates," *IEEE Trans. Nucl. Sci.*, vol. 53, no. 6, pp. 3644–3648, Dec. 2006.

[28] J. M. Benedetto, H. E. Boesch, Jr., and F. B. McLean, "Dose and energy dependence of interface trap formation in colbalt-60 and X-ray Environments," *IEEE Trans. Nucl. Sci.*, vol. 35, no. 1, pp. 1260–1264, Dec. 1988.

[29] D. M. Fleetwood, R. A. Reber, P. J. McWhorter, P. S. Winokur, M. R. Shaneyfelt, and J. R. Schwank, "New insights into radiation-induced oxide-trap charge through thermally stimulated-current measurement and analysis," *IEEE Trans. Nucl. Sci.*, vol. 39, no. 6, pp. 2192–2203, Dec. 1992.

[30] K. L. Brower, "Kinetics of H_2 passivation of P_b centers at the (111) Si-SiO_2 interface," *Phys. Rev. B.*, vol. 38, pp. 9657–9666, 1988.

[31] J. F. Zhang, S. Taylor, and W. Eccleston, "Electron trap generation in thermally grown SiO_2 under Fowler-Nordheim stress," *J. Appl. Phys.*, vol. 71, pp. 725–734, 1992.

[32] G. Pananakakis, G. Ghibaudo, R. Kies, and C. Papadas, "Temperature dependence of the Fowler-Nordheim current in metal-oxide-degenerate semiconductor structures," *J. Appl. Phys.*, vol. 78, pp. 2635–2641, 1995.