Total Dose Failures in Advanced Electronics from Single Ions*

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Abstract

Hard errors from single heavy ions have been reported in advanced commercial CMOS memories. We examine the physical interactions of ions with MOS gate oxides--charge generation, recombination, transport and trapping. We also consider device and circuit characteristics. We conclude that hard errors from single ions are to be expected, and should not be considered surprising.

INTRODUCTION

In 1991, Koga et al[1] first reported stuck bits in commercial SRAMs tested with heavy ions. In 1992, Dufour et al.[2] also reported stuck bits in heavy ion tests. Dufour and coworkers argued that these hard errors are due to total dose effects from one or two ions incident on the gate oxide of sensitive transistors. They showed that the errors occurred in random, isolated bits and that they could be annealed by exposure to UV light or by raising the temperature. The question of total dose failures from single ions was first examined by Oldham and McGarrity in 1981,[3] who concluded then that such failures were a long way off. Since several generations of commercial SRAMs have come and gone since then, and since such failures have now been reported, it seems reasonable to take another look at the physical interactions contributing to the total dose response of advanced memories exposed to heavy ions.

In this paper, we will first discuss the heavy ion experiments with emphasis on the response of the memory cell. So far permanently failed bits have been reported only in commercial SRAMs with 4T cells and resistive loads. Both Koga et al[1] and Dufour et al[2] have observed hard errors in 1M SRAMs of this type produced by Hitachi and by Micron. There is apparently also unpublished data[4] suggesting the similar effects in DRAMs however. In both cases, the memory cell itself is basically NMOS, although the circuits are described as CMOS because of the peripheral circuitry. We will consider the features of the NMOS circuits that make them relatively sensitive to total dose effects. We will conclude that this is a complicated statistical problem. The pass gate devices are smaller and presumeably more sensitive, but they are normally irradiated without bias. The latch devices are larger, but they are sometimes irradiated with the gate held at 5V. It has also been shown[5,6] that the response of a transistor to an ion strike can depend on where in the active area of the device the hit occurs. When all the statistical factors (device threshold variation, randomly distributed ion strikes, device types and voltages) are considered, it is likely that both latch and pass gate devices can contribute to the observed error rate. Second, we will discuss the physical mechanisms of the interaction of a heavy ion with the gate oxide of a transistor. Specifically, we will consider the generation, recombination, transport and trapping of ion-generated charge. The distribution of charge that results in the gate region will be highly nonuniform. Third we will discuss the impact of this nonuniform charge on the operating characteristics of the device. Finally, we will consider the likely effect of continued scaling in light of these results. We will conclude that reducing the oxide thickness will actually make future memories less sensitive to single ion total dose effects. Furthermore, the 4T cell is being abandoned by the industry for other reasons, so the natural evolution of the industry will probably eliminate this total dose problem eventually.

CIRCUIT CONSIDERATIONS AND HEAVY ION EXPERIMENTS

The permanent stuck bits (hard errors) reported by Dufour et al.[2] were observed first in the Micron Semiconductor 1M SRAM, but they have also been observed in a similar Hitachi SRAM. The basic cell, illustrated in Fig. 1, contains two poly-Si load resistors and four n-channel transistors. The sensitivity of this kind of 4T cell to heavy ion upset is well

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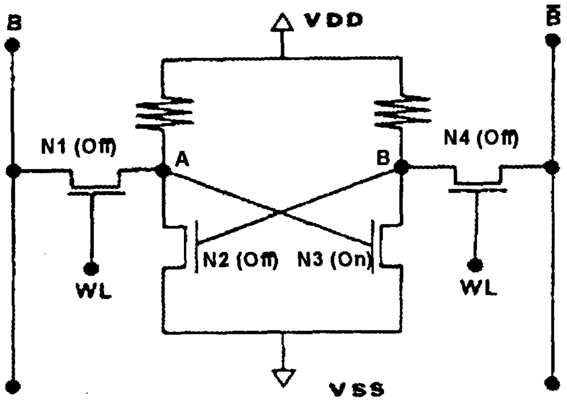

Figure 1: Schematic of 4T SRAM cell with resistive loads.

known. It was first pointed out by Diehl,[7] and several other authors [8,9,10] have also discussed the upset response of the 4T cell. The basic problem that might cause an upset is that if an ion strikes a high node (say A, in fig. 1) and pulls it down, the cell is disturbed for an extended period. The load resistance has to be large to limit the power consumption of the circuit, but it also then limits the current that can flow to restore the struck node. In this case, the cell eventually recovers to the correct state, but it may be read incorrectly until it does recover.

The most likely explanation of total dose failures from heavy ions in a 4T cell is closely related to the upset problem. Numerous papers have been presented in recent years in the Journal of Solid State Circuits which describe SRAMs developed by different semiconductor manufacturers.[11-30] Two of these give specific load resistance values for their SRAM,[17,30] and one other[26] gives the value the authors would have needed had they used a resistive load. The range of quoted resistance values for the 1M generation is 3 x 10^{12} Ω to 10^{13} Ω. That is, for typical 1M SRAMs, which operate at 5 V, the load resistor limits the current which can flow to about 1 pA, give or take a factor of two. We propose that the ion exposure damages one of the transistors, N1 or N2 or N3 or N4, to the point where it leaks 1 pA or more, causing the bit to become stuck. First let us consider the pass gate device N1, then we will consider the latch device N3. In Fig. 1, if the leakage current through device N1 is greater than the current that can flow through R1, then node A can never be charged up, and device N3 cannot be held on, hence the bit becomes stuck. Evidence for this mechanism can be obtained from further analysis of the experiments reported by Dufour et al[2]. Similarly if N3 is damaged, then the cell cannot be written to a state where B is held high.

The nominal ion fluence in those experiments was 2 x 10^6 particles/cm^2, and the chip area is 0.75 cm^2, so the total particle count was 1.5 x 10^6 ions/chip. According to sources at Micron,[31] the dimensions of the latch devices are 0.85 μm long by 1.90 μm wide (drawn). The pass gate devices are drawn 1.0 μm x 1.0 μm, but the birds beak encroachment is about 0.25 μm on each side. Thus the width of the thin gate oxide in the pass gate devices in reduced to only 0.5 μm. Then for a 1M SRAM, there are 1,048,576 cells with two pass gate devices and two latch devices. The total area of all the pass gate devices is 0.0105 cm^2 or 1.4% of the total chip area, which implies that 1.4% of the ions or 21,000 ions will strike the active area of pass gate devices. Similarly, the total area of the latch devices is 0.0339 cm^2 or 4.5% of the total chip area, implying that about 68,000 ions strike the active region of latch devices.

Using these numbers, one can then calculate the number of pass gate and latch devices struck by one ion, two ions, and so on. (This problem is similar to the so-called two-birthday problem, which is treated in many probability theory textbooks. For N people in a room, the probability that two of them have the same birthday is much higher then most people would guess until they do the calculation.) The simplest approach to the problem is to solve it numerically, dropping particles one at a time, randomly into two million bins. Thus, the first particle goes into a bin; the second particle has one chance in two million of landing in the same bin that already has a particle in it; the third particle has two chances in two million of landing in a bin with a particle already in it and so on. The 10,000th particle has a probability of about 0.005 of landing in a bin with a particle already in it. If one integrates the probability of multiple hits up to 21,000 particles for pass gate devices and 68,000 particles for latch devices, one obtains the results shown in Table I. Dufour et al. reported about 100 stuck bits for their typical exposure. Thus it seemed reasonable to conclude that most of the errors were due to double ion hits. However, more recent experiments were done at much lower fluences (down to 10^4 total particles) to eliminate double hits, and there are still significant numbers of errors. In addition, more recent exposures have resulted in higher error rates - perhaps 1000 stuck bits for the most sensitive die. Therefore errors due to single ions must contribute to the observed error rate.

TABLE 1

Pass Gate Devices	
zero hits	2,076,000
single hits	≈21,000
double hits	≈110
triple hits	< 1

Latch Devices	
zero hits	2,030,000
single hits	≈66,000
double hits	≈1100
triple hits	≈13
more than three hits	<< 1

The complexity of the statistical problem here (and in device threshold variation which is discussed later) make it likely that all possible variations -- pass gate devices, latch devices, single ions, double hits -- contribute to the observed error rate to some extent. In what follows, we try to quantify these effects as much as possible.

An obvious question is whether the stuck bits are stuck in their initial state, or the opposite state, or randomly distributed. In these experiments, there is no way to tell, unfortunately. These memories are relatively soft, so many of the bits are upset by exposure to 10^6 or so ions. When the RAM is checked for stuck bits at the end of the exposure, there is no way to tell what state the cell was really in when it became stuck. However, recent experiments have shed some light on this question, nevertheless.

The SRAMs are normally tested with a 5V power supply, and hard error cross sections for such tests are shown in Fig. 2a. Generally the results are 10^{-6} to 10^{-4} cm^2, indicating one to 100 stuck bits per million incident particles regardless of LET. The memories can, however, also be tested in a standby, data retention mode with only a 2V power supply. These results are shown in Fig. 2b. Under this condition, no errors are observed except at the highest LET, so there is a clear voltage dependence to the effect. In Fig. 1, only transistor N3 is biased differently in the tests summarized in Fig. 2, so much of the damage causing stuck bits must be to the "on" latch device, N3 in our example. In this event, node B could not then be held high, so the bit would be stuck in its initial state. Next we consider the physical interactions of an ion with a gate oxide.

CHARGE DEPOSITION, TRANSPORT, AND TRAPPING

When an energetic ion passes through an insulator, a dense column of electron-hole pairs is created. Depending on the density of charge and applied field, some fraction of this charge will immediately recombine. This much has been known since the early years of this century, shortly after the discovery of radioactivity and α, β, and γ rays. Proper analytical techniques to describe this recombination process were at one time the subject of a controversy between Bragg[32] and Langevin.[33] This controversy was ultimately settled in Langevin's favor by Jaffe,[34] who developed what is still the definitive model for columnar recombination. Jaffe's model was first applied to MOS oxides by Ausman and McLean,[35] and it was first applied to total dose damage to oxides from ions by Oldham and McGarrity.[3] Since then it has also been used in a number of other studies.[36-38] The model is described in great detail in some of these studies,[3,36,37] so we will simply give the results of applying it to the ion experiments reported by Dufour et al.[2]

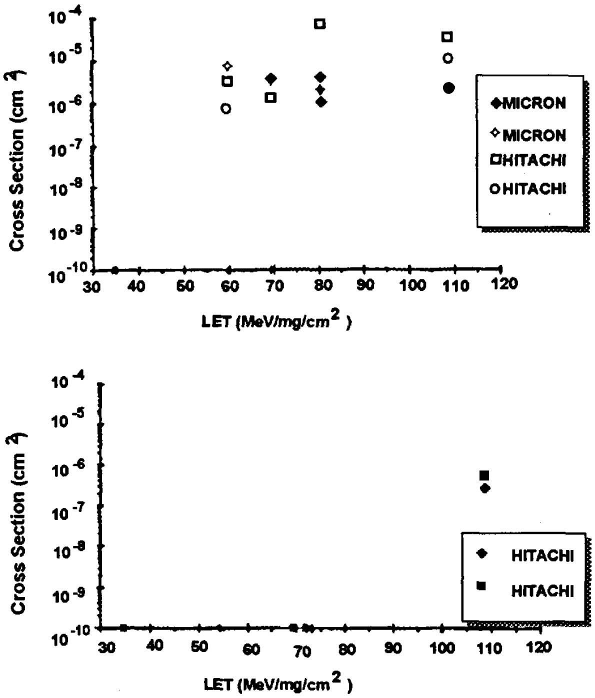

Figure 2: Measured hard error cross sections: (a) normal 5V operating voltage, and (b) 2V data retention mode.

The exposure condition we consider here is the following: Xe^{129} ions at 580 MeV incident at 48° on a 200 Å thick oxide. The LET for the ions in SiO_2 is then 64 MeV/mg/cm^2. If one assumes 17 eV per electron-hole pair, the line density of ionization is then 8.3×10^9 pairs/cm. For a 48° incidence on a 200 Å oxide, the total path length is about 285 Å, and there are initially about 23,500 charge pairs created. Solving the Jaffe equation numerically lends to a predicted fractional yield of about 0.005, or (only) 120 holes reaching the Si/SiO_2 interface for zero volts applied. This value of yield was calculated for a column with a Gaussian half-diameter, b, of 3.5 nm, a value obtained by Oldham in alpha particle experiments.[36,38] This value for b was obtained by empircally fitting a curve to experimental data taken with alpha particles.[3] However, using the same value of b for these higher LET ions leads to a greater ionization density at the center of the column than the total density of electrons present. So this b value cannot really be correct under all conditions, and certainly not here. The problem is that there is little experimental data to guide us in choosing a different value. Stapor[37] conducted the only measurements known to us of the yield for heavy ions in SiO_2, but only for normal incidence. In these experiments, the ions were incident at oblique angles, and the component of the field normal to the particle axis is known to be critical because it is what ultimately separates the positive and negative charges. Thus, it is difficult to know exactly how to scale Stapor's results to apply to these experiments.

For the off transistors, the model[3] calculates a yield of about 0.005 or 120 holes (only). However, Stapor's measurements were about a factor of two greater than the model predicted, so we used yield about 0.01 (240 holes) in the following analysis. For the latch devices (latches), the model predicts a yield of about 0.012, but we know that some correction is necessary here also.

To estimate this correction, some of us (the Matra group) performed a preliminary experiment, irradiating a MOS capacitor with Xe^{129} ions and with Co^{60} gamma radiation. This capacitor oxide is quite different from the memory devices, but it can be used to estimate yield. These results are shown in Fig. 3. Clearly the post-radiation curves are almost identical, so the damage mechanisms - probably mostly oxide trapped charge - must be the same. However, the doses are different.

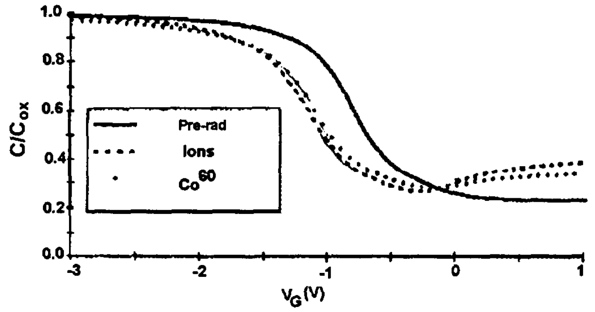

Figure 3: CV curves for ion and Co^{60} exposures, used to estimate charge yield for heavy ions in SiO_2.

For the Co^{60} exposure, the nominal dose was 29 krad. Following the standard analysis (ref. 35, for example), we have

$$\Delta V_T = \frac{-3.23x10^7 t_{ox}^2 D f(E) f_t}{W_o} \quad (1)$$

where D=29000 rad, $t_{ox} = 9 \times 10^{-6}$ cm, and W_o is the electron-hole pair creation energy (17 eV). The field dependent recombination, f(E), is taken to be 0.7 for 5V applied across a 900Å oxide, consistent with previous work (see for example,ref. 39). For ΔV_T (or, in this case ΔV_{FB}) about 350 mV, we can calculate $f_t \cong 0.056$.

Then for the ion experiment, the total flux is 1.16×10^8 particles/cm^2. The experimental conditions approximately match the memory tests, but not exactly. The ions was Xe^{129} at 11.3 MeV per nucleon, which implies LET = 54 MeV/mg/cm^2. The angle was 60°, leading to an estimate of 2.8×10^5 holes/ion produced initially, or 3.25×10^{13} holes/cm^2. Since ΔV_{FB} is 0.350V, Q works out to 8×10^{10} trapped holes/cm^2. That is,

$$f(E) f_t = \frac{8x10^{10} \text{ trapped holes}}{3.25x10^{13} \text{total holes}} = 0.0025$$

Since f_t was determined to be 0.056 in the Co^{60} exposure, f(E) = 0.044.

In the following analysis, we use f(E) = 0.044 or 1034 holes per ion reaching the interface for 5V applied in the SRAM. We recognize that this is a rough estimate, but it is the best we can do now, and it is good enough to illustrate the main points we wish to make.

Since the charge is generated with a highly nonuniform spatial distribution, the next step is to calculate the transport of the holes that escape recombination. The transport calculation works in the following way. First, 240 holes (or 1034 holes) are distributed randomly in a cylinder 100 Å in diameter. Second, the total field on each particle is calculated, including any applied field in addition to the repulsive force between each pair of holes. (Since pass gate devices are usually off, the applied field here is due only to work function differences.) Third, each hole is allowed to "hop" 10 Å parallel to the total field it sees. This treatment is consistent with the hole transport work of McLean and others,[39-42] which shows that holes transport in SiO_2 by hopping from shallow trap to shallow trap. The hopping is strongly field activated and 10 Å is a typical hopping distance. The difference here is that the field is nonuniform. After the charges hop the fields are recalculated, then the charges hop again and so on. When the holes reach the Si/SiO_2 interface they are either trapped or allowed to escape. Generally, the first charges to reach the interface become trapped and set up a space charge field which prevents any more charges from reaching the interface near the end of the ion track. Charges which reach the interface later are pushed out farther and farther by space charge fields. This situation is illustrated schematically in Fig. 4. In Fig. 5 we show

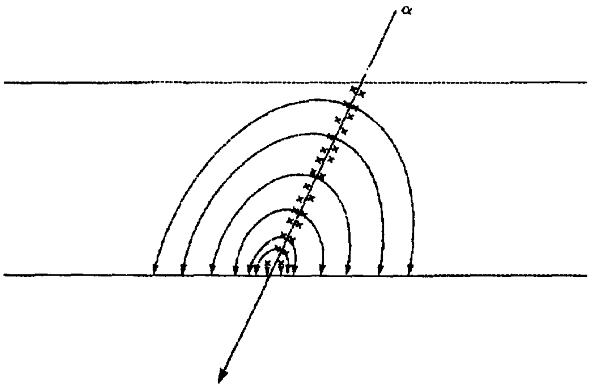

Figure 4: Schematic illustrating transport of holes to the interface after an ion strike in SiO_2.

typical results for the pass gate devices, and in Fig. 6 we show results for the latch devices.

In Fig 5a, we have assumed that 100% of the charges reaching the interface are trapped. The figure shows a top view of the interface where the ion entered the oxide above the point (20 nm, 0) and exited at the origin (45° incidence). Each dot represents one trapped hole. The full range of the plot is 0.5 μm which is the effective width of the pass gate device in the Micron 1M SRAM. Clearly, the spot of trapped charge covers almost the entire device width. Since the channel length is drawn 1.0 μm, it also covers a significant portion of the device length. The assumption in Fig. 3a that 100% hole trapping occurs is obviously conservative. The oxide is completely unhardened, so the real trapping efficiency is relatively high. In addition, the $E^{-1/2}$ dependence of the trapping efficiency implies heavy trapping, since no field except a work function is applied. But 100% is still a worst-case limit.

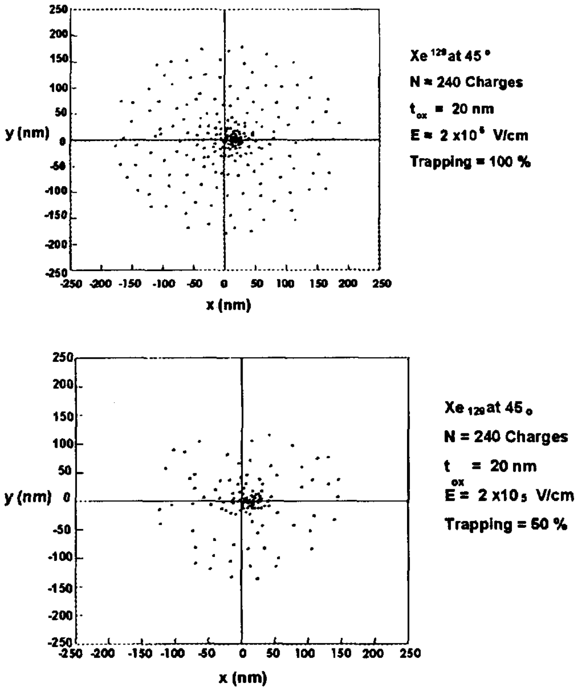

Figure 5a & 5b: Calculated charge trapping at interface in a pass gate device: (a) assuming 100% trapping, and (b) assuming 50% trapping.

To determine the effect of varying the trapping on this result, we repeated the calculation shown in Fig. 3a, except that when each hole reaches the interface, the random number generator is called to decide whether that hole is trapped or escapes. In Fig. 3b, the result is shown for nominal 50% trapping. The result is qualitatively similar to Fig. 3a except that the spot is smaller since removing some of the positive charge reduces the repulsive fields acting on the remaining charges. In this case the spot of trapped charge covers only about half the width of the device. Similarly, for still lower trapping efficiencies, the spot size continues to scale. Obviously as the trapping efficiency is reduced (that is, as the oxide is made harder) the spot size becomes smaller relative to the device and presumably less disruptive to the circuit. However, the density of trapped charge within the spot remain roughly constant, consistent with the idea that the transport is space charge limited.

In Fig. 6, we show results similar to Fig. 5, except that the field is 5V across a 200Å oxide, and the number of holes in the calculation is 1034. Here we are simulating the response of a latch device biased on. In Fig. 6a, the trapping efficiency is 100%, and in Fig. 6b 50% trapping is assumed. The differences between figures 5 and 6 are that the spots are smaller in Fig. 6 because the applied bias pushes the holes to the interface more quickly, and the density of charge is higher with a bias applied.

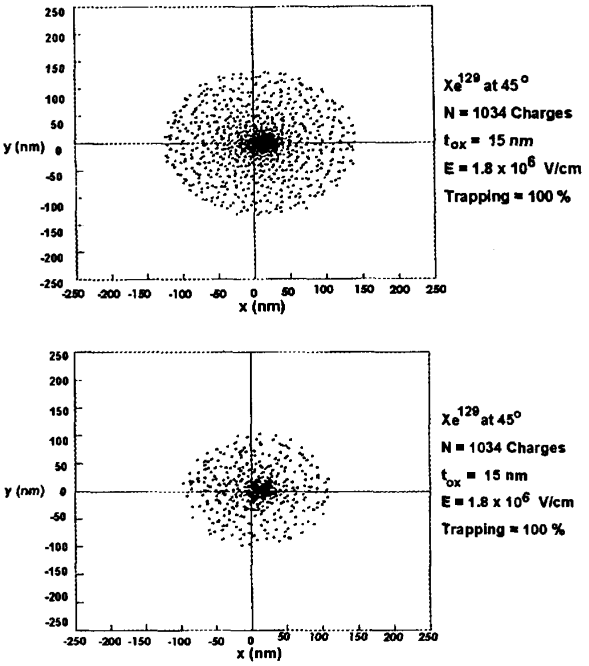

Figure 6a & 6b: Calculated charge trapping at interface of an "on" latch device, with 5V applied: (a) assuming 100% trapping, and (b) assuming 50% trapping.

DEVICE CHARACTERISTICS

Next we consider the baseline electrical characteristics of the individual devices and try to assess the impact on them of any of the trapped charge distributions shown in Fig. 5 or 6. Of the papers already cited that describe different SRAMs, five give nominal n-channel threshold voltages,[19,20,25,27,29] and the range of values is from 600 to 700 mV. For technology in the range of 0.8 to 1.0 µm, the typical subthreshold swing seems to be about 100 mV/decade of drain current.[20] And most manufacturers[13] have tried to set their zero-volt leakage current at 10^{-13} or 10^{-14} A for their n-channel devices. These characteristics are all reflected in the subthreshold I-V curve shown in Fig. 7. The curve in Fig. 7 is for a real commercial device similar (but not identical) to the Micron n-channel pass gate. The curve has been normalized to the same device width.

There are two key points about Fig. 7. First, the gate voltage that corresponds to 10^{-12} A is only about 100 mV. In other words, a shift of only 100 mV in the curve would increase the leakage current to about 10^{-12} A, which is roughly the condition needed to cause a bit to fail.

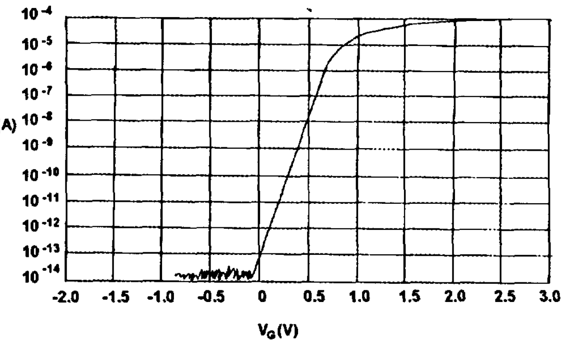

Figure 7: Nominal I-V characteristic for an n-channel transistor in a 4T cell.

Second, the curve in Fig. 7 is nominal, meaning that it represents the mean for the process. But there is some variation in V_T associated with the manufacturing process. Obviously devices shifted 2σ to the left in Fig. 7 will be more sensitive than those shifted 2σ to the right. So we need to estimate the σ associated with the manufacturing process. Studies of the variation of V_T in typical production processes have been presented.[43,44] Although many factors contributed to the total variation, it was found that the largest effect was from the threshold adjust implant.[43] (Other sources of variation can be significant across a large wafer, but they generally contribute much less variation across a single die or between adjacent cells.) For simplicity we focus on the threshold adjust implant in the following discussion. There is extensive literature on the performance of implanters.[45,46] Three sources of variation in implanter performance must be considered in discussing threshold voltage uniformity. First is the repeatability of the implant dose from wafer to wafer. One sigma variation in the range of 1% for a given implanter has been reported as typical.[45] (Implanter-to-implanter variation is much greater without careful calibration.)

Second, implant uniformity across a wafer typically is reported in the range of 1 to 2% (one sigma). However, this can be misleading. The data is typically taken with a four point probe which measures sheet resistance over macroscopic areas. The variation is often due to the fact that there is a systematic variation across the wafer. For instance, the left edge might have an implant dose a few percent below the mean, the right edge is a few percent above the mean dose, and only a line running down the center of the wafer actually receives the mean dose. Then the variation on a single die will be much less than on the wafer.

In addition to this macroscopic variation in dose, there is also a microscopic variation -- the third factor and the most important one for this discussion. Even if the implanter is perfectly tuned to eliminate macroscopic nonuniformity, adjacent transistors will still not receive exactly the same number of implanted atoms. For example, a typical threshold adjust implant might be designed to raise the threshold voltage about 0.45 V, from 0.25 V to 0.70 V.[47,48] The dose required to do this can be determined from the following equation:[48]

$$\Delta V_T = qN_I/C_{OX} \qquad (2)$$

For a 200 Å oxide, the implant dose would be about 5×10^{11} ions/cm^2. The active area of the pass gate devices in the Micron 1M SRAM is 5×10^{-9} cm^2, implying an average dose of 2500 ions/transistor. Now $\sigma = \sqrt{N} = 50$ atoms/transistor. That is, σ is 2% of the mean corresponding to about 10 mV. This variation is fundamental, and cannot be eliminated even in an "ideal" implanter. For a circuit with millions of transistors, the full range of data on a die would extend out at least ± 6 σ or ± 60 mV about the mean threshold. (Current et al.[49] have recently discussed implanter performance as a limiting factor in the production of increasing complex circuits.)

For a latch device, the mean implant dose is the same, but the area is larger. Similar analysis for a device with area 1.62×10^{-8} cm^2 yields mean implant dose 8.1×10^3 atoms, and σ = 90 atoms or 1.1% of the mean which works out to σ = 5 mV for V_T. Then 6σ is about 30 mV, so that the weakest latch devices have more margin than the weakest pass gate devices.

If we combine the three sources of variation, the variation on a single die in V_T is perhaps 10 mV for the macroscopic variation in implant dose and ± 60 mV for the microscopic variation. Die-to-die variation will be larger. If ± 3σ about the mean is take to be the acceptable range, wafer to wafer variation is ± 15-30 mV. If these effects are combined, the variation in mean V_T for different die is at most $[(15)^2 + (30)^2]^{1/2} = 34$ mV, which is to say ± 34 mV. But there will also be at least ± 60 mV variation in V_T on any given die, so the full range of variation is almost 100 mV. For the weakest device on the weakest die there is a very small voltage margin at 10^{-12} A.

For the technology represented in Fig. 5, the margin at 10^{-12} A is 100 mV, which is controlled by setting the threshold voltage. If the variation were more than this margin, many of the parts would be rejected because of excess leakage current - the variation from manufacturing would be a yield inhibitor, in other words. Generally, a manufacturer will set this margin as low as possible for performance, and as high as necessary for yield. The device illustrated in Fig. 7 seems to be consistent with all these considerations.

Next we consider the impact on a device characteristic (such as Fig. 7) of a trapped charge distribution such as those calculated and shown in Fig. 5 or 6. If the total charge deposited by one ion is all trapped in a pass gate device it would be 240 trapped holes in an area 0.5×10^{-8} cm^2. If the charge were trapped uniformly over the whole device, resulting in a simple shift of the curve in Fig. 7 to the left with no distortion, the shift, ΔV_T, would be 45 mV. (Two ions would double this result.) This result is almost less than half of the 100 mV margin at 10^{-12} A, shown in Fig. 4. If the trapping were less than 100%, this shift would scale proportionately: 23 mV at 50%, 9 mV at 20%, 4.5 mV at 10%. For the latch devices biased on, more charge reaches the interface but the area is greater (1.62×10^{-8} cm^2 as opposed to 0.5×10^{-8} cm^2 for the pass gate devices. In addition, the trapping would be expected to vary roughly as $E^{-1/2}$ as has been reported by several authors. For f(E) - 0.044, or 1034 holes reaching the interface, 100% trapping works out to ΔV_T - 0.060 V per ion, assuming a uniform translation of the I-V curve. As for the pass gate devices, this number will scale with assumed trapping fraction and number of ions.

A key point here is that although we calculate these threshold shifts assuming a uniform charge distribution, the actual distribution is highly nonuniform. To date we have not attempted to do device modeling on the effects of these nonuniform distributions, and apparently no one else has either. We are not even sure whether adequate models even exist because until very recently it has not occurred to anyone that it might be important to model charge distributions such as we show in Fig. 5 and 6. Modelers are only now beginning to try it.

We expect to main results to come from a comprehensive modelling effort. First, we know that nonuniform charge distributions cause distortion in I-V curves. So we expect that the shift ΔV at 10^{-12} A will be greater than ΔV_T which corresponds to a larger current value. The qualitative difference will be quantified - we will learn how much greater. Second, there are two recent papers dealing with the effects of ion strikes as a function of position. Massengill and co workers[5] report that for SOI MOSFETs, the parasitic bipolar gain depends on where in the channel the ion strikes. Even more recently, Gaillard et al[6] have begun to model non uniform charge distributions in gate oxides to explain hard errors. They report ΔV_T varying by a factor of three or more in some examples depending on the position of the ion strike. Generally shifts are smaller when the ion hits the middle of the channel, and larger when it hits near the source or drain. Probably the effect is to reduce the effective channel length, giving rise to a short channel ΔV_T. Gaillard himself points out that his work so far is done with a 2D simulator, and that a 3D simulation is necessary to draw quantitative conclusions, however.

We do not know the charge trapping efficiency of the oxide in the Micron 1M SRAM, but we have argued that a shift of about 100 mV at 10^{-12}A is the most that can be tolerated even for the average device on a die. Variation in V_T is several tens of mV on any given die, so the weakest devices on a die have much less margin than 100 mV at 10^{-12}A. Threshold voltage shifts that can be expected depend on bias, device size, assumed trapping, and position of the ion strike, but generally shifts are several tens of mV, large enough to cause the weakest devices on the die to fail. We note that relatively few struck devices actually fail (see Table I, for example). Thus we conclude that the observed hard error rate is roughly what should be expected, based on our understanding of both physics and circuit and device characteristics.

DRAM CONSIDERATIONS

Although we have only considered 4T SRAMs so far, a similar argument can be presented for DRAMs. For a 5V part, there is a critical voltage change, ΔV_{crit}, of 2.5 V. If the storage capacitance is 30 fF, as is often true for 4M, 16M, and 64M circuits,[50-70] then the critical charge is 75 fC. Typical refresh times are 16 ms for the 4M generation.[62-70] We can calculate a maximum tolerable average leakage current for the access device by dividing the critical charge on the storage capacitor by the refresh time: 75 fC/16 ms = 4.7×10^{-12} A for a 4M DRAM. That is, if the leakage current through the access device is greater than 4.7 pA, the stored charge will leak away before the bit can be refreshed. Similarly for a 16M, one would estimate 2.4 pA is the maximum tolerable leakage current, and 1.2 pA for a 64M because of longer refresh times. (Actually, the correct answer will be even less because the power supply will be reduced to 3.3 V.) The discussion we have presented for the amount of charge generated and transported to the interface and V_T variation all carries over to DRAM access devices. Therefore, heavy ions can be expected to cause total dose failures in advanced DRAMs as well, because DRAMs are also sensitive to extremely low levels of leakage current.

It is true that DRAMs are less often used than SRAMs in space systems because of their upset sensitivity. Nevertheless, a solid state recorder containing 672 4M DRAMs is apparently scheduled to fly on JPL's Cassini mission.[4] The recorder has extensive error detection and correction built in, and its main use is storing pictures, where some errors are tolerable. But there is apparently heavy ion test data suggesting stuck bits in the DRAMs also.[4]

FUTURE TRENDS

Finally, we consider what impact can be expected in future generations of memories from heavy ion total dose effects. Superficially one might expect the problem to get worse with continued scaling of device geometries. The 16M SRAMs now under development[11,12] will use 0.4 μm design rules. Thus, a spot of trapped charge such as Fig. 5 or 6 would cover the whole device or nearly so. And one might expect an experiment such as that of Dufour et al[2] to produce tens of thousands of stuck bits instead of 100. However, there are three factors at work which will probably eliminate the problem or greatly reduce it in future memories.

First, the 4T resistive load SRAM cell will not be used by the industry much longer. There are already a number of papers announcing 16M SRAMs,[11,12] and none of them use resistive load devices. In addition, the Micron 16M SRAM will also not use resistive loads.[71] Instead they build an active PMOS load device in a poly-Si film on top of the n-channel devices. This thin film transistor (TFT) has relatively poor characteristics compared to one built in single crystal Si, but its on-current is still several orders of magnitude greater than the off-current. Thus, the cell is no longer sensitive to leakage current of about 1 pA. This change in circuit design is being forced by the upset rate aused by alpha particles at sea level, but it will address the hard error problem as well. Although some 4M SRAMs will still have resistive load devices, it is likely that many that are actually sold will have the TFT technology.[13-15] Therefore, new circuit designs will probably solve the SRAM problem for a while. However, DRAM cell designs will not change, but even so, there is a trend in that technology, too, which will reduce the problem.

The second mitigating factor is thinning of the gate oxide. It is by now well known that trapping efficiency drops rapidly as oxides are thinned to 100Å and beyond.[72-75] Published gate oxide thicknesses for 64M DRAMs and 16M SRAMs are typically around 100Å,[11,12,51,53] with typical thicknesses for 16M DRAMs[56,58-60] and 4M SRAMs[15-18] around 150Å. We have performed a set of calculations similar to those in Fig. 5, except that the oxide thickness is varied systematically. Further the trapping efficiency at the interface is taken to be a function of oxide thickness, following the model presented by Benedetto et al.[75] These results are summarized in Table II. Obviously as the oxide thickness is reduced, the total trapped charge is reduced rapidly, and the size of the region affected by the charge is also reduced. Many products now in development have 100Å oxides already, and even thinner oxides will follow soon.

TABLE II

t_{ox}(Å)	INITIAL N(charges)	APPLIED FIELD (V/cm)	NOMINAL TRAPPING	NUMBER TRAPPED
200	240	2x10^5	50%	126
180	216	2.2x10^5	50%	124
150	180	2.7x10^5	15%	33
125	150	3.3x10^5	8%	12
100	120	4x10^5	5%	9
75	90	5.4x10^5	< 1%	0

Third, NEC[50] has announced that its 64M DRAM will have what is described as built in self test (BIST) and self repair (BISR). Basically, on chip software tests for failed bits, and then those locations are just not used. This approach is likely to spread rapidly.

We conclude that TFT technology will greatly reduce the heavy ion total dose problem in SRAMs in either the 4M or 16M generation, and oxide thinning and software developments will also tend to reduce the problem. DRAMs will be sensitive for longer, but eventually oxide thinning and software will probably reduce that sensitivity also. We would not make a sweeping statement that single ion hard errors will be eliminated, because more complex circuits will inherently have more statistical variation, and because short channel effects will likely become more important. But circuit design, oxide thinning, and software improvements may keep this problem from becoming bigger than it is now.

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