Total-Dose Radiation Response of Hafnium-Silicate Capacitors

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***Abstract*—Hafnium-silicate capacitors with 4.5-nm equivalent oxide thickness gate insulators were irradiated with 10-keV X-rays. The midgap and flatband voltage shifts in these devices increase linearly with dose and are significantly larger than the shifts seen in high quality, thermal SiO_2 gate oxides of similar electrical thickness. The standard trapping efficiency equation is adapted for calculating effective trapping efficiencies in alternative dielectrics and used to compare the radiation response of hafnium silicate to SiO_2 from several manufacturers. The effects of common reliability screens such as "burn-in" and bias stress tests are also discussed. It is shown that baking these devices can degrade their capacitance-voltage characteristics, and large applied voltages inject excess charge into the dielectric, which can lead to a misinterpretation of the radiation results. However, the radiation responses of these devices, coupled with the demonstrated resistance of these films to heavy-ion induced gate rupture in previous studies, suggest that alternative dielectrics to SiO_2 potentially could be integrated into future electronics technologies for many low-power space applications.**

***Index Terms*—Alternative dielectric film, burn-in effects, MOS capacitor, oxide trapped, radiation effects.**

I. Introduction

ONE OF THE most challenging problems facing the microelectronics industry today is the search for an alternative gate dielectric to SiO_2 for sub-100-nm channel length CMOS devices [1]–[6]. Large leakage currents (i.e., 1 to 10 A/cm^2) can arise in these devices via direct tunneling from the substrate to the gate electrode [1], [2]. By using a material with a larger dielectric constant for the gate insulator, it will be possible to build devices with an equivalent oxide thickness (EOT) of $\sim$10 Å that have significantly reduced leakage currents compared to similar devices built using SiO_2 [2], [4]–[8].

Several "high-k" materials are being considered to replace SiO_2. A considerable amount of uncertainty exists regarding which material can be integrated most easily into a modern CMOS process and become mainstream for future technologies. Some of the materials under consideration are Al_2O_3, HfO_2, ZrO_2, Y_2O_3, TiO_2, and Ta_2O_5 and/or the silicates of some of these materials [1], [2], [9]. Each of these materials has advantages and disadvantages, but to date, the Group IV B metal oxides have been studied most extensively. In particular, the oxides and silicates of hafnium and zirconium appear to be the most promising because they have relatively high dielectric constants and they are the most thermodynamically stable on Si [2]–[5], [9], [10]. Using a silicate instead of a pure metal oxide has the advantages of allowing a larger thermal budget during processing and improved interface quality. However, the tradeoff for using a silicate is a potentially significant decrease in dielectric constant [2]. The relative dielectric constant of pure HfO_2 is $\sim$40; whereas, the relative dielectric constant of hafnium silicate ($Hf_xSi_yO_z$) is between 15 and 25, depending on the amount of hafnium in the film [1], [4]. It has been suggested recently that high-k gate dielectrics could be developed initially as silicates, with the concentration of Hf or Zr gradually increasing as processing techniques improve with each technology node [2].

Despite the large amount of ongoing research into alternative dielectrics, very little work has been done to understand the radiation responses of these materials. In this paper, we examine the total dose radiation response of hafnium-silicate capacitors and compare this response to SiO_2 of similar electrical thickness. We also discuss the effects on these devices of commonly used reliability screens such as elevated temperature stress and bias stress. Hafnium silicate was chosen because it has shown encouraging results in measurements of reliability such as stress-induced leakage current, time-dependent dielectric breakdown, and mean time to failure [1], [2], [4], [5], [9], [10]. We find that hafnium silicate may well be a promising candidate for a future high-k dielectric material for applications where the total-dose requirements are not extreme.

II. Experimental Details

The devices used here were 1×10^{-4} cm^2 and 2.5×10^{-5} cm^2, aluminum gate, MIS capacitors with 4.5 nm EOT hafnium-silicate gate insulators and 200-nm field-isolation oxides, as shown in Fig. 1. The physical thickness of the films is $\sim$29 nm and the dielectric constant is $\sim$24. The capacitors were built at North Carolina State University on 2-in p-type Si(100) wafers, with a doping concentration of $\sim 10^{18}$ cm^{-3}. The hafnium-silicate gate dielectric was deposited using chemical vapor deposition (CVD) following a wet etch of the field isolation oxide. The deposition temperature and pressure were 200 °C and 300 mTorr. The CVD precursors were O_2, hafnium

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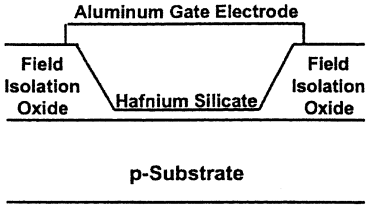


Fig. 1. Schematic diagram showing the cross section of the devices tested in this paper.

t-butoxide ($Hf[CO(CH_3)_3]_4$), and silane (SiH_4). The resulting film composition was approximately $Hf_8Si_{25}O_{67}$. Following deposition the devices were given a rapid thermal anneal (RTA) in argon for 30 s at 700 °C. The backside of the wafer was then sputtered with aluminum to allow electrical contact to the substrate. Test chips from each wafer were prepared and packaged in 40 pin ceramic dual in-line packages (DIPs) at Sandia National Laboratories.

Irradiations were performed at a dose rate of ~525 rad(SiO_2)/s using an ARACOR 10-keV X-ray source. The capacitors were irradiated incrementally to a total dose of either 500 krad(SiO_2) or 1000 krad(SiO_2). Presently, quoting doses in terms of rad (alternative dielectric) is difficult because several properties of these materials are not well known. Furthermore, it is meaningless to compare irradiation data from silicate films with different concentrations of Hf or Zr if the dose information is quoted in terms of equivalent dose in each material (e.g., 100 krad $[Hf_{25}Si_{10}O_{65}]$ is a different amount of radiation than 100 krad $[Hf_{15}Si_{20}O_{65}]$). For this reason and for ease of comparison with prior work, all dose information in this paper will be quoted in terms of equivalent dose in SiO_2.

A total of ~30 capacitors were irradiated at biases ranging from −1 V to 2 V. These capacitors did not receive any post-processing baking treatments or bias stress prior to irradiation to be certain the effects discussed below in Section V did not influence the radiation results. Additionally, all irradiation biases were evaluated on supplementary parts from the same wafer to confirm there was no charge injection due to the applied field. All irradiation data reported in this paper were obtained from devices with leakage currents of less than 10 pA, capacitance within ±10% of the theoretical value, and no hysteresis in the capacitance-voltage (CV) characteristics.

III. Results

Fig. 2 shows representative 1 MHz CV data after total dose exposure to 10, 100, 500, and 1000 krad(SiO_2) at a gate bias of 2 V. There is a monotonic increase in net oxide trap-charge density ($\Delta N_{\rm ot}$) with increasing dose. After total doses of 500 and 1000 krad(SiO_2), we observe midgap voltage shifts ($\Delta V_{\rm mg}$) of ~ −0.24 V and ~ −0.4 V, respectively. For these same total doses we also observe flatband voltage shifts (ΔV_{fb}) of ~ −0.24 V and ~ −0.4 V. Using these values for $\Delta V_{\rm mg}$, net oxide trap-charge densities can be estimated by [11]

$$\Delta N_{\rm ot} = -\frac{C_{\rm ox}\Delta V_{\rm mg}}{qA} \tag{1}$$

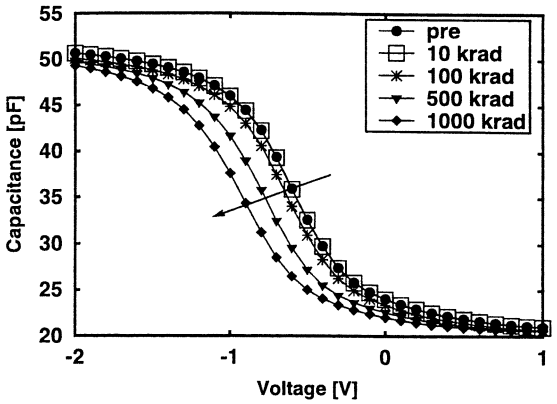


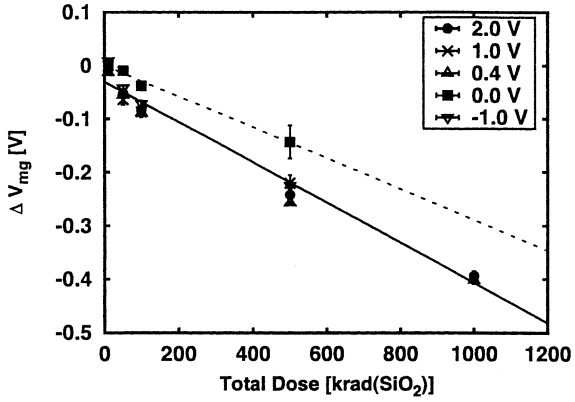
Fig. 2. Pre- and post-irradiation 1-MHz CV measurements on a 1×10^{-4} cm^2 hafnium silicate capacitor with an EOT of ~4.5 nm, irradiated to total doses of 10, 100, 500, and 1000 krad(SiO_2) at 2 V.

where $\Delta V_{\rm ot}$ is the radiation induced net oxide trap-charge density projected to the interface, $C_{\rm ox}$ is the oxide capacitance measured in accumulation, $-q$ is the electronic charge, and A is the area. Using (1) we estimate $\Delta N_{\rm ot}$ to be ~7.5×10^{11} cm^{-2} after 500 krad(SiO_2) and ~1.2×10^{12} cm^{-2} after 1000 krad(SiO_2). Similarly, the interface trap-charge densities (ΔN_{it}) can be estimated from midgap-to-flatband stretchout of 1 MHz CV curves by [12]

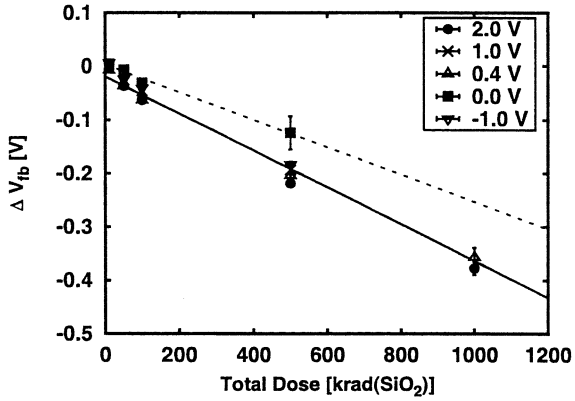
$$\Delta N_{it} = \frac{C_{\rm ox}(\Delta V_{fb} - \Delta V_{\rm mg})}{qA}. \tag{2}$$

Using the values listed above, we find that there is no measurable interface trap build-up with ionizing irradiation for these devices. This seemingly surprising result is likely due to the large pre-irradiation density of interface charge (~2×10^{12} cm^{-2}, as calculated by comparison to the theoretical CV characteristics of these devices) [13]. The effect of these charges can be seen by the relatively large stretchout of the pre-irradiation curve in Fig. 2 [14].

Fig. 3(a) and (b) show $\Delta V_{\rm mg}$ and ΔV_{fb} for all total doses and bias conditions. The data in these figures represent the average of the results from ~5 capacitors for each bias condition and the error bars represent the standard error. These data indicate the radiation induced midgap and flatband voltage shifts are nearly the same for all radiation biases shown here except 0 V. The solid line is a linear fit of the −1 V, 1-, 0.4-, and 2-V irradiation data, and the dashed line is a linear fit of the 0-V data. The lack of a significant bias dependence in these data at low electric fields has also been observed in thermal SiO_2 [15]. In this limited bias range, this may result from the competition between an increase in charge yield and a decrease in effective hole capture cross section with increasing electric field [15]. Since both positive and negative biased irradiations result in the same amount of damage, these data suggest that the radiation induced charge centroid is not strongly affected by the radiation bias. This may be consistent with a very low mobility for holes in hafnium silicate and/or a relatively high bulk trap density. The shifts seen in Fig. 3(a) and (b) are significantly larger than would be expected for high-quality radiation-hardened SiO_2 of equivalent electrical thickness under similar experimental conditions, as discussed further below.



(a)



(b)

Fig. 3. A summary of (a) midgap voltage shifts and (b) flatband voltage shifts for total dose irradiations at biases of -1 , 0, 0.4, 1, and 2 V for hafnium-silicate capacitors with 4.5-nm EOT insulators.

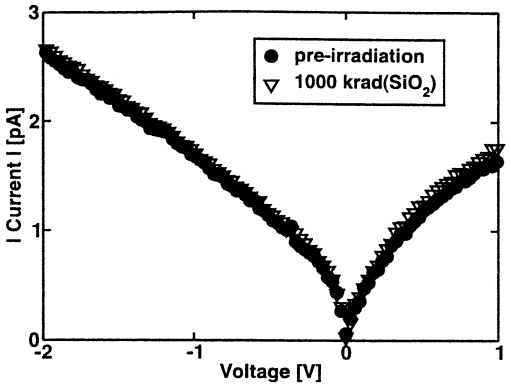


Fig. 4. Absolute value of leakage current as a function of gate voltage during current–voltage measurements of the devices of Fig. 2.

Fig. 4 is a plot of leakage current measured as a function of gate bias for the devices of Fig. 2. These data show that there is no noticeable increase in leakage current with radiation exposure up to 1000 krad(SiO_2). The currents shown in Fig. 4 are low enough that devices like these could be used in applications that require low power or standby operation. However, these currents are about a factor of ten too large to allow characterization of these devices via alternative techniques such as thermally stimulated current [11], [16], [17].

IV. Discussion

To understand the physical significance of the trapped charge densities illustrated by Figs. 2 and 3, we estimated an effective trapping efficiency for these devices. Trapping efficiency is a dimensionless quantity used to approximate the intrinsic "trappiness" of the insulator [18]. The effective trapping efficiency of an alternative dielectric is defined here as what the trapping efficiency would be if the gate dielectric were SiO_2 instead of an alternative dielectric. This definition is consistent with the concept of EOT, which describes what the thickness of the dielectric would be if it were SiO_2 instead of an alternative dielectric, based on the measured capacitance value. Neglecting possible dose enhancement effects, the effective trapping efficiency can be estimated for an alternative dielectric film using

$$f_{\rm ot} = -\frac{\Delta V_{\rm mg}\epsilon_{\rm ox}}{q\kappa_g f_y t_{\rm eq} t_{\rm phys} D} \tag{3}$$

where $f_{\rm ot}$ is the effective trapping efficiency, $\Delta V_{\rm mg}$ is the midgap voltage shift, $\epsilon_{\rm ox}$ is the dielectric constant of SiO_2 ($\sim$3.5 $\times$ 10^{-13} F/cm), $-q$ is the electronic charge, κ_g is the number of electron-hole pairs (EHP) generated per unit dose, f_y is the charge yield, $t_{\rm eq}$ is the equivalent oxide thickness ($\sim$4.5 nm), $t_{\rm phys}$ is the physical thickness of the alternative dielectric ($\sim$29 nm), and D is the total dose [18].

Currently, some of the quantities in (3) such as dielectric constant, κ_g and f_y are not well known for hafnium silicate and many other alternative dielectrics. Therefore, we have attempted to modify the values for SiO_2 to get a reasonable estimate of the effective trapping efficiency in these films. The value for $\Delta V_{\rm mg}$ in (3) was obtained from the data shown in Fig. 3(a). For charge yield (f_y) we used 0.2, which is the value for SiO_2 at the same electric field, 0.3 MV/cm, for the 2 V bias irradiation [19]. The κ_g used here is $\sim 1.2 \times 10^{13}$ cm^{-3} rad^{-1} (SiO_2). This is the known value of charge generation in SiO_2($\sim 8.1 \times 10^{12}$ cm^{-3} rad^{-1} (SiO_2)) [19] scaled by the ratio of the bandgap of SiO_2 to the bandgap of hafnium silicate ($\sim$6 eV [20]). This is a first-order approximation to account for the increase in EHPs generated per unit dose in these devices compared to SiO_2 due to the difference in band gap energies. The $t_{\rm phys}$ term in (3) accounts for charge generation throughout the entire volume of the oxide, whereas the $t_{\rm eq}$ term is to account for the moment arm effect resulting from the spatial distribution of the charges in the oxide projected to the interface [21]. In similar equations for SiO_2, both of these effects are accounted for by a single $t_{\rm ox}^2$ term [18]. However, since we are using the dielectric constant of SiO_2, it is necessary here to distinguish between the electrical thickness and the physical thickness of the material.

Using the results for a total dose of 500 krad(SiO_2), we estimate from (3) an effective trapping efficiency of $\sim$28% for these hafnium silicate devices. As a point of reference, net oxide charge-trapping efficiencies for SiO_2 reported in the literature typically range from a few percent up to $\sim$50%, depending primarily on the number of oxygen vacancies in the oxide [22], [23]. High-quality radiation-hardened oxides generally exhibit trapping efficiencies of less than $\sim$5%, and this percentage decreases as oxide quality increases [11], [18].

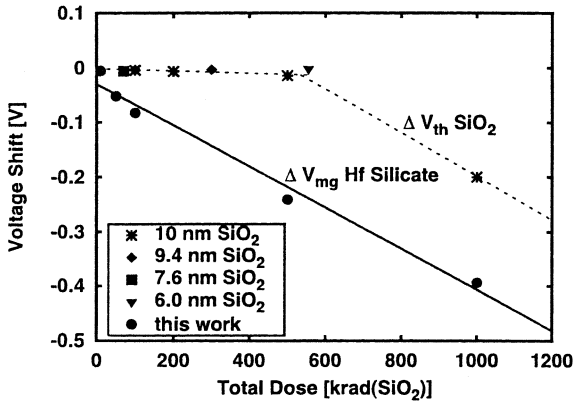


Fig. 5. Voltage shift versus dose for 2 V irradiation of the 4.5 nm EOT (29-nm physical thickness) hafnium-silicate devices from this paper compared to shifts seen in SiO_2 from several processes [24], [25], [27], [29], irradiated with ^{60}Co gamma rays under similar bias conditions.

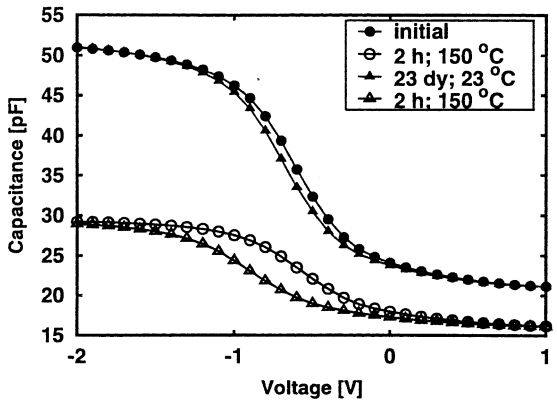


Fig. 6. Capacitance-voltage curves for 1×10^{-4} cm^2 capacitors with 4.5 nm EOT, which were baked in room ambient at 150 °C for 2 h without bias, annealed in room ambient at ∼23 °C for 23 days, then baked again at 150 °C for an additional 2 h. Changes in the CV curves of hafnium silicate were commonly observed in the devices we have tested, but large and reversible changes (like those shown here) were not always seen, presumably depending on variations in device and metal characteristics from device to device.

As mentioned above, the real need for devices with alternative dielectric gate insulators is in applications with low power requirements that cannot be met with devices using higher leakage current SiO_2 dielectrics. To date, several papers have been published that indicate the total dose damage due to trapping in the gate insulator, is not a major concern for ultra thin SiO_2 [24]–[29]. Therefore, it is useful to compare the radiation response of hafnium silicate with some previously published data on SiO_2 of similar electrical thickness.

In Fig. 5, the midgap voltage shifts for the 2-V irradiation data from Fig. 3(a) (circles) are compared to the threshold voltage shifts $(\Delta V_{\rm th})$ of: 0.35 μm SOI transistors with 10-nm radiation-hardened oxides from Honeywell (asterisks) [25], 0.5 μm transistors with 9.4 nm oxides from Hewlett-Packard (diamonds) [27], 0.35 μm transistors with 7.6-nm oxides from TSMC (squares) [24], and 6.0-nm MOS capacitors from NRL (triangles) [29], all of which were irradiated with ^{60}Co gamma rays. During irradiation, the transistors had a bias of 3.3 V on the gate with all other terminals grounded [24], [25], [27], and the capacitors had a gate bias of 2 MV/cm [12], [29]. Thus, Fig. 5 is intended to be a first order comparison of the radiation responses of these materials. Fig. 5 shows these hafnium silicate films are trapping significantly more charge than SiO_2 of similar electrical thickness. The voltage shift in the 10 nm SiO_2 films after a 500 krad(SiO_2) irradiation is ~ -15 mv, which corresponds to a trapping efficiency of 1.2%. Therefore, the trapping efficiency of these hafnium-silicate devices $(\sim 28\%)$ is larger than the trapping efficiency of the SiO_2 devices in Fig. 5 by a factor of ∼23. In contrast, the difference in voltage shifts in Fig. 5 between the hafnium silicate and 10-nm SiO_2 films is only a factor of ∼16. To understand why this is the case, consider the ratio of the parameters in (3) for hafnium silicate to the parameters for SiO_2. The values of these ratios (hafnium silicate to SiO_2) are as follows: $f_{\rm ot} \sim 23$, $\kappa_g = 3/2$, $f_y = 1/3$, $t_{\rm eq} = 1/2$, $t_{\rm phys} = 3$, and q, $\epsilon_{\rm ox}$, and D all equal one. Therefore, the factor of 16 difference in Fig. 5 is because there is half as much trapping in the hafnium silicate due to differences in charge generation and charge yield, three times more trapping in the hafnium silicate since it is physically thicker, half as much moment arm effect because it is electrically thinner, and ∼23 times more trapping because these hafnium silicate films have a higher defect density than the SiO_2. The large difference in trapping efficiencies is not surprising considering the hafnium silicate is a research quality dielectric and SiO_2 is a much more mature materials system. The fabrication methods for alternative dielectrics are still not fully developed and are likely to improve with additional research and process integration. Therefore, these results should not exclude hafnium silicate as a possible radiation-hardened dielectric material in the future. Indeed, the midgap voltage shift of ~ -0.1 V at ∼100 krad (SiO_2) for these films may already be acceptable for many potential space applications, assuming manufacturing and reliability issues are manageable. In this regard, it is especially encouraging that alternative dielectrics have been found to be quite resistant to single-event gate rupture [30]. This emphasizes the need to continue the investigation of how to improve the properties and manufacturability of these materials.

V. Baking and Bias Effects

Long-term reliability will be an important consideration for future electronic devices that use alternative dielectrics. A common type of reliability screen for microelectronic devices is an elevated temperature bias stress or "burn-in" test [31], [32]. It has been shown that these screens can alter the radiation response of SiO_2 [31], [32]. Therefore, it is necessary to see how these hafnium-silicate devices respond to a burn-in treatment.

Fig. 6 is a plot of representative CV curves that shows the effect of baking these devices, unbiased, in room ambient at 150°C for 2 h. After the baking treatment, we observe a ∼40% decrease in the accumulation capacitance and a ∼24% decrease in the depletion capacitance for these devices. In addition to a reduction in capacitance, after baking we observed hysteresis in the CV characteristics of >100 mV (not shown). After being stored in anti-static foam for ∼3 weeks in room ambient, the hysteresis recovered, and the capacitors returned, almost completely, to their initial state (solid triangles). However, as shown

by the open triangles, the effect was reproduced in these devices by subjecting them to a second baking treatment. One possible cause of this effect is that the reduction and subsequent recovery of the capacitance in these devices could be due to water vapor being baked out and re-absorbed by these films [32]. To further explore this idea, the devices were stored in a vacuum desiccator at room temperature for another ∼3 weeks following the second baking treatment. The devices were then measured again to see if the capacitance had returned to the original state in the absence of water vapor. After ∼3 weeks of storage in the desiccator the parts did not recover, suggesting that water vapor may well be responsible for the baking effect observed in these devices.

In order to see a significant change in capacitance, either the capacitor area, dielectric thickness, or dielectric constant must change. The changes seen in Fig. 6 are not likely due to a change in area or in dielectric thickness. However, the reduction in capacitance might be due to a change in the dielectric constant. To understand this, recall that the dielectric constant of a material, defined as one plus the electric susceptibility $(1 + \chi_e)$, is directly proportional to the dipole moment per unit volume [33]. Therefore, a change in the dipole moment of a material can alter the dielectric constant. Although the devices were baked at relatively low temperature (150 °C) for a short time (2 h), perhaps enough water vapor was removed from the film to cause a noticeable change in the dielectric constant of these hafnium-silicate devices. Indeed, it appears that a chemical change takes place in these devices in the absence of water vapor; however, a more detailed baking study is still necessary to determine completely the cause of the baking effect observed in Fig. 6. Similar baking effects (though often not as dramatic, and not always reversible) have also been observed on other hafnium silicate devices. However, these results may not be generally applicable to devices with hafnium silicate or another alternative dielectric as the gate insulator. Moreover, fully processed devices will be passivated to prevent moisture absorption. Still the results of Fig. 6 suggest that effects related to water vapor or hydrogen could be a significant issue for future devices with alternative gate dielectrics [32], [34].

It is also important to consider the intended device operating conditions when selecting biases for radiation testing. As mentioned above, the bandgap of hafnium silicate is ∼6 eV, which is 30% smaller than the ∼9 eV band gap of SiO_2 but comparable to the band gap of several other high-k materials [2], [20]. Some recent studies have determined the conduction and the valence band offsets between Si and hafnium silicate to be ∼1.5 eV and ∼3.4 eV, respectively, as shown in Fig. 7 [20], [35]. Therefore, the barrier to electrons tunneling into the silicate is about half of the barrier that exists in Si/SiO_2 films. Consequently, applying large biases to these devices can cause increased charge injection from the substrate into the dielectric, which may not only result in a degradation of reliability, but also a potential misinterpretation of the device radiation response. To see this, consider Fig. 8, which shows the effect of applying 3.4 V to the gate of a small area hafnium-silicate capacitor for ∼15 minutes. This is the same amount of time that it takes to do a 1000 krad(SiO_2) irradiation at the dose rate used for the devices of Fig. 3. The bias applied to the devices in Fig. 8 corresponds to

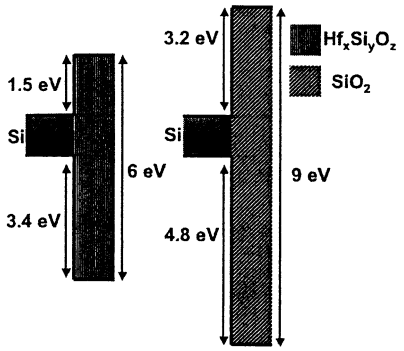


Fig. 7. Band alignments for hafnium silicate and SiO_2, after [20].

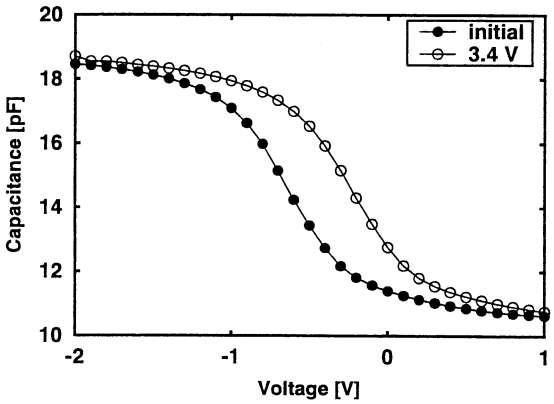


Fig. 8. Capacitance-voltage curves for 2.5×10^{-5} cm^2 capacitors with 45 Å EOT showing the changes observed due to a physical electric field of ∼1 MV/cm applied for ∼15 min.

an electric field of only ∼1 MV/cm. This is not an unreasonably large field; however, in practice these devices would most likely never be operated at a bias greater than ∼1.5 V. The midgap and flatband voltage shifts in Fig. 8 are ∼0.4 V. Comparing this value with the 1000 krad(SiO_2) irradiation data in Fig. 3(a) and (b), we find they are equal and opposite. Therefore, the radiation response could be drastically underestimated due to the bias induced charge injection. Thus, radiation testing of these devices should be done at biases relevant to device operation, which do not inject charge into the dielectric. Baking and bias effects must be considered when developing radiation and reliability test methods for devices that incorporate these types of gate dielectrics.

VI. Summary and Conclusion

We have found that the net oxide charge-trapping efficiency of these hafnium-silicate capacitors is significantly larger than high-quality radiation-hardened SiO_2 of similar electrical thickness, but may be suitable for many applications. Burn-in baking treatments were shown to degrade the device characteristics, presumably as water vapor was removed from the film. It has also been demonstrated that radiation testing at high fields may lead to an underestimation of the radiation damage due to increased charge injection from the substrate. These results show that there are some remaining obstacles that must be overcome before hafnium silicate can be considered as reliable as ultra-thin SiO_2. However, these data should not be used

to exclude hafnium silicate as a possible radiation-hardened dielectric material in the future because the fabrication methods for alternative dielectrics are still not fully developed and are likely to improve with additional research and process integration. Moreover, even the research grade dielectric films evaluated in this work likely would exhibit acceptable radiation response in applications where the total-dose requirements are not extreme. Coupled with the demonstrated resistance of these films to heavy-ion gate rupture [30], it appears that alternative dielectrics to SiO_2 may well be capable of being integrated into future electronics technologies for many low-power space applications.

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