Total-Ionizing-Dose Effects and Low-Frequency Noise in 30-nm Gate-Length Bulk and SOI FinFETs with SiO_2/HfO_2 Gate Dielectrics

By

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INTRODUCTION

In the previous almost 100 years, low-frequency noise with spectral density inversely proportional to frequency $S(f) \sim f^{\alpha}$ at frequencies f<100 kHz, where $\alpha \approx -1$, has been observed and extensively investigated in a variety of microelectronic materials and devices: from metal films, wires and resistors [1] to high-electron-mobility transistors [2], solar cells [3] and graphene devices [4], [5]. It has been found that different physical mechanisms can be responsible for the *1/f* noise in different electronic systems. In many cases, the noise is due to thermally-activated stochastic processes with a distribution of characteristic times [6]. Low-frequency noise has been used as a reliability-determining nondestructive technique for evaluating quality of dielectric-semiconductor interface in electronic devices, both in terms of performance of fabricated devices [7], [8] and characterization of new microelectronic materials and compositions [9], as well as a determination of metallization reliability [10]–[12], and variability of device parameters on the circuit level [13]. *1/f* noise has been proposed as a tool for nondestructively predicting the radiation hardness of MOS devices [14], and as a means for understanding reliability-limiting defects and impurities in the as-processed and stressed and/or irradiated devices [6], [15], [16].

The total ionizing dose (TID) response of microelectronic devices for space applications was significantly affected by technological miniaturization. While previously the response was mostly governed by charge trapping in the SiO_2 gate oxide, the introduction and the following development of high-k dielectric materials in gate stacks shifted attention to the shallow trench isolation (STI) oxides in bulk devices and buried oxides (BOX) in the SOI devices [17], as well as to the rising importance of radiation-induced short channel (RISCE) and narrow channel (RINCE) effects [18].

One of the significant developments in semiconductor miniaturization was a rise of non-planar transistors started in 1998 with work of Digh Hisamoto and Chenming Hu [19], [20], which demonstrated FinFETs fabricated with conventional MOSFET technology with the suppression of short channel effects and the reduction of parasitic resistances. Due to the advances in manufacturing technology and enhanced gate control of the transistor channel, FinFETs became commonly used in highly-scaled integrated circuits (ICs) [21]–[24]. Soon FinFETs/tri-gate FETs turned into a topic of interest in the radiation reliability community

because of their promising radiation tolerance [25]–[30]. Extensive studies show that the geometry of the devices is one of the key factors impacting radiation responses of FinFETs [31]. Triple-gate/FinFETs built on SOI with relatively long channels and greater than ~ 40 nm fin width tend to show degraded TID response with increasing fin width, as a result of increasing influence of charge trapping in the BOX [25]–[27], [29], [32], [33]. In contrast, bulk FinFETs tend to show increasing charge trapping with decreasing fin width, as a result of the electrostatic effects of nearby trapped charge in the STI [34], similar to trends observed in submicron bulk MOSFETs [18]. Although the effects of ionizing irradiation exposure on FinFETs have been evaluated extensively [18], [25], [26], [29]–[43], there has been limited work on the TID response of highly-scaled FinFETs [44], [45] and the impact of radiation on the *1/f* noise of FinFETs [46], [47].

In this thesis, we investigate the TID response of bulk and SOI FinFETs and low-frequency noise of 30 nm gate-length FinFETs with fin widths of 10 nm to 40 nm. Chapter II gives a brief overview of *1/f* noise origin in MOS devices and describes how ionizing irradiation affects *1/f* noise. Chapter III provides information about studied devices and experimental setups. Chapter IV discusses the radiation-induced degradation of DC characteristics and device parameters. Qualitatively similar trends with fin width are observed, but radiation-induced leakage is more significant for the shortest-and-narrowest channel bulk FinFETs. Results are compared to those of longer-channel FinFETs in previous studies. Despite different geometries, technological processes, and biases during irradiation, all SOI devices demonstrate enhanced radiation tolerance with decreasing fin width. Chapter V shows *1/f* noise response of bulk and SOI FinFETs before and after irradiation for room temperature as well as for a wide temperature range. Large increases are observed in post-irradiation low-frequency noise, resulting from the generation of prominent individual defects, which have greater relative effects on smaller devices than larger devices. The gate-voltage dependence of the noise indicates that the pre-irradiation defect-energy distributions of the bulk devices considered in this study generally increase towards the conduction band, while that of the SOI devices increases towards midgap. A strongly non-uniform defect-energy distribution is observed. Chapter VI provides a summary of the work.

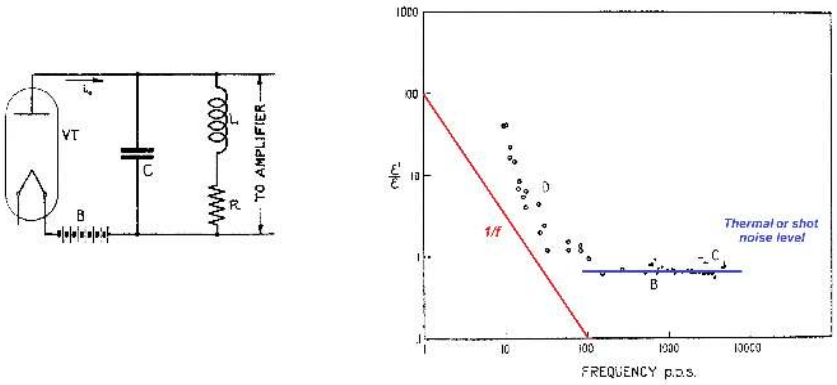
CHAPTER I

BACKGROUND

This chapter provides a brief overview of *1/f* noise origins in MOS devices, introduces the temperature dependence of *1/f* noise, and implementations of the Dutta-Horn model. We also discuss the mechanism of TID response in MOS devices, the degradation of IV characteristics, and the impact of ionizing irradiation of MOS devices on *1/f* noise. For simplicity of explanations further in this chapter, we assume a planar Si-based MOS device with SiO_2 gate dielectric.

1.1 Low-frequency noise in the MOS devices

The first observation of *1/f* noise occurred in 1925 by Johnson [48]. The voltage fluctuations across the experimental circuit consisting of a vacuum tube and a resonant RLC circuit were found to be dependent on the frequency at low frequencies. The observed results and experimental circuit are shown in Fig. I-1.



(a) (b)

Fig. I-1. (a) The experimental circuit used in the experiment. (b) An increase in voltage fluctuations following *1/f* law was found for low frequencies (B, C, D – different inductances) (after [48]).

According to [6] investigation of *1/f* noise was related to the following significant achievements: firstly, it was established in 1937 that *1/f* noise is a thermally-activated random process with a uniform distribution of energies. Secondly, McWhorter's model allowed first-

order estimates of effective trap densities in MOS transistors in 1957 [49], attributing the noise to carrier number fluctuations caused by tunnel-assisted trapping and detrapping electrons from the Si channel on near-interfacial SiO_2. Finally, the development of the Dutta-Horn model [50] allowed one to infer defect energy distributions from the temperature dependence of *1/f* noise, which was proved to apply to Si- and compound-semiconductor-based microelectronic devices. Results obtained by the application of the McWhorter model and the Dutta-Horn model to the studied devices are discussed in chapter 4.2 of this thesis.

1.1.1 Origin of *1/f* noise in MOS devices

1/f noise in semiconductor devices is a process caused by the thermally activated interaction of carriers with border traps close to the interface between a channel and the oxide with a distribution of characteristic times. Traps are distributed in physical space and energy space, so the effective density of border traps obtained through *1/f* noise measurements depends on the time scale and voltage bias conditions during the measurements [51]. The probability of an oxide defect to trap an electron decreases exponentially as the distance from the interface to the trap increases [52]–[54]. The McWhorter model suggests that with *1/f* noise measurements it is easier to access traps in SiO_2 with the energy level in the vicinity of the Fermi level, usually within a few kT [6], which means that we are able to sense defects close to the conduction band for *n*MOS transistors and to the valence band in the *p*MOS transistors. In Fig. I-2 a schematic illustration of the process leading to *1/f* noise is shown. An electron, traveling from the source to the drain through the inversion layer of Si substrate can be trapped by defects in the gate oxide located close to the semiconductor-dielectric interface (border traps). Each trap has its characteristic time τ_i with which the trap can exchange charge or "switch" (trap and release an electron) with the channel by a tunneling process, which causes time constant dispersion [52].

Electrons, trapped in the gate oxide, decrease the net potential drop between the positively biased gate terminal and grounded substrate, which decreases the effective gate voltage and subsequently decreases the drain current. Releasing the electron to the channel and leaving an empty border trap behind increases the effective gate voltage and the drain current. Since the trapping/detrapping process is stochastic, and the number of carriers in the channel is large, it can significantly affect the device performance. The diagram of the process is shown in Fig I-3.

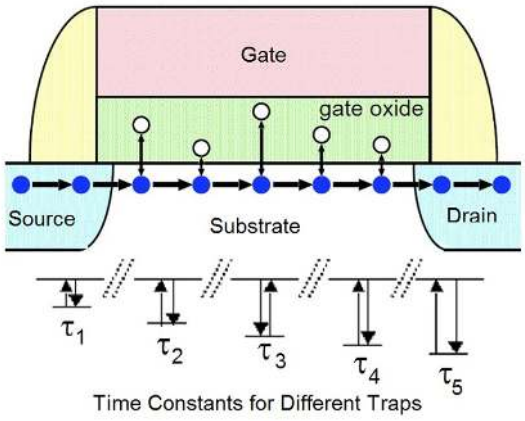


Fig. I-2. The schematic illustration of *1/f* noise origin in MOSFET due to gate oxide traps with different time constraints (after [55]).

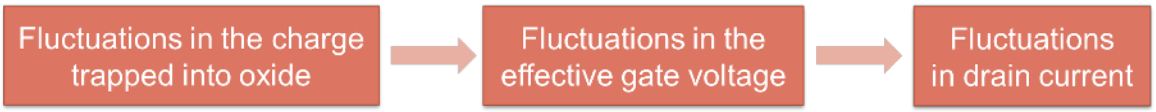
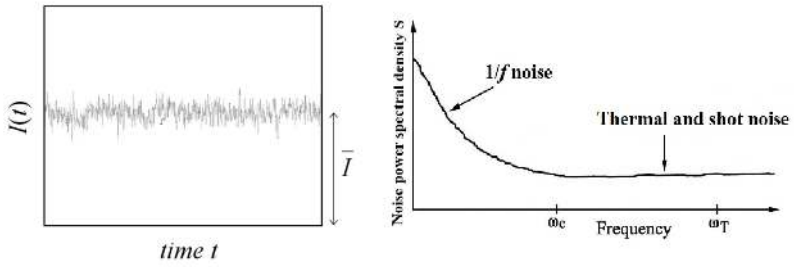


Fig. I-3. A diagram of the impact of charge trapping on device parameters.

Accounting for the random fluctuations component the drain current can be written as:

$$I(t) = \bar{I} + i_n(t) \tag{I-1}$$

where $\bar{I}$ is the average bias current and $i_n(t)$ is a randomly fluctuating current [56] which is illustrated in Fig I-4(a). When converted with Fourier transformation noise in the MOS device will look like Fig. I-4(b): at low frequencies, the noise spectrum in form of power spectral density (PSD) is proportional to $1/f^{\alpha}$ with $\alpha \approx 1$ and at high frequencies where thermal and shot noise components are dominant the noise is approximately constant.



(a) (b)

Fig. I-4. (a) A typical noise waveform in the time domain [56]; (b) the schematic illustration of noise power spectral density in the frequency domain (after [57]).

1/f noise in MOS devices is caused by fluctuations in the number of carriers, i.e. a stochastic process of capturing and emitting carriers as discussed above. The trapping/detrapping process caused by a single trap will have a power spectral density in the form of:

$$S_N(f) = 4\overline{\Delta N^2}\frac{\tau}{1+\omega^2\tau^2} \tag{I-2}$$

where $\overline{\Delta N^2}$ is the variance of number fluctuations and τ is a time constant for charge fluctuations in this trap [56]. Eq. I-2 produces a noise spectrum with a Lorentzian shape, where the noise PSD is constant for low frequencies and decreases as $1/f^2$ after reaching the cut-off frequency. *1/f* noise is formed by a plurality of the switching events and if the distribution of the time constants of traps follows the rule $D(\tau) \sim 1/\tau$ for $\tau_1<\tau<\tau_2$, so the shape of the *1/f* noise is proportional to *1/f* for $1/\tau_2<f<1/\tau_1$ [6] and results in a similar spectrum shown in Fig. I-5. Here *1/f* noise spectrum is a superposition of 11 prominent traps spectra with different characteristic times and, subsequently, cut-off frequencies.

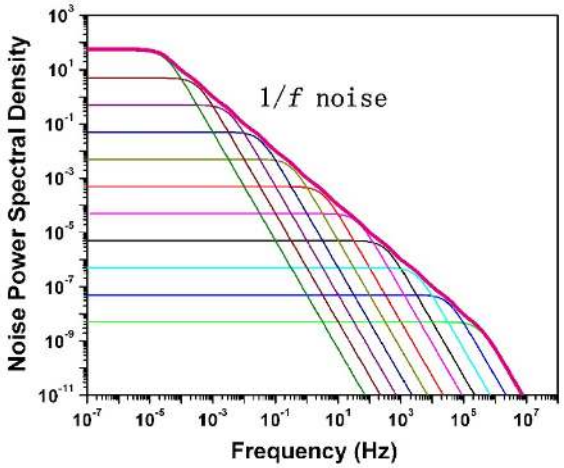


Fig. I-5. The schematic illustration of *1/f* noise power spectral density as a superposition of Lorentzian spectra of generation-recombination noise with different corner frequencies (after [57]).

1.1.2 Temperature dependence of *1/f* noise

Dutta and Horn have shown that if (1) the noise is caused by a random thermally activated process having a broad distribution of energies *D(E)* relative to *kT*, where *k* is the Boltzmann constant and *T* is the temperature, (2) the fluctuation process is characterized by an attempt frequency f_0 much higher than the measuring frequency, and (3) the coupling constants between

the random processes responsible for the noise and the total integrated noise magnitude are independent of frequency [1], [6], [50], [58], the frequency and temperature dependences of the noise are related via

$$\alpha(\omega,T) = 1 - \frac{1}{\ln(\omega\tau_0)}\left(\frac{\partial \ln S_V(T)}{\partial \ln T} - 1\right). \quad \text{(I-4)}$$

Here S_V is the excess voltage-noise power spectral density after the thermal noise is subtracted, $\tau_0 = 1/f_0$ is the characteristic attempt time of the process leading to the noise and the frequency $\omega = 2\pi f$. A value of $\tau_0 = 1.81 \times 10^{-15}$ s is chosen here to be consistent with previous MOS studies[6], [15], [58]. For noise described by Eq. I-4, the shape of the defect-energy distribution $D(E_0)$ can be described via:

$$D(E_0) \propto \frac{\omega}{kT} S_V(\omega,T), \quad \text{(I-5)}$$

where the defect energy [6], [59]:

$$E_0 \approx -kT \ln(\omega\,\tau_0). \quad \text{(I-6)}$$

If the noise is the result of thermally activated processes involving two energy levels, for example, E_0 is the barrier that the system must overcome to move from one configurational state to the other [6], [14], [50].

1.2 Total ionizing dose effects in MOS devices

1.2.1 Mechanism

TID irradiation creates electron-hole pairs in dielectrics and contributes to charge trapping, which affects the performance of the device. The classical mechanism of this process is explained in Fig. I-6. This is a band diagram of a biased device under ionizing irradiation. (1) The electron-hole pairs created during irradiation transport in different directions under applied electric field: unrecombined electrons - towards the positively charged gate, unrecombined holes - to the oxide-semiconductor interface. Since the mobility of holes is significantly lower than the mobility of electrons, (2) they slowly travel towards the Si-SiO_2 interface through localized states in SiO_2 along with protons. When they reach the interface, (3) the pre-existing oxygen vacancies capture holes and form oxide and border traps, and (4) free protons contribute to interface-trap buildup [17], [60]–[64]. Nowadays for highly-scaled devices, radiation-induced

charge trapping in the STI for bulk devices and in BOX for SOI devices became a primary radiation-tolerance concern since gate stack oxides have been replaced by thin layers of high-k materials [17].

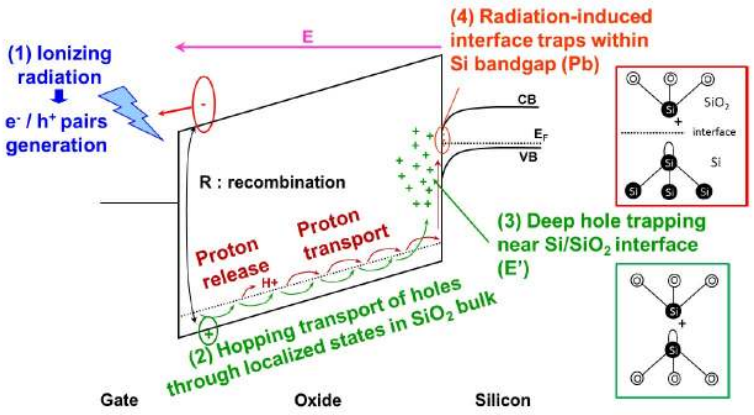


Fig. I-6. Process of radiation-induced interface and oxide traps formation described in the band diagram of a biased metal-oxide-semiconductor structure [62].

1.2.2 Influence of irradiation on DC characteristics

As discussed in Section 1.2.1 TID irradiation contributes to the formation of interface traps and oxide traps in a microelectronic device. Oxide traps are positively charged in SiO_2, while interface traps can change their electrical states due to surface potential. Border traps are located in the oxide close to the interface, but these traps are able to exchange charges with the channel in the time frame of the measurements [16], [51], [65]. Fig. I-7 illustrates the physical locations of all three types of traps and the analogy with “border states” in the US Civil War.

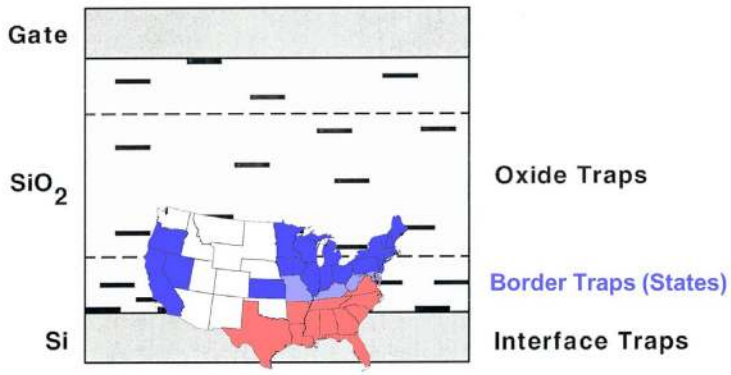


Fig. I-7. Schematic illustration of existing traps in the MOS device [16].

Fig I-8 indicates the contribution of radiation-induced oxide and interface traps buildup to the DC characteristics of *n*MOS and *p*MOS devices. Oxide traps are charged positively in SiO_2 both in *p*MOS and *n*MOS, i.e., they decrease the threshold voltage and shift IV curves negatively, which is shown with dashed green lines in Fig. I-8. *p*MOS transistors at threshold are mostly affected by positively charged interface traps located in the lower part of the Si bandgap (empty donor-like traps). Consequently, the effects of positive interface traps and positive oxide traps add up for *p*MOS device, increasing the absolute value of the negative threshold voltage, and shift the IV curve negatively during TID exposure (i.e., the increase of the radiation-induced threshold voltage shift) [62], [63]. On the other hand, *n*MOS devices at threshold are mostly affected by negatively charged traps located in the upper part of the Si bandgap (filled acceptor-like traps), so for *n*MOS devices, the effect of negatively charged interface traps compensates the negative radiation-induced threshold voltage shift due to always positive oxide traps.

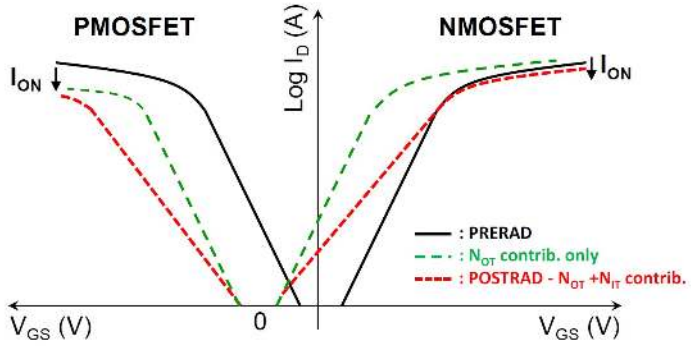


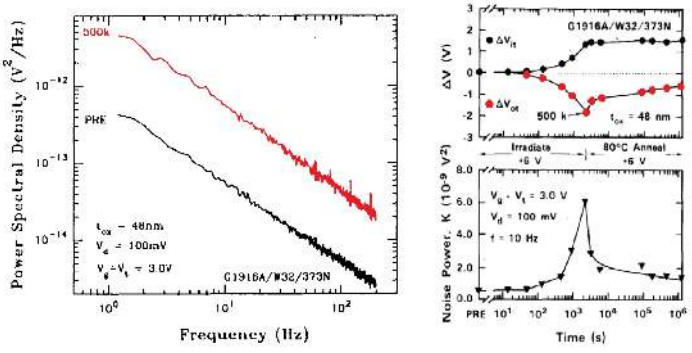
Fig. I-8. Radiation-induced oxide trapped charge (green dash) and interface traps (red short dash) contributions on I-V curves in *p*MOSFET and *n*MOSFETs [62].

1.2.3 Influence of irradiation on *1/f* noise

Due to the increase of border traps during TID irradiation low-frequency noise of irradiated devices is higher than the low-frequency noise of as-processed devices [6], [58], [66]–[69]. Fig. I-9(a) shows typical results for a micron-sized MOSFET before and after irradiation with a significant uniform increase in the post-irradiation noise spectrum over the whole range of measured frequencies.

It has been found that the pre-irradiation *1/f* noise level in MOS devices strongly correlates with post-irradiation threshold voltage shift due to border traps buildup [54], [70]. Further evidence of correlation between *1/f* noise and threshold voltage shift due to oxide traps was observed in [71], demonstrating that *1/f* noise in studied transistors was increasing with increasing of the amount of the oxide traps during irradiation and decreasing during annealing with decreasing of the oxide traps, while the amount of interface traps was almost constant during annealing [66], which is shown in Fig I-9(b).

The combination of density functional calculations and low-frequency noise measurements as a function of temperature and irradiation is a powerful tool for determining reliability-limiting defects in microelectronic materials and devices and processes occurring during irradiation [6]. One of the examples [1], [15], [67], [72], [73] is shown in Fig. I-10, where defects in graphene transistors activated during irradiation were passivated during high-temperature annealing and were attributed to the influence of hydrogen- and oxygen-related defects.



(a) (b)

Fig. I-9. (a) Pre- and post-irradiation *1/f* noise spectra for MOSFET L_{CH} = 7.5 μm, W_{CH} = 50 μm (after [71]); (b) Top: threshold voltage shift due to interface-trap charge ΔV_{it} and oxide trap charge ΔV_{ot} as a function of irradiation and annealing. Bottom: normalized noise power through the same irradiation and annealing processes (after [66]).

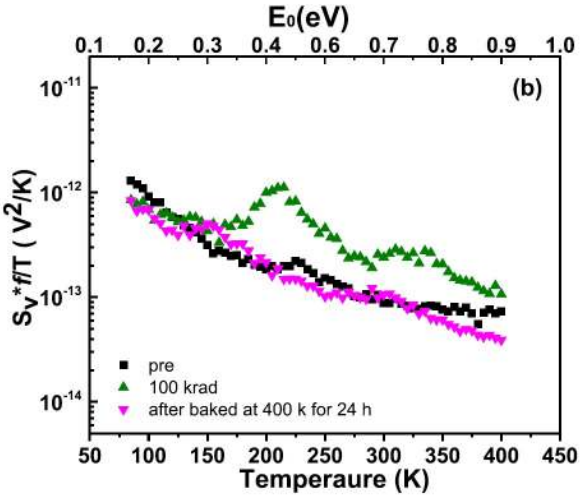


Fig. I-10. *1/f* noise vs temperature before and after irradiation and after high-temperature annealing of graphene transistors from [5].

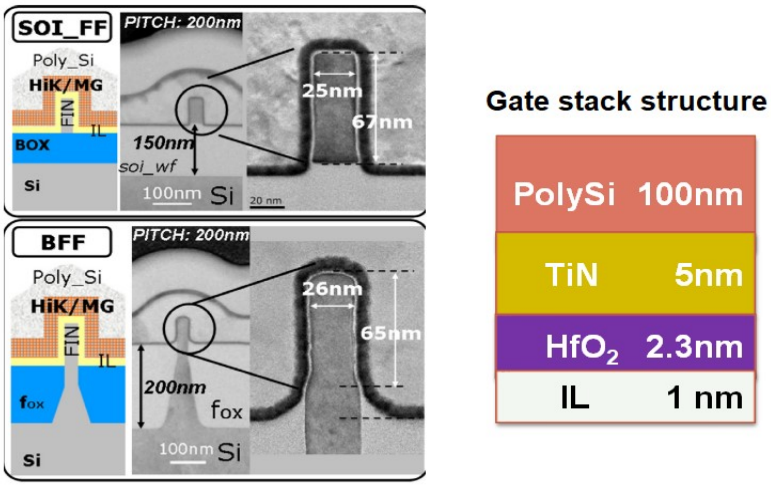
CHAPTER II

EXPERIMENTAL DETAILS

This chapter provides information about the studied devices and experimental setups. All the experiments discussed in this thesis were performed at Vanderbilt University with the equipment of the Radiation Effects and Reliability group.

2.1 Studied devices

SOI and bulk FinFETs were fabricated by imec [74] using otherwise similar processes [34], [39], [75]. Fig. II-1(a) provides a schematic cross-section of the devices. The gate stack consists of high-k gate dielectrics of 2.6 nm HfO_2 on a 1-nm SiO_2 thermal interfacial layer (EOT (effective oxide thickness) of 1.5 nm). The 5-nm TiN metal electrode is fabricated with Physical Vapor Deposition (PVD) with 100 nm of polycrystalline silicon on top. The gate stack structure is schematically shown in Fig. II-1(b). The source/drain access regions were formed by selective epitaxial growth of Si on the source and drain areas, followed by NiPt silicidation.



(a) (b)

Fig. II-1. (a) SOI FinFET and bulk FinFET gate stack diagrams (on the left) and x-TEM images with critical dimensions (on the right). After [75]. (b) Schematic representation of gate stack materials (not to scale).

TID response and *1/f* noise were studied on devices that had 5 fins, channel lengths of 30-250 nm, and fin widths of 10-40 nm, as summarized in Table 1. The fin height is ~ 65 nm. During the experiments, the devices were bonded into handcrafted high-speed packages shown in Fig. II-2.

TABLE I

GEOMETRIC PARAMETERS OF FINFETS

Type	Varied Parameters	Values of Varied Parameters, nm	Fixed Parameters	Aspect Ratio W_{FIN}/H_{FIN}
SOI, bulk	Fin Width (W_{FIN})	10, 20, 40	L_G = 30 nm, N_{FIN} = 5	6.5, 3.3, 1.6
SOI	Gate Length (L_G)	30, 45, 70, 110, 250	W_{FIN} = 20 nm, N_{FIN} = 5	3.3

Fig. II-2. High-speed package with eight SMA-connectors and the bonded device. Microstrips connect wires from the device to SMA-connectors. Non-conductive glue is used for attaching connectors and microstrips to the package.

2.2 Experimental setup

2.2.1 Irradiation

Devices were irradiated at ~ 295 K with 10-keV X-rays at a dose rate of 30.3 krad(SiO_2)/min up to 2 Mrad(SiO_2) (unless stated otherwise) with ARACOR Model 4100 Semiconductor Irradiation Test Source. IV characteristics were obtained at V_d = 0.05 V with an

Agilent 4156A/4156B semiconductor parameter analyzer. The schematic TID setup diagram is shown in Fig. II-3. The TID-induced degradation was evaluated for devices with geometry $L_G = 30$ nm, $W_{FIN} = 10$ nm, and $N_{FIN} = 5$ for on-state (V_g = 1 V and $V_d = V_s$ = 0 V), off-state ($V_d = 1$ V and $V_g = V_s = 0$ V), and grounded condition ($V_g = V_d = V_s$ = 0 V) with similar parametric shifts and trends for all device geometries.

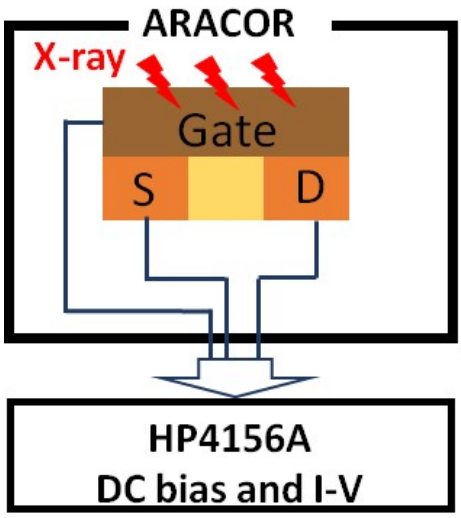


Fig. II-3. Schematic TID setup diagram (after [76]).

2.2.2 Low-frequency noise

The noise power spectral density S_{Vd}, with correction for background noise, was measured at ~ 295 K over a frequency f range from 1 Hz to 390 Hz unless otherwise stated. During noise measurements, the drain voltage V_d was held at 0.05 V with a source and substrate grounded. The gate-to-threshold voltage V_{gt} was varied from 0.2 V to 0.6 V. Temperature dependence of low-frequency noise was measured in the temperature range from 80K to 320K. For the low-frequency noise testing in a wide temperature range, a mounted device was placed into Janis VPF-100 Cryostat in a low-pressure environment. The schematic diagram of the low-frequency noise setup is shown in Fig. II-4. Random telegraph noise (RTN) measurements were performed at room temperature with Keithley 4200-SCS Parameter Analyzer at the same bias conditions as *1/f* noise measurements.

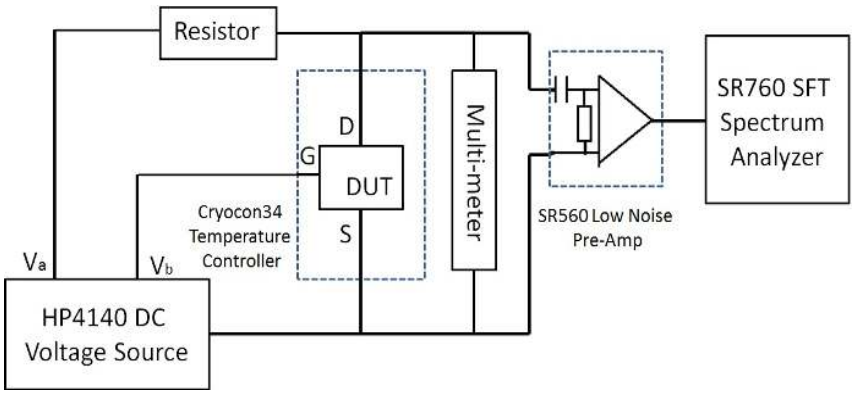


Fig. II-4. Schematic diagram of the low-frequency noise setup (after [77]).

CHAPTER III

IMPACT OF IONIZING IRRADIATION ON DC CHARACTERISTICS

This chapter discusses the radiation-induced degradation of DC characteristics and device parameters such as threshold voltage shift ΔV_{th}, normalized transconductance g_{m_max}, and maximum drain current I_{on}.

3.1 Bulk FinFETs

Fig. III-1 shows that a bulk FinFET irradiated under on-state bias condition (V_g = +1 V) exhibits a negative V_{th} shift over the full range of examined doses and a significant increase in off-state leakage. The increased leakage is due to charge trapping in the shallow trench isolation (STI), which is illustrated in Fig. III-6 for narrow and wide bulk FinFETs. Trapped charge creates an electrical field, which affects charge separation in the subchannel area, and inverts the region near the edges of STI and forms a parasitic leakage path from the source to the drain [34]. This leakage path in the subchannel region results in a dominant part of the radiation response of bulk FinFETs.

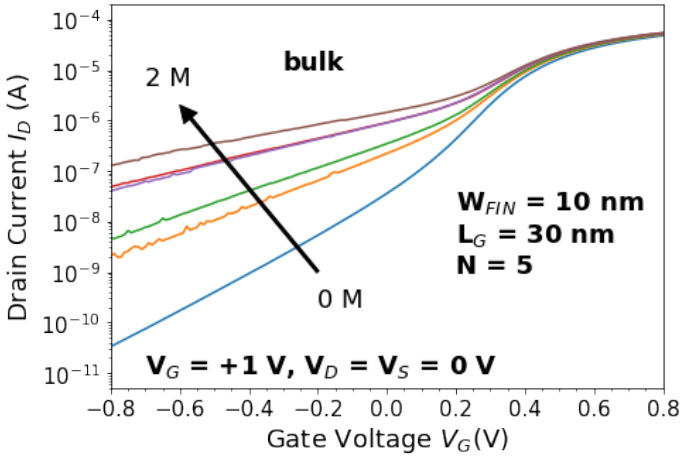


Fig. III-1. I_d-V_g curves as a function of dose for bulk devices with gate length of 30 nm and fin width of 10 nm; V_d = 0.05 V. The bias condition during irradiation was on-state (V_g = +1 V).

Because a significant part of threshold voltage shifts ΔV_{th} during irradiation in bulk devices was determined by the influence of a leakage current increase, we used a linear extrapolation method for finding threshold voltage V_{th} with correction for leakage illustrated in Fig. III-2 [78]. In the linear extrapolation method, the x-intercept of the linear extrapolation of the I_d-V_g curve at the point of maximum transconductance g_m with the V_g axis is defined as $V_{th} + V_d/2$ [79].

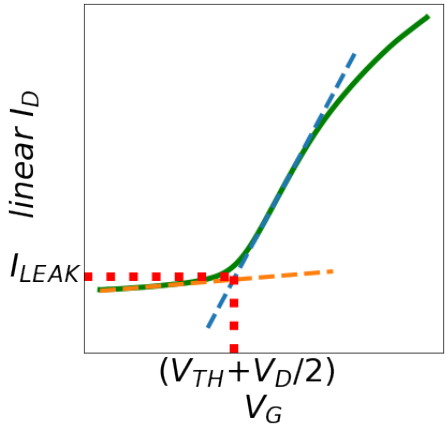


Fig. III-2. Illustration of the leakage correction method [78].

Fig. III-3 shows effective V_{th} shifts of bulk FinFETs with fin widths of 10 nm, 20 nm, and 40 nm, as functions of irradiation and annealing time for devices irradiated under on-state bias condition (V_g = +1 V). Narrower fin devices exhibit larger V_{th} shifts [34]. A maximum effective V_{th} shift of ~30 mV is observed for the 10 nm fin-width devices. Wider-fin bulk devices exhibit comparable degradation, with V_{th} shifts less than ~15 mV.

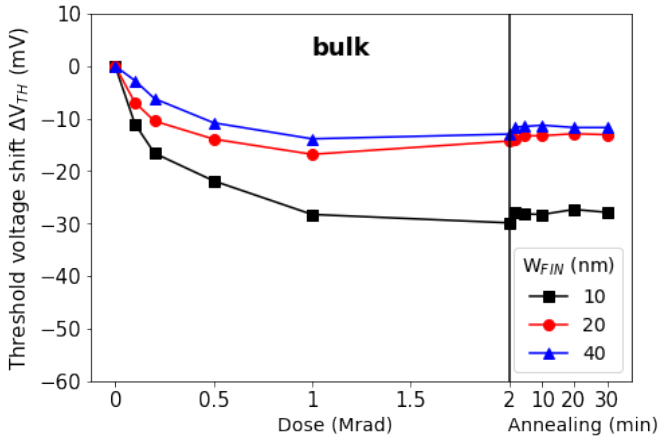


Fig. III-3. Threshold voltage shifts ΔV_{th} as a function of irradiation and annealing time for bulk FinFETs with fin widths of 10 nm to 40 nm.

Fig. III-4 demonstrates the normalized peak transconductance g_{m_max} with fin widths of 10 nm, 20 nm, and 40 nm, as functions of irradiation and annealing time for bulk devices irradiated under on-state bias condition (V_g = +1 V). The normalized peak transconductance g_{m_max} shows an increase of less than 3% during irradiation for bulk FinFETs. This small change most probably is related to the g_{m_max} determination error and cannot be considered as a meaningful result.

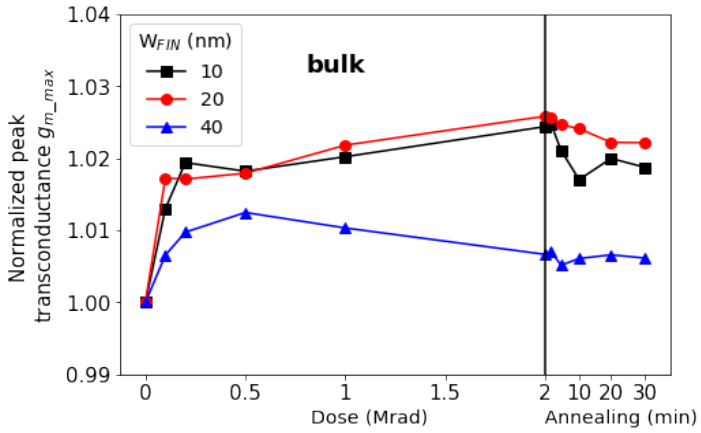


Fig. III-4. Normalized peak transconductance g_{m_max} as a function of irradiation and annealing time for bulk FinFETs with fin widths of 10 nm to 40 nm.

Fig. III-5 shows an increase in maximum drain current I_{ON} (V_g = +0.8 V) for bulk devices with fin widths of 10 nm, 20 nm, and 40 nm, as functions of irradiation and annealing time for

devices irradiated under on-state bias condition (V_g = +1 V). The narrowest devices demonstrate the largest increase in on-current of ~12% versus ~6% for wider devices, which emphasizes the relatively more significant influence of radiation-induced trapped charge in the STI region in modulating threshold voltage for narrow-fin devices.

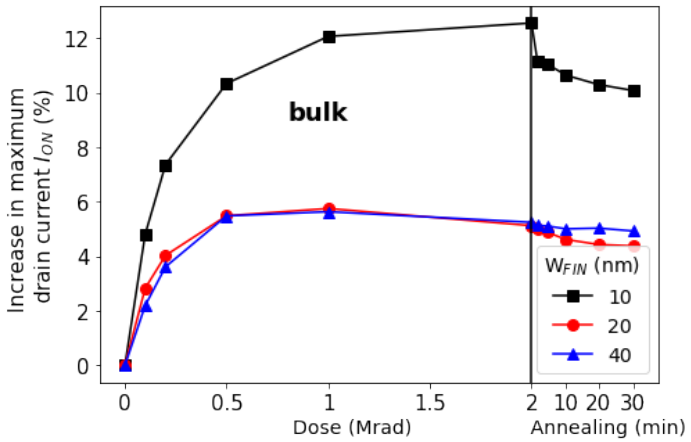


Fig. III-5. Increase in maximum drain current I_{on} (V_g = +0.8 V) as a function of irradiation and annealing time for bulk FinFETs with fin widths of 10 nm to 40 nm.

The relative difference in the influence of radiation-induced trapped charge and interface traps in narrow (on the left) and wide (on the right) bulk FinFETs is illustrated in Fig. III-6. For the wide-fin transistor, the electrostatic coupling between the front gate and trapped charge is more relaxed due to a relatively large length of the front gate. Here, the narrow-fin device has higher electric fields between the front gate and trapped charge over a strait subchannel region in the STI, which turns on a parasitic lateral transistor and enables a conduction leakage path under the channel [34]. Therefore, the impact of a trapped charge inside the STI region near the channel is greater for the same accumulated dose in the narrow-fin device than in the wider-fin device.

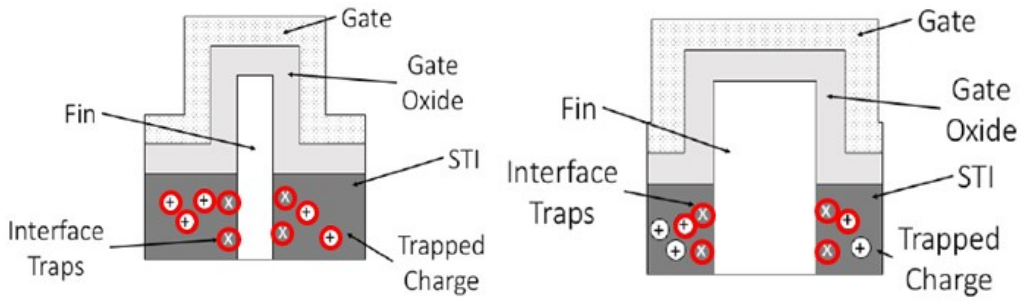


Fig. III-6. Diagram illustrating relative positions of interface traps and oxide trapped charge in the BOX of a narrower fin bulk FinFET (left) and wider fin bulk FinFET (right). Not to scale. (after [80]).

3.2 SOI FinFETs

Fig. III-7 shows I_d-V_g characteristics of SOI devices with gate length of 30 nm and fin width of 10 nm irradiated under on-state bias condition (V_g = +1 V). Devices generally show a negative V_{th} shift from pre-irradiation to 500 krad(SiO_2), and a positive V_{th} shift with increasing TID from 500 krad(SiO_2) to 2 Mrad(SiO_2). The decrease in V_{th} for doses below 500 krad(SiO_2) is due to radiation-induced trapped positive charges in the buried oxide (BOX) [25], [26], [81], as shown schematically in Fig. 2(a). Above 500 krad, the I_d-V_g curves shift positively because of (1) the combined effects of negatively charged interface traps at the gate oxide/Si and Si/BOX interfaces [25], [26], [81], and (2) net negative charge trapping in the HfO_2 due to radiation-induced electrons generated in SiO_2 and transported into HfO_2 under positive gate bias [41]. Since the leakage path in the sub-fin region is eliminated in SOI devices, the main reason of radiation-caused degradation in SOI FinFETs is charge trapped in the BOX region under the channel, which is responsible for a moderate increase in leakage current in SOI devices. The positive charge trapped in BOX forms an inversion layer at the bottom of the silicon fin, which creates a leakage path. Due to the location of this path inside the silicon fin, it has a stronger gate control, which doesn't allow the leakage to increase as it was seen in bulk transistors in Fig. III-1, and even reduces the leakage when the impact of net negative charge trapping prevailed over the impact of positive charge trapped in the BOX.

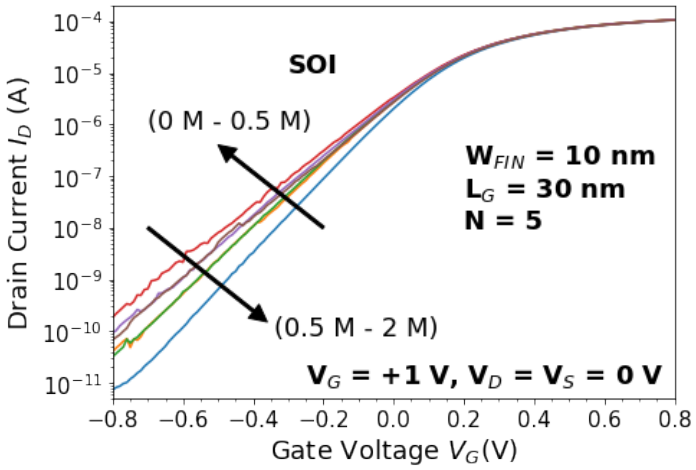


Fig. III-7. I_d-V_g curves as a function of dose for SOI FinFETs with gate length of 30 nm and fin width of 10 nm; V_d = 0.05 V. The bias condition during irradiation was on-state (V_g = +1 V).

Fig. III-8 shows threshold voltage shifts ΔV_{th} for SOI FinFETs with fin widths of 10 nm to 40 nm, for devices irradiated and annealed under on-state bias condition (V_g = +1 V). The threshold voltage first shifts negatively, reaching a maximum degradation point, and then shifts positively. A maximum shift of ~35 mV at 500 krad(SiO_2) is observed for the 40 nm fin-width devices, emphasizing their radiation tolerance. V_{th} shifts decrease with decreasing fin width, consistent with trends in larger SOI devices [25], [26], [32].

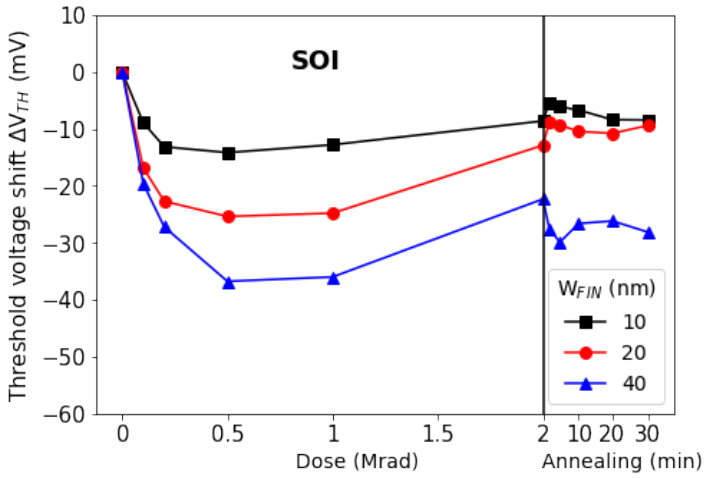


Fig. III-8. Threshold voltage shifts ΔV_{th} as a function of irradiation and annealing time for SOI FinFETs with fin widths of 10 nm to 40 nm.

Fig. III-9 demonstrates the normalized peak transconductance g_{m_max} with fin widths of 10 nm, 20 nm, and 40 nm, as functions of irradiation and annealing time for SOI devices irradiated under on-state bias condition (V_g = +1 V). The normalized peak transconductance g_{m_max} decreases for 2-4% during irradiation for SOI FinFETs, which can be explained as increased carrier scattering by the radiation-induced interface and border traps. No fin width dependence for radiation-induced g_{m_max} change is observed in SOI devices.

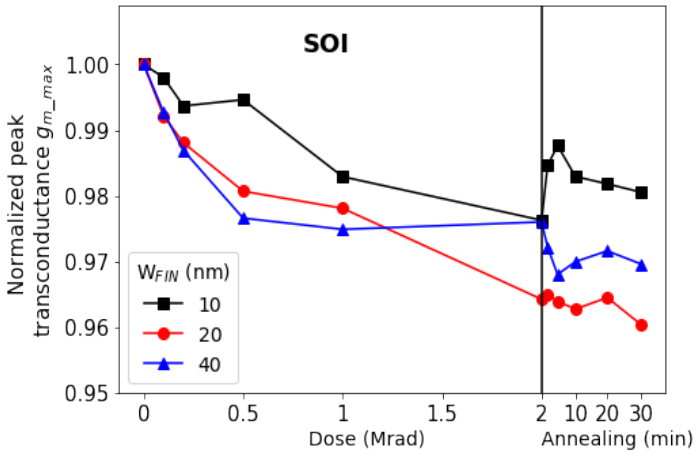


Fig. III-9. Normalized peak transconductance g_{m_max} as a function of irradiation and annealing time for SOI FinFETs with fin widths of 10 nm to 40 nm.

Fig. III-5 shows an increase in maximum drain current I_{ON} (V_g = +0.8 V) for SOI devices with fin widths of 10 nm, 20 nm, and 40 nm, as functions of irradiation and annealing time for devices irradiated under on-state bias condition (V_g = +1 V). Devices show a similar trend with a small ON-current increase (less than 2%) up to 0.5 Mrad(SiO_2) with a following gradual decrease (less than 2%), and ON-current stays stable during annealing.

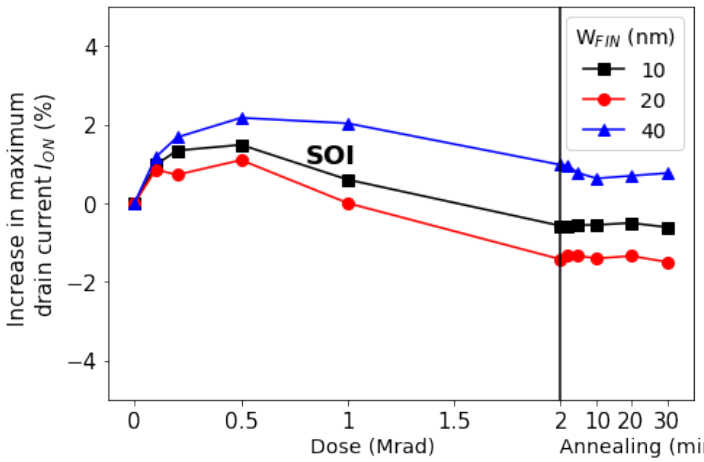


Fig. III-10. Increase in maximum drain current I_{on} (V_g = +0.8 V) as a function of irradiation and annealing time for SOI FinFETs with fin widths of 10 nm to 40 nm.

To explain the fin width dependence of threshold voltage shifts ΔV_{th} for SOI FinFETs we need to discuss the influence of the lateral gates in this type of devices. Two vertical sides of a gate stack, folded around a silicon fin, form a strong horizontal electrical field, reducing the vertical electrostatic coupling between the top horizontal part of the front gate oxide and trapped charge in the BOX [31], which is schematically shown in Fig. III-11. Narrower fins in SOI devices with the reduced area under the channel improve the efficiency of lateral screening, resulting in a remarkable radiation tolerance of narrow SOI FinFETs [26], [29], [32], [82], which is true for a wide range of gate lengths [31]. The summary of this effect from different studies is provided in Fig. III-14.

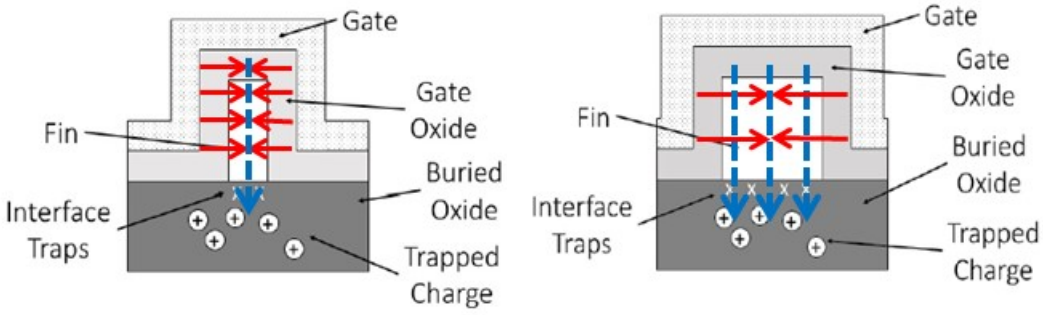


Fig. III-11. Diagram illustrating electrostatic coupling between the front gate and radiation-induced interface traps and oxide trapped charge in the BOX of a narrower fin SOI FinFET (left) and wider fin SOI FinFET (right). Not to scale. (after [80]).

Fig. III-12 shows the gate length dependence of the radiation response for SOI FinFETs with W_{FIN} = 20 nm and N_{FIN} = 5. Devices were irradiated under positive gate bias V_g = +1 V. The greatest degradation is observed for the shortest channel devices [83]. The least radiation-induced degradation is observed for L_G = 110 nm at lower doses and L_G = 70 nm to 110 nm for higher doses. The similarly complicated gate length dependence was observed for NW SOI devices in [27], where it was simulated and attributed to the complicated distribution of charges in the subchannel region.

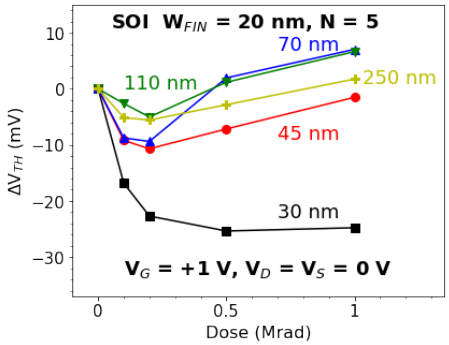


Fig. III-12. Threshold voltage shifts ΔV_{th} as a function of dose for SOI FinFETs with gate lengths L_g = [30, 45, 70, 110, 250] nm as a function of accumulated dose.

3.3 Discussion and Conclusions

In this chapter radiation-induced degradation of DC characteristics of bulk and SOI transistors was discussed. Several DC parameters such as threshold voltage shift ΔV_{th}, normalized transconductance g_{m_max}, and maximum drain current I_{on}. were considered. In this part, we'll show a comparison of the results obtained in this work and literature results.

Radiation response for bulk devices is governed by the parasitic leakage path in the subchannel region created by the radiation-induced trapped charge in the STI. Effective threshold voltage shifts, corrected for the increased leakage demonstrate that the narrowest devices degrade the most due to the localization of the trapped charge close to the middle of the channel and the stronger influence of the trapped charge on the electrostatic coupling of the lateral gate in the bulk transistor.

Compared to the results obtained for 70-nm channel-length bulk devices in [34], absolute values of off-state drain leakages for pristine devices are up to 1.5 orders of magnitude higher for

30-nm channel-length devices studied in this work due to short-channel effects. However, the normalized radiation-induced off-state leakage increase $I_{off}(D = 0.5\,Mrad)/I_{off}(D = 0\,Mrad)$, which is shown in Fig. III-13, is similar for both gate lengths, except for the narrowest devices due to both RINCE and radiation-induced short channel effects (RISCE) [83]. In the narrowest and shortest channel transistors, the radiation-induced charge trapped in the STI affects the potential distribution in the subchannel region more strongly, lowering the barrier between the source and drain, thereby allowing carriers to transport between the terminals, increasing the subthreshold leakage due to band-to-band tunneling [82].

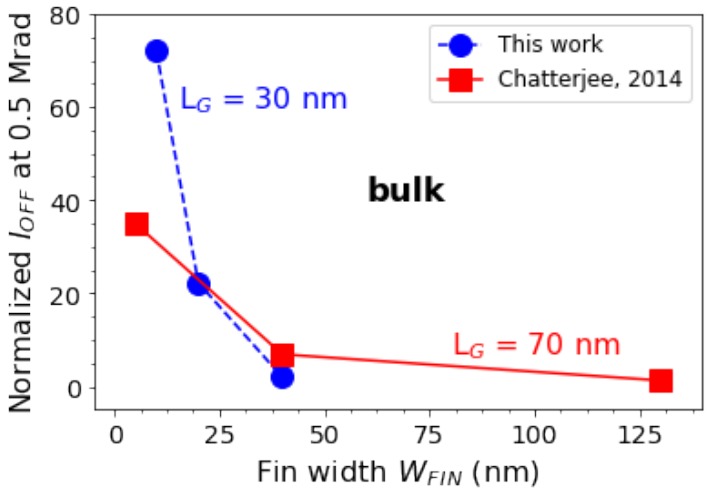


Fig. III-13. TID-induced normalized off-state drain leakage increase for bulk FinFETs irradiated up to 0.5 Mrad as a function of fin width. Devices are fabricated using the same technological process. Results for L_g = 70 nm are from [34]. The only significant differences are for the shortest, narrowest devices, for which both RINCE and RISCE are observed due to the electrostatic effects of trapped charge in the STI on V_{th} shifts and subthreshold stretchout and leakage.

SOI devices proved their exceptional radiation tolerance down to 30-nm gate length, showing a turnaround effect in threshold voltage shifts ΔV_{th} and maximum drain current I_{ON} due to a combination of trapped charge in the BOX predominant at low doses up to 0.5 Mrad(SiO_2), and negatively charged interface traps and net negative trapped charge in the HfO_2 gate oxide, predominant at higher doses.

Fig. III-14 summarizes results obtained for different SOI FinFET designs as a function of fin width. Despite different geometries, technological processes, and biases during irradiation, all

devices demonstrate enhanced radiation tolerance with decreasing fin width. The higher tolerance of narrower FinFETs results in all cases from the increased lateral gate control in narrow-channel devices, which in turn provides efficient electrostatic control over the potential in the silicon body. Therefore, the coupling effects of the front and the back gates are weakened and the effects of the trapped charges in the BOX are reduced [26], [32].

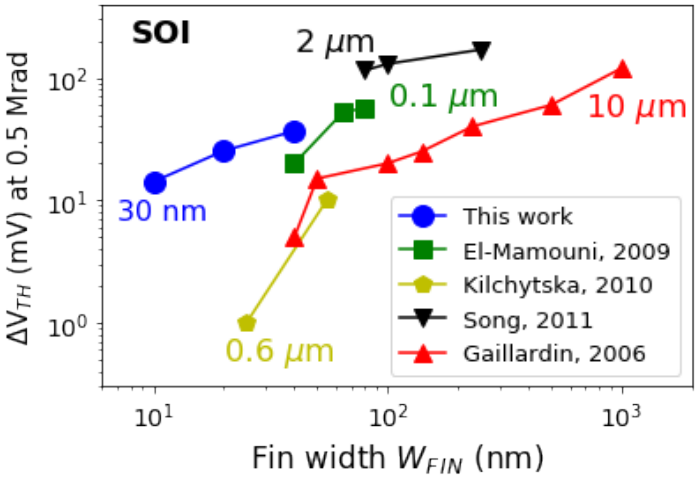


Fig. III-14. TID-induced V_{th} shifts vs. fin width at similar accumulated doses D in this work and previous studies for SOI FinFETs. Gate lengths are noted in the plot. For [17], $D = 1$ Mrad(SiO_2); for the other cases, $D = 0.5$ Mrad(SiO_2). Results from [29], [32], [37] are for off-state-bias irradiation; results from [26]and this work are for on-state-bias irradiation. Lines are aids to the eye.

CHAPTER IV

IMPACT OF IONIZING IRRADIATION ON *1/F* NOISE

This chapter discusses the *1/f* noise response of bulk and SOI FinFETs before and after ionizing irradiation for room temperature as well as for a wide temperature range. Frequency dependence, gate-voltage dependence, *1/f* noise dependence on fin number, random telegraph noise (RTN), as well as Dutta-Horn model application are reported.

4.1 Room-temperature *1/f* noise

Fig. IV-1 shows S_{Vd} versus f for V_g-V_{th} = 0.4 V for SOI and bulk FinFETs with gate length of 30 nm and fin width of 10 nm before and after irradiation. The bias condition during irradiation was on-state (V_g = +1 V). The frequency dependence of the noise changes significantly with irradiation for each device [71], [84], [85]. For the SOI device, increasing noise magnitudes are observed predominantly in the higher range of frequencies after irradiation. The bulk device shows increasing noise magnitudes predominantly in the lower range of frequencies after irradiation, with a decrease at higher frequencies. These changes are caused by the impact of a relatively small number of additional radiation-induced oxide and border traps, compared with pre-irradiation, consistent with the small shifts in V_{th}, as we discuss below. These defects are located in the gate stacks and in the STI for bulk devices and in the BOX for the SOI FinFETs [6], [9], [15], [53], [59], [66], [86]–[88].

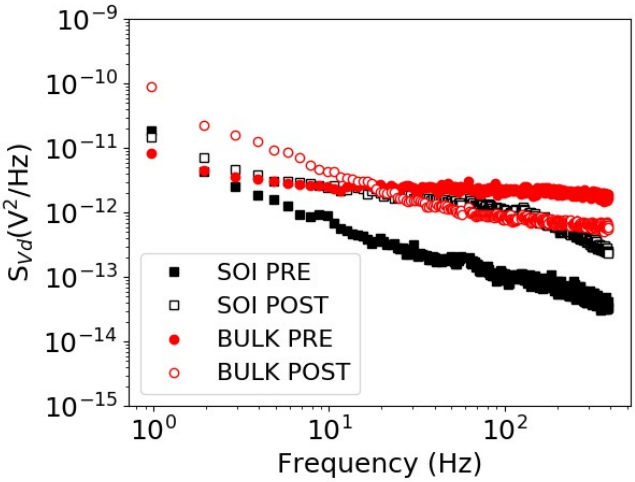


Fig. IV-1. Frequency dependence of S_{Vd} for SOI (square symbols) and bulk FinFETs (circle symbols) before (solid symbols) and after (open symbols) irradiation. The bias condition during irradiation for both devices is on-state. Biases were V_g–V_{th} = 0.4 V and V_d = 0.05 V during noise measurements.

Fig. IV-2 shows post-irradiation *1/f* noise for the extended frequency range f = 1 Hz to 12.5 kHz for a bulk device with fin width of 40 nm that is otherwise similar to the devices of Fig. IV-1. Here V_g-V_{th} = 0.4 V and V_d = 0.05 V. The device was irradiated up to 2 Mrad(SiO_2) with V_g = +1 V. Pre- and post-irradiation *1/f* noise spectra in the frequency range f = 1 Hz to 390 Hz are shown in the inset. Both curves fluctuate from a "pure" *1/f* law, demonstrating a Lorentzian form of noise spectrum [6], [50], [53], [86], [87], [89], [90]. The corner frequency of the Lorentzian spectrum is ~ 30 Hz before irradiation and ~ 120 Hz after irradiation. These results may reflect the passivation of a pre-existing defect with lower corner frequency and activation of a new defect with a higher corner frequency. Alternatively, small changes in position, energy, or bond angles with surrounding atoms, induced by nearby radiation-induced trapped charge, may have altered the observed frequency response due to the same defect [6], [53], [58].

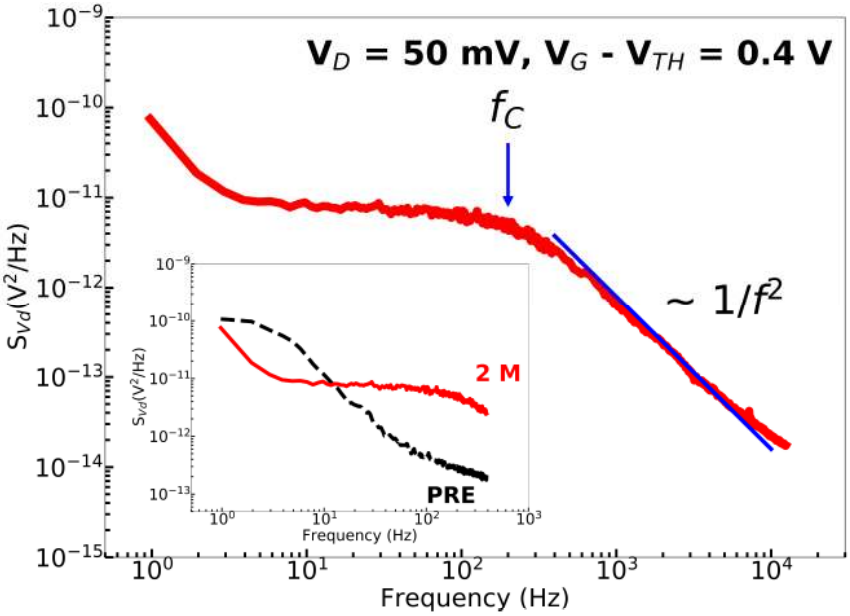


Fig. IV-2. Frequency dependence of S_{Vd} in the extended range f = 1 Hz to 12.5 kHz, measured with V_g - V_{th} = 0.4 V and V_d = 0.05 V, for an irradiated bulk FinFET. Inset: *1/f* noise before and after irradiation in the frequency range f = 1 Hz to 390 Hz.

Fig. IV-3 presents channel resistance fluctuations as a function of time for the same device as in Fig. IV-2 measured under the same bias conditions. The purple line depicts switching between two stable states known as the random-telegraph noise (RTN), indicating the presence of a prominent single defect and confirming the observation from Fig. IV-2.

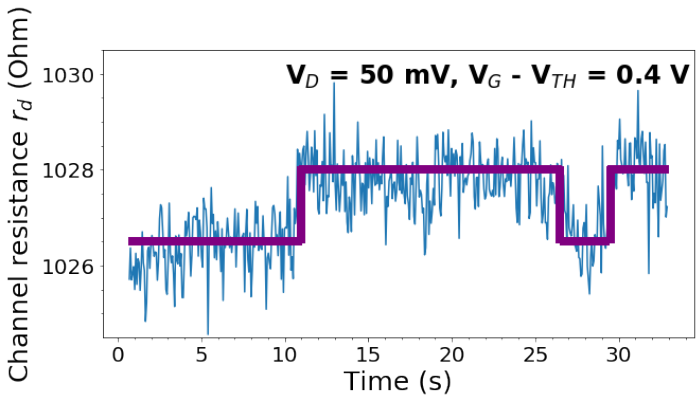
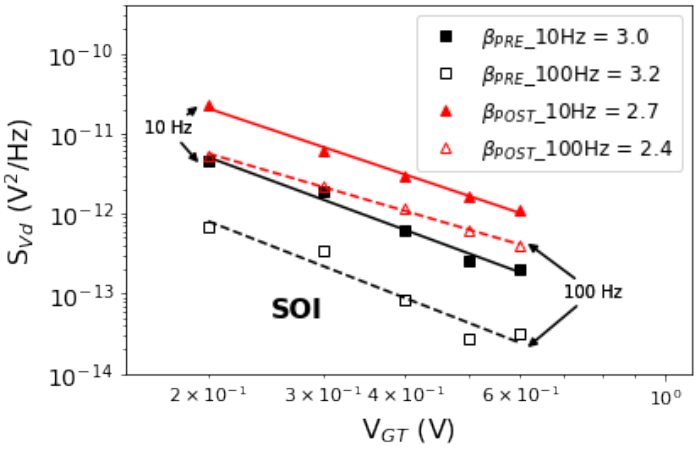
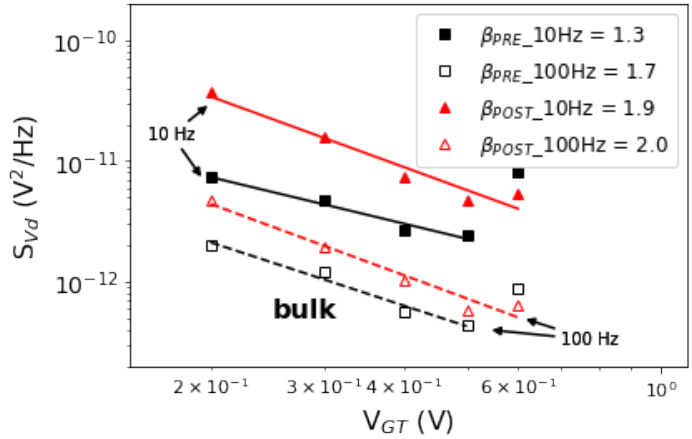


Fig. IV-3. Channel resistance fluctuations ($R = V_D/I_D$) as a function of time for the same measurement conditions.

Fig. IV-4 shows the gate-voltage dependence of the low-frequency noise of (a) SOI and (b) bulk FinFETs before and after irradiation. Solid and dashed lines represent the gate-voltage dependences $\beta = \partial \ln S_{Vd} / \partial \ln |V_g - V_{th}|$ calculated at 10 Hz and 100 Hz, respectively. Spectra deviating significantly from a $1/f$ shape due to significant contributions from RTN (e.g., Fig. IV-3) are excluded from these particular comparisons. Deviations from $\beta = 2.0$ and $\alpha = \partial \ln S_{Vd} / \partial f = 1.0$ are caused by non-uniform defect-energy distributions that are responsible for the observed noise [6], [58], [85]. When the defect energy distribution is increasing towards midgap, values of β are greater than 2.0 [6], [85], [89], e.g., as for the SOI devices in Figs. IV-4, IV-5, and IV-6. When the defect energy distribution is increasing towards the conduction band, values of β are less than 2.0 [6], [85], [89], e.g., as for the bulk devices in Figs. IV-4, IV-5, and IV-6. At least some of these differences may be due to defects in the near-channel BOX for the SOI devices [91]–[94] and the near-channel STI for bulk FinFETs [87], [88]. After irradiation, the defect concentration in these devices is larger, leading to a higher noise magnitude, and the defect-energy dependence is more uniform, with $\beta \approx 2.0$.



(a)



(b)

Fig. IV-4. S_{Vd} at f = 10 Hz (closed symbols) and 100 Hz (open symbols) versus V_g–V_{th} for (a) SOI and (b) bulk FinFETs with W= 40 nm, L=30 nm, N=5 before (squares) and after (triangles) irradiation. The bias condition during irradiation for all devices is ON-state. Lines are aids to the eye.

Fig. IV-5 shows normalized noise magnitudes for pristine bulk and SOI FinFETs with different fin numbers. SOI and bulk FinFETs with fewer fins exhibit 3-10 times higher noise magnitudes than ones with more fins, suggesting that some individual fins have higher than usual densities of as-processed defects [75], [95]. For 10-fin devices, these effects are relatively less important since *1/f* noise is inversely proportional to the effective fin width of the transistor [6]; therefore, the noise contribution of each fin is inversely proportional to fin number.

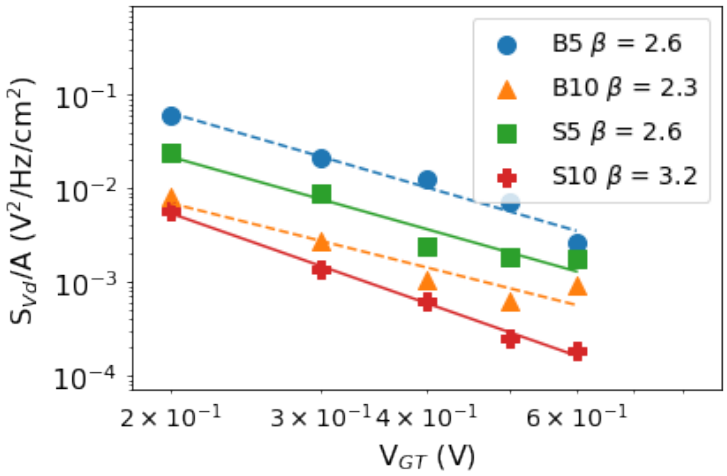


Fig. IV-5. Normalized S_{Vd} as a function of frequency for 5-fin and 10-fin SOI (solid lines, S5 and S10) and bulk (dashed lines, B5 and B10) FinFETs with approximate β values shown in the inset.

4.2 Temperature dependence of *1/f* noise

4.2.1 Bulk FinFETs

Fig. IV-6 shows the normalized low-frequency noise magnitude at $f = 10$ Hz as a function of temperature for pristine bulk devices, and for bulk devices irradiated with $V_g = +0.5$ V up to 1 Mrad(SiO_2). Here the upper horizontal scale represents the effective border-trap energy E_0 for cases in which Eq. (1) is valid [50]. The geometry parameters of the irradiated device are $L_{GATE} = 30$ nm, $W_{FIN} = 10$ nm; and $N_{FIN} = 10$. With irradiation, the effective densities of border traps increase significantly for temperatures of ~ 170-190 K and above 250 K for the bulk device in Fig. IV-8. After irradiation, a peak appears in the noise magnitude of the bulk devices in Fig. IV-8 at a temperature T of ~180 K (0.46 eV). An overall increase is observed, relative to pre-irradiation values, for 240 K < T < 320 K. These increases are associated with radiation-induced trapped charge [71], [84]. The normalized noise level is generally much higher (~1-2 orders of magnitude) for the pristine and irradiated bulk FinFETs in Fig. IV-6 than for the SOI FinFETs in Fig. IV-7. This high noise level for the bulk device may be due to the high defect density near the Si/STI interface in the sub-fin region in as-processed devices.

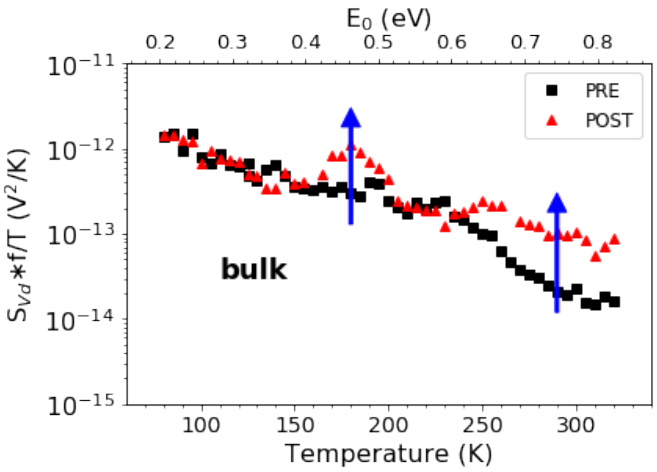


Fig. IV-6. Normalized low-frequency noise from 80 K to 320 K at f = 10 Hz for bulk FinFET irradiated to 1 Mrad(SiO_2) at V_g = +0.5 V. The device was biased at V_g–V_{th} = 0.4 V and V_d = 0.05 V during the noise measurements.

4.2.2 SOI FinFETs

Fig. IV-7 shows the normalized low-frequency noise magnitude at f = 10 Hz as a function of temperature for pristine SOI devices, and for SOI devices irradiated with V_g = +0.5 V up to 1 Mrad(SiO_2). Here the upper horizontal scale represents the effective border-trap energy E_0 for cases in which Eq. I-4 is valid [50]. The geometry parameters of the irradiated device are L_{GATE} = 30 nm, W_{FIN} = 10 nm; and N_{FIN} = 8. The noise magnitude for the SOI FinFETs is relatively constant before irradiation in Fig. 12(b). After irradiation, there are peaks at ~110 K (0.28 eV), ~175 K (0.45 eV), and ~285 K (0.73 eV). Liang *et al.* attribute noise peaks at similar energies in black phosphorus (BP) MOSFETs with HfO_2 gate dielectrics with a reversible motion of H^+ between sites in the near-interfacial HfO_2 and a BP surface site in response to the applied bias [15]. This H^+ shuttling also occurs in Si-based MOS devices with HfO_2 gate dielectrics [96], suggesting similar motion may occur in these devices. Other peaks in the noise spectra are most likely associated with O vacancies [6], [89].

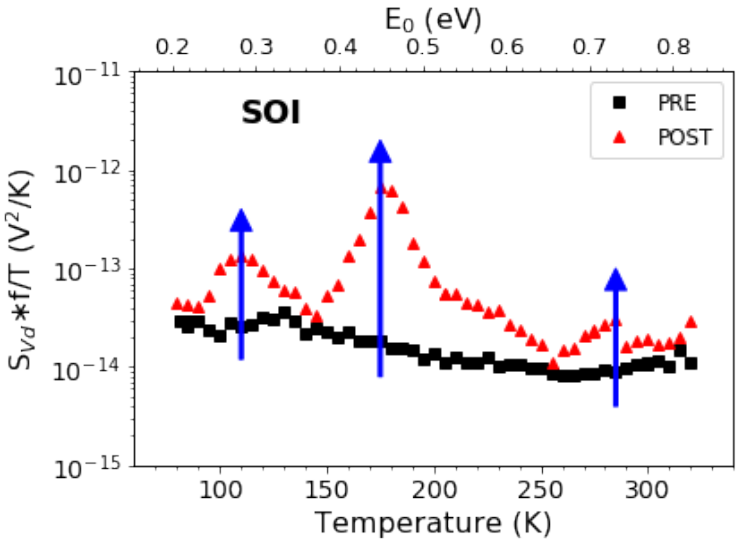


Fig. IV-7. Normalized low-frequency noise from 80 K to 320 K at f = 10 Hz for SOI FinFET irradiated to 1 Mrad(SiO_2) at V_g = +0.5 V. Devices were biased at V_g–V_{th} = 0.4 V and V_d = 0.05 V during the noise measurements.

4.3 Conclusions

In this chapter, the influence of ionizing irradiation on *1/f* noise was discussed. *1/f* noise was analyzed for room temperature and for cryogenic and elevated temperatures. Large increases are observed in post-irradiation low-frequency noise, accompanied by prominent random-telegraph noise. The gate-voltage dependence of the noise indicates that the defect-energy distributions of as-processed bulk devices considered in this study generally increase towards the conduction band, while that of as-processed SOI devices generally increase towards midgap, the summary of β is provided in Table II. The low-frequency noise in the bulk devices is attributed to oxygen vacancies in the gate dielectric and H^+ shutting in the near-interfacial oxides. For the SOI devices, significant contributions from defects in the buried oxide are also evident. These results provide insight into the nature, density, and energy distributions of defects in highly-scaled, as-processed and irradiated, bulk and SOI devices.

TABLE II

AVERAGE *B* VALUES FOR SOI AND BULK FINFETS

SOI FinFETs			
Fin width, nm	10	20	40
Pre-rad	2.6±0.4	3.0±0.5	3.2±0.2
Post-rad	2.4±0.6	2.9±0.8	4.05±0.03
BULK FinFETs			
Fin width, nm	10	20	40
Pre-rad	1.3±0.5	2.0±0.6	1.3±0.1
Post-rad	2.3±0.2	1.6±0.3	2.4±0.1

CONCLUSIONS

Highly-scaled bulk and SOI FinFETs demonstrate enhanced degradation under ionizing irradiation due to increased leakages and the greater effects of single prominent defects.

Net positive oxide-trap charge in the BOX and interface and border traps in the gate dielectric are found to contribute to threshold voltage shifts for SOI devices. Trapped charges in the STI have the most significant effects on the TID response for bulk devices. Similar trends with fin width are observed in both bulk and SOI devices as found in longer-channel devices, with enhanced charge trapping in the shortest- and narrowest-channel devices for bulk FinFETs, and in the shortest and widest-channel devices for SOI FinFETs.

Large increases are observed in post-irradiation low-frequency noise, accompanied by random-telegraph noise. The random telegraph noise results from the generation of individual/small numbers of defects, which have greater relative effects on smaller devices than larger devices. The gate-voltage dependence of the noise is consistent with non-uniform defect-energy distribution, specifically, it indicates that the defect-energy distributions of as-processed bulk devices considered in this study generally increase towards the conduction band, while that of as-processed SOI devices generally increase towards midgap. The low-frequency noise in these devices is attributed to oxygen vacancies in the gate dielectric and H^+ shutting in the near-interfacial oxide.

FinFET technology is an intermediate step on the road to microelectronics miniaturization. At the scale of devices studied in this work it slowly loses the benefits of enhanced gate control due to fringing fields caused by small dimensions, band-to-band tunneling caused by radiation-induced charge, and the increased impact of single defects in the near interfacial region due to narrow and short channel effects. It requires further advancements to better withstand TID exposure for 30-nm devices or it will be replaced by more promising technological solutions.

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