Total Ionizing Dose Hardened and Mitigation Strategies in Deep Submicrometer CMOS and Beyond

Eleni Chatzikyriakou, Katrina Morgan, *Member, IEEE*, and C. H. Kees de Groot, *Senior Member, IEEE*

***Abstract*— From man-made satellites and interplanetary missions to fusion power plants, electronic equipment that needs to withstand various forms of irradiation is an essential part of their operation. Examination of total ionizing dose (TID) effects in electronic equipment can provide a thorough means to predict their reliability in conditions where ionizing dose becomes a serious hazard. In this paper, we provide a historical overview of logic and memory technologies that made the biggest impact both in terms of their competitive characteristics and their intrinsically hardened nature against TID. Further to this, we also provide guidelines for hardened device designs and present the cases where hardened alternatives have been implemented and tested in the lab. The technologies that we examine range from silicon-on-insulator and FinFET to 2-D semiconductor transistors and resistive random access memory.**

***Index Terms*— 2-D semiconductor, carbon, CMOS, deep submicrometer, FinFET, graphene, MoS2, resistive random access memory (RRAM), silicon-on-insulator (SOI), thin film, total ionizing dose (TID), ultrathin buried oxide (UTBOX).**

I. Introduction

In a radiation harsh environment, complex mechanisms take place which contribute to disturbances in the normal operation of electron devices. In space, energetic protons and other nuclei from galactic cosmic rays as well as energetic electrons and protons in the Van Allen belts impinge on spacecraft equipment at fluxes dependent on the mission journey followed [1]. Solar flares can induce coronal mass ejections with fluxes of electrons and ions that can reach the earth a few days after an event is initiated. Aviation electronics could also be subjected to terrestrial gamma-ray flushes, emanating from thunderstorms, and carrying gamma rays of energies up to tens of megaelectronvolt [2], [3].

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In high-energy physics establishments such as particle accelerators and nuclear power plants, energetic particles used for their operation and their ionizing products gradually degrade electronic devices operating close to areas of increased exposure [4], [5]. Sensory equipment, robotic control and telemetry, and data acquisition electronics can all be affected in such harsh environments [6].

One characteristic of the radiation that reaches on-board and other shielded electronics is that it is different than that found in the environment as a result of secondary particle emission from adjacent materials and equipment, as well as radioactivity that may be intrinsic to the materials used for shielding and packaging or resulting from radiation interactions [7].

Total ionizing dose (TID) describes the process by which degradation is gradually induced in the electronic devices as a function of the total dose incident in the device and is usually used to make a distinction between the dose-dependent mechanisms in which the effects of the total dose are more pronounced when the irradiation is taking place under low dose rate (enhanced low dose rate sensitivity) [8].

Particle interactions that can ionize matter are the photoelectric effect, Compton scattering, electron-positron pair production, and Bremsstrahlung and inelastic collisions. Photons, electrons, positrons, protons, and other ions all participate in such processes whose sequence is defined by the energies of the aforementioned particles [7].

Electrical equipment that is to be used in a radiation-harsh environment should be thoroughly tested. Radiation hardening is an elaborate process that involves many different layers of testing before the products are finally available. Radiation hardening can be of different types and at different levels. Hardening by process is performed at the technology level and involves changing materials and fabrication processes to suite particular needs for harsh environments. Hardening by design involves changing the structure of the integrated circuits (ICs) in ways that can mitigate the effects of radiation [9]–[11]. As a result of the extra production steps, the final technologies and circuits used for radiation applications lag behind the ITRS map [12].

In this paper, we explore deep submicrometer and beyond-CMOS technologies, and especially those that have exhibited an intrinsic hardness to TID effects. This includes off-the-shelf

commercial solutions as well as other technologies that are still under research as replacements for Si CMOS. Initially, in Section II, we list terminology of TID effects on device characteristics that will be presented further in the text. Section III focuses on silicon-on-insulator (SOI) technologies, the effect of shallow trench isolation (STI), and the response of ultrathin body (UTB) and buried oxide (BOX) FETs. In Section IV, TID response of FinFETs and multigate technologies is described, and in Section V, nanowire (NW) as well as 3-D stacking of fins and NWs is described separately. In Section VI, the novel effects that arise in thin film and 2-D semiconductor FETs are described in detail along with those in carbon nanotube FETs, and last, in Section VII, TID effects in resistive random access memory (RRAM) are discussed. This paper is not an exhaustive listing of all the technologies that have been examined for their TID response; however, we hope that the reader will gain a general overview of the mechanisms that take place during TID exposure as well as insights toward TID resistant technology designs.

II. TID Effects on Device Characteristics

Ionizing radiation causes electron-hole pairs to be produced inside the electronic components. These free carriers, when trapped in preexisting trapping sites in CMOS devices, can significantly alter the characteristics of the latter, causing temporary, or permanent failures in ICs. The magnitude of the electron-hole pairs produced is a function of: 1) the type of incident radiation and 2) the electric field that exists in the material at the time of irradiation [13]. The most important characteristic of this mechanism is that mainly positive charges are aggregated inside the bulk of the material, as electrons can escape much faster. This is translated to the effects of TID being more important in n-channel transistors, where the charges take on the role of positive bias and induce threshold voltage shifts (ΔV_{th}) and leakage paths which depend on the device architecture and manifest as OFF-state current (I_{off}). Mobility degradation is also observed under TID, both in n-channel and p-channel devices and results from scattering centers created at and close to the semiconductor/oxide interfaces (interface traps) in the oxide [14].

The final changes in device characteristics are, however, separated from the underlying mechanisms that take place, which depend on the structure and materials used. In the following, we use the term scaling to refer to the concerted effort to reduce the final IC size as well as its power consumption either through reducing the size of the components, or from examination of alternative, novel technologies.

III. Silicon-on-Insulator and Shallow Trench Isolation

Historically, SOI technologies were introduced in submicrometer gate lengths around 150 nm and involve the separation of the active silicon volume by an oxide layer (the BOX) which provided multiple advantages that assured increased performance in line with scaling. Research on radiation hardness of SOI was sparked by the idea that a smaller active silicon volume would, contrary to bulk transistors, reduce

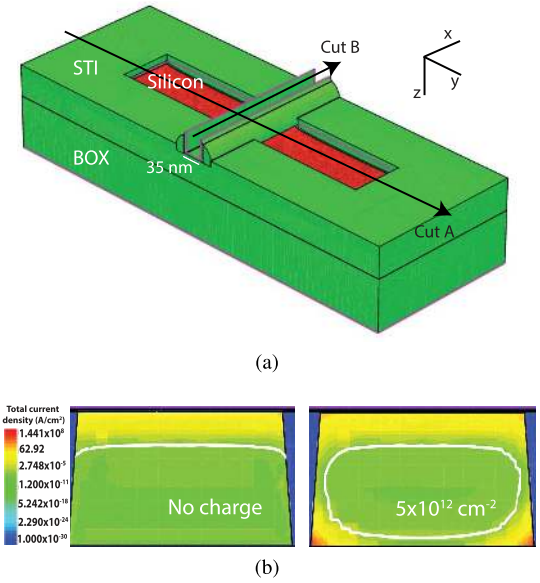

Fig. 1. (a) 3-D view of 45-nm PDSOI nMOSFET. (b) Cross section of the device along cut B in (a) showing the OFF-state leakage current formed in the bottom corners of the top silicon film for no oxide charge and effective areal oxide charge of 5×10^{12} cm^{-2} in the field oxides (from [17]).

charge collection from traversing ions that cause single event effects. However, it was shown that in practice SOI transistor ICs were also susceptible to charged particle effects [15]. More recent scaled bulk devices have shown significant improvement in the effects caused by heavy ions, such as soft error rates in memory components, and especially some SOI technologies like the 28-nm FDSOI have achieved major improvement (up to 110×) compared to their bulk counterpart [16].

However, in terms of the TID hardness, the inclusion of the BOX increases the volume for charge trapping caused by ionizing radiation. Field oxides have in fact become the focus of all studies when, in order to satisfy scaling demands, thinning of the SiO_2 gate oxide increased quantum mechanical tunnelling of trapped charge. Thicker gate insulators of materials with a high dielectric constant (high-k) were introduced when SiO_2 had to be thinned down to dimensions that allowed electrons to tunnel through. But even in these cases, charge trapping in gate insulation was not a problem to their TID response [18]. Charges aggregated in the field oxides, namely, the intradevice isolation regions such as the BOX and the interdevice isolation such as the STI, induce drain-to-source I_{off}. In bulk transistors, the charges gathered at the STI contribute further to interdevice leakage current from n+ source/drain or n-well regions of adjacent transistors in a CMOS circuit [19].

TID hardness exhibited an increase with device scaling for specific SOI technologies until the 32-nm nodes [20]. Among the most notable commercial submicrometer transistor technologies to show an intrinsically hardened nature to TID were partially depleted SOI (PDSOI) MOSFETs, and especially at the 45-nm node and beyond [21]–[23]. A schematic of 45-nm PDSOI MOSFET is shown in Fig. 1(a). The positive charges that are gathered at the STI and BOX create what was initially termed a "back-gate" parasitic transistor [19].

Finite-elements method (FEM) simulations have revealed that the charges are mainly trapped at the bottom corner of

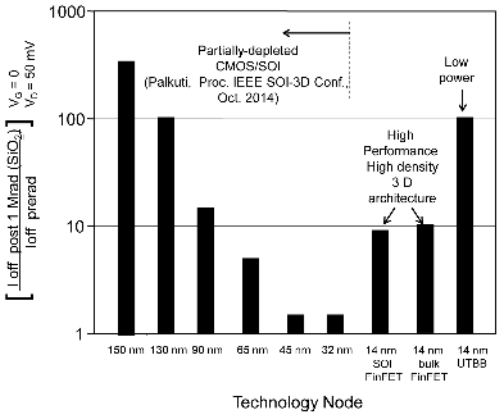

Fig. 2. TID hardness trend for commercial transistor technology nodes for irradiation at 1 MRad (SiO_2). Reprinted with permission from [26]. Copyright 2015, IEEE.

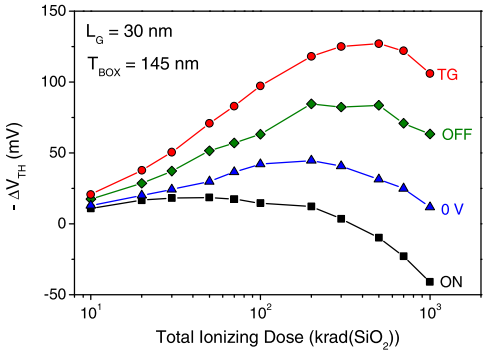

Fig. 3. Front gate ΔV_{th} as a function of TID for an ETSOI device with L_g = 30 nm and BOX thickness of 145 nm, under different bias conditions. Reprinted with permission from [31]. Copyright 2013, IEEE.

the STI, adjacent to the BOX, and this creates leakage paths at the bottom silicon corners, as shown in Fig. 1(b) [24], [25]. However, further examination shows that the high body doping used in this device makes it immune to the formation of a leakage path up to very high total doses, and furthermore, that there exists a threshold above which no further charges are being trapped due to an equivalent positive charge density aggregating at the bottom of the BOX [17]. This reveals that, rounding the bottom STI/silicon corner can further increase the radiation hardness of the device as this would reduce the intensity of the electric field and prevent the creation of the corner leakage paths.

In fully depleted SOI, positive charge in the BOX can induce many complex mechanisms, such as coupling of the front with the parasitic transistor [27] and a total dose latch phenomenon [28]. This situation can be mitigated with the use of a back contact, or body doping schemes, which, however, increase device complexity.

The overall increased TID hardness of commercial transistor technologies down to the 32-nm nodes is reflected in Fig. 2 which shows the pre- to post-I_{off} percentage at 1 MRad (SiO_2) as a function of transistor scaling [26]. The increased TID hardness trend stops after 32-nm technologies, where overcoming scaling issues creates a rich landscape of alternatives.

Another issue that arises in planar transistors at 50 nm and beyond is statistical variability from sources such as random dopant fluctuations (RDF), which can reach up to 50% of total variability [29]. Therefore, FDSOI transistors that include a doped silicon body to mitigate latch phenomena are susceptible to RDF. At the same time, the TID hardness of 45-nm PDSOI MOSFETs is reduced when RDF effects are taken into account, which could be a problem for some lower levels of doping [17].

Beyond 32-nm ultrathin BOX (UTBOX) devices for lower power applications were introduced. These devices feature a BOX of 25 nm down to a few nanometer that, when combined with UTB, results in very good electrostatic control of the gate and reduced variability originating from RDF effects [32]–[36]. UTB and BOX (UTBB) device performance is enhanced compared to extremely thin SOI (ETSOI) [37], both in terms of short channel effect control and S/D coupling due to the use of the thin BOX, and especially when combined with a ground plane doping scheme [38].

ETSOI device performance after TID exposure exhibits similar characteristics with that of FDSOI, namely, the electrostatic coupling between the front and back parasitic channels is the dominant effect. The front gate threshold voltage shift (ΔV_{th_front}) in devices with BOX thickness, T_{BOX} = 145 nm and Si film thickness, T_{Si} = 8 nm, has shown a bias dependence during irradiation with transmission gate being the worst bias condition due to the distribution of the electric field lines in the BOX [30], [31]. ΔV_{th_front} as a function of total dose for different bias conditions is shown in Fig. 3. In this case, the reduction in ΔV_{th_front} has been attributed to counterbalancing negative interface trap buildup at the interface of the silicon film with the gate and BOX. Throughout this paper, we examine cases where this characteristic can or has been used to increase the radiation hardness of different technologies.

UTBB transistors do not show a bias dependence on their TID characteristics as there is not enough space in the thin BOX for the electric field lines to assume varying directions. In these devices, although the leakage current is reduced, strong coupling between front and back transistors is induced, equivalent to ETSOI and FDSOI in general, and therefore there is no advantage in their use, while GP doping schemes do not alter the response significantly [30], [31].

The only exception to the previous rule is the case of T_{BOX} = 11 nm that showed no significant ΔV_{th} up until 200 kRad(SiO_2). This, combined with the information induced from Fig. 3, could mean that UTBB devices with very small BOX thickness, that may include passivated negative interface traps, could provide interesting postirradiation characteristics. Therefore, alumina BOX and composite SiO_2/alumina UTBOX transistors such as those reported in [36] (Fig. 4) are very interesting for examination.

UTBOX configuration is also advantageous for the creation of low-power one-transistor DRAMs. Thus, floating body RAMs with UTBOX have been investigated for their TID response, and showed that exposure to TID reduces both the read window and the retention time [39]. Reduction of the memory window in the n-channel UTBOX MOSFETs is

Fig. 4. UTBB SOI architectures with Al_2O_3 and composite BOX as reported in [36].

caused by the threshold voltage shifts of the front and back gate transistors and retention time is reduced when leakage current is induced in the device. The worst irradiation bias was found to be the HOLD DATA, with both the front and back gates biased at 1 V. This produced the highest shift in the memory window. However, it was also revealed that the back gate bias could be used to alleviate the effects of the irradiation by using a lower voltage. Due to the inherent operation of the device, decreasing the back-gate bias also increases retention time, and is therefore a useful way of reducing the TID effect on the final characteristics.

IV. FinFETs and Other Multigate Architectures

Multigate devices provided the answer to variability-induced problems in planar submicrometer transistors [40], [41] and were mainly introduced by manufacturers at 22-nm nodes and beyond. The FinFET has been established as the workhorse of the semiconductor industry for high performance down to 10-nm nodes [12]. Notably, the commercial 22-nm bulk tri-gate technology shows increased immunity against many reliability effects, including bias-temperature instability and stress-induced leakage current [41].

The TID response of multigate devices is slightly more complex than that of planar, as more factors come into play. Thorough reviews are provided in [42] and [43]. Here, we stress on the role that the distribution of trapped charge in the field oxide plays for the emergence of this complexity.

Fig. 5 shows a simplified schematic of bulk and SOI FinFETs with the directions that the width and thickness are measured. The introduction of multiple gates creates an environment where the control of the electrostatic potential induced in the fin and the isolation regions from the lateral gates largely defines the TID response of the whole device. Therefore, wide-fin devices have shown reduced hardness when compared to narrower fin SOI devices [44], [45]. By contrast, in bulk FinFETs, the opposite is true where wide fins increase the TID hardness [46]. Using FEM simulations, the latter has been shown to be due to the proximity of the STI sidewall closer to the middle of the fin, where it increases the electrostatic potential, thus increasing the effective width of the parasitic-channel transistor. Accordingly, the BOX introduced in SOI technologies defines the final characteristics of the parasitic channel formed adjacent to it. By reducing the width of the fin, the lateral gates move closer and the electric field lines inside the BOX are distorted so as the majority of the holes move away from the Si/BOX interface, thus protecting the back-channel region [47].

In terms of channel length, longer fins in bulk devices are also less susceptible to TID because the density of the charge

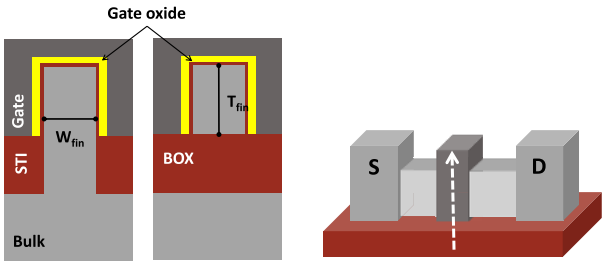

Fig. 5. Simplified (a) 2-D and (b) 3-D views of bulk and SOI FinFET structures. The width and thickness are measured perpendicularly to the gate length axis. The shape of the fin can vary significantly.

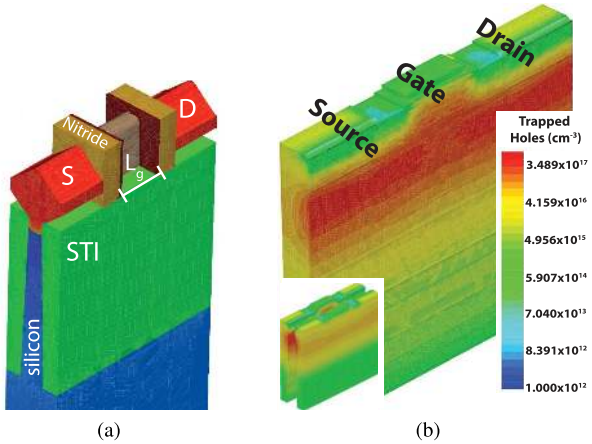

Fig. 6. (a) 3-D structure of 22-nm FinFET structure. (b) Trapped charge concentration in the STI with bulk donor trap density of 8.2×10^{17} cm^{-3} (from [50]).

trapped does not depend on the channel length. As such, the electrostatic force experienced by the electrons in the leakage path is more intense with short-channel lengths [46]. In SOI FinFETs, the electrostatic potential of the gate reduces when the gate length decreases, and therefore charges trapped in the BOX dominate the TID response. Therefore, for gate lengths less than 40 nm, it is advised to use an SOI structure that gives more control over the channel, such as the gate-all-around (GAA) described in Section V [43].

The bias during irradiation influences the distribution of the charges in the isolation regions, with ON bias conditions for SOI nFinFETs inducing more pronounced TID effects due to the holes being trapped higher in the BOX, and closer to the active silicon region [48]. In four-gate 90-nm bulk FinFETs, the OFF state ($V_D = 0.7$ V) has been shown to be the worst bias condition for irradiation due to a higher electric field present at the STI corner compared to the rest of the bias conditions examined [49]. The TID response, however, also depends on the doping distribution in the neck region of the fin. In Fig. 6, the distribution of trapped charge in the STI is shown in a 22-nm bulk FinFET in the ALL-0 bias regime. This distribution is solely defined by the doping concentration in the silicon [50]. When the majority of the trapped charge is located deeper in the STI from the surface the path length of the electrons in the parasitic channel increases compared to when it is located at the vicinity of the S/D regions.

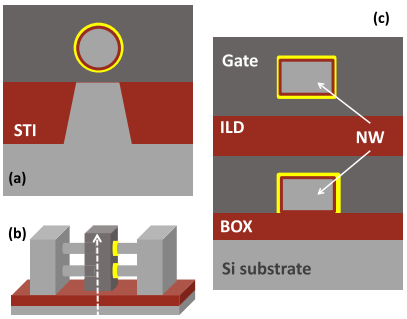

Fig. 7. Types of NWFET architectures. (a) GAA NW FET on bulk substrate. The 2-D cut is taken in the direction shown below. (b) 3-D view of NW FET that includes stacking tiers of NWs. (c) 2-D cut of stacked NWs in a 3-D architecture. The first NW is placed on top of the SOI. Subsequent tiers are fabricated in a GAA design [57].

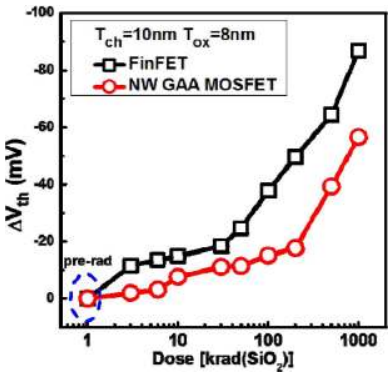

Fig. 8. ΔV_{th} of GAA NW FETs and FinFETs with 10- nm-thick NWs and fins respectively and $t_{ox} = 8$ nm. Reprinted with permission from [58]. Copyright 2015, IEEE.

At last, the type of architecture (Π-gate, Ω-gate, and trigate) has also been shown to influence TID response, with increased "wrapping" around the channel providing higher immunity to TID [47].

V. Nanowires and 3-D Stacking

NW FETs are extremely scaled FinFETs [51], [52]. In this case, the channel is fabricated either on an SOI substrate, or free standing by isotropic etching followed by deposition of the gate dielectric and the metal gate [Fig. 7(a)] [53]. In the latter case, the device is called GAA FET. Another option is to grow the NWs vertically using, for example, conformal chemical vapor deposition [54], dry etching with reduced oxidation techniques [55], or ion beam etching and the spacer etch technique presented in [56].

Stacking the NWs in tiers is also an efficient method of device integration, fully 3-D in nature [52]. NWs are stacked on top of each other with each channel being wrapped by a gate oxide stack and the gate. The first tier in this case could be implemented as in SOI architectures.

For NWs that are fabricated on SOI substrates, the width of the latter can affect the TID response of the device. In fact, threshold voltage shifts and subthreshold slope degradation have been observed in 30-nm gate-length nNWFETs, which was attributed to field oxide and interface trapped charges, respectively [57]. Furthermore, with FEM simulations, Gaillardin *et al.* [57] showed that the major influence in the leakage path formation originated from the BOX, instead of the S/D capping layer oxides. In the same work, the effect of changes in the gate length of the NW in the TID response were also examined. Longer nNWFETs exhibited increased TID hardness compared to the shorter gate counterparts. Overall, the geometric dependencies for these devices were similar to SOI multigate FinFET n-channel devices described earlier. It would be interesting to examine the response of stacked nNWFETs as having their channels wrapped completely by the gate, they could also prove hardened against TID effects.

The scenery is different for GAA FETs. Originally, GAA FET architectures to be tested for their TID response featured thick gate isolation oxides, which aggregated trapped holes in bulk and border/interface traps [19]. The postrad device characteristics were then dependent on the interplay of the trapping and annealing mechanisms of the latter [59], [60]. Modern GAA FETs, however, feature thin high-k/SiO_2 gate stacks, which, combined with the complete "wrap" of the channel from the gate, eliminate the aforementioned problem, and making the GAA devices exceptionally hardened against TID (Fig. 8) [58], [61]. The devices in [58] feature 10- and 20-nm InGaAs NW channels with 8-nm Al_2O_3 gate oxide. Using FEM simulations, it was shown that the electric field in the 20-nm NW FETs was stronger, which slightly aggravated the postirradiation device response. For thinner gate oxide thickness, high electric fields can also favor quantum mechanical tunnelling, and therefore reverse this situation. In the same study, the use of forming gas anneal has shown to increase radiation hardness by increasing the quality of the Al_2O_3/InGaAs interface.

For all the technologies described so far, the role of the thick field oxides in the postirradiation response is dominant. Although for further scaled devices more factors come into play, field oxides still contribute significantly with competing effects for positive bulk oxide and negative interface charge buildup. Therefore, FEM simulations can elucidate the role played from each and aid during device design [62], [63].

VI. Thin Film, 2-D Material, and Nanotube Transistors

The 2-D and 1-D channels have become increasingly attractive solutions for highly scaled electronic devices. These materials exhibit a range of interesting properties. The high mobility of graphene was found suitable for high-frequency FETs [64], while low stand-by power transistors have been exhibited with single-layer MoS_2 [65]. CNT FETs have also shown superior mobility and threshold voltage variability characteristics due to the lower atomic dislocations present in the channel. Single wall (SW) CNT (SWCNT) FETs exhibit ballistic transport that makes these devices better candidates for RF performance [66]–[68].

Due to their large surface to volume ratios, 2-D and 1-D semiconductors undergo doping mechanisms during both the fabrication process and irradiation which dominate the final

device characteristics. Such mechanisms are more pronounced in ambient conditions, due to the large percentage of potential doping species that exist [69]. Postirradiation, secondary electrons, and protons that are released through Compton scattering processes have the potential to induce defects [70]. As a result, to understand the TID response and implement any hardening solutions, we need to be able to discriminate between intrinsic effects taking place in the 2-D channel and extrinsic effects taking place in the rest of the device, such as the dielectric layers. This is done in different ways, both analytically from the extracted device characteristics [71] and with the help of supplementary measurements, such as Raman spectroscopy [70]. When materials such as graphene and carbon nanotubes are used for the fabrication of TFTs, their postirradiation response shares many common features with 2-D and 1-D channel transistors. Unless otherwise stated, all devices described next have a back-gated configuration, for which we use V_g to denote the gate bias. The gate dielectrics in this case separate the thin film or 2-D channel from the Si substrate.

In p-type network channel SWCNT TFTs with 100-nm SiO_2 gate dielectric and 32/32 W/L ratio, negative ΔV_{th} of the order of 1 V was observed when irradiated in vacuum with a back gate voltage of 2 V, and was attributed to holes created during irradiation, migrating toward the SiO_2/SWCNT interface, increasing the electrostatic potential, and therefore requiring more negative voltages to turn the transistor on [69]. Further irradiation of the same transistors in air resulted in positive ΔV_{th} approximately 37 times greater and increased channel conductance. Raman spectra and mobility measurements showed that atomic lattice defects of the film were not the main cause of the postrad shifts, but rather the interactions of these defects with O_2, H_2O, and water-oxygen redox couples that were weakly adsorbed at the surfaces of the nanotubes and other charge trapping sites at their vicinity and at the surface of the SiO_2.

Similar results were obtained in another study for p-type SWCNT network TFTs irradiated in air [72], and furthermore revealed improved junction contact performance after irradiation. The density of the CNTs on the film also plays an important factor as higher density CNTs contribute to reduced adsorption mechanisms. N-type CNT TFTs of both array and network type were also examined in the same study, where the surfaces of the films were covered with Si_3N_4. Donors created in this insulating layer from the irradiation caused negative ΔV_{th}, but for network-type CNTs. The insulating layer also reduced the effect of irradiation, and therefore Zhao *et al.* [72] proposed covering the p-type devices with insulating layers that do not switch the polarity of the device, decreasing the thickness of the insulating layers to reduce the number of fixed charges introduced by them, and irradiating the device during fabrication to make the junctions saturated. Further to this, they exhibited TID-hardened logic inverters based on ambipolar TFTs by covering the p-type TFTs with Al_2O_3. SWCNT TFTs with a high degree of intrinsic TID hardness ($\Delta V_{\text{th}} < 0.25$ V and no appreciable change in mobility and maximum drain current when irradiated in vacuum, as shown in Fig. 9) have been fabricated using a thin Si oxynitride gate dielectric, taking

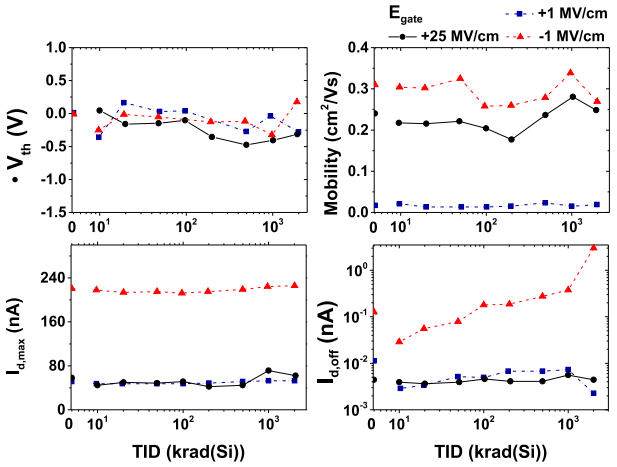

Fig. 9. (a) ΔV_{th} and changes in (b) mobility, (c) maximum drain current, and (d) OFF-state drain current of SWCNT TFTs with SiON gate dielectrics. Adapted with permission from [73].

advantage of the competing effect of holes trapped in the oxide and electrons at the interface to counterbalance the changes in the electric field [73]. This is the same mechanism that was described in Section III for hardened UTBB devices.

Mechanically exfoliated graphene ambipolar devices with 300-nm SiO_2 dielectrics exhibited increasing positive ΔV_{th} with increasing dose when irradiated in air with 10 keV X-rays at $V_g = -5$ V up to 300 kRad(SiO_2) [74]. However, a dose greater than 1 MRad(SiO_2) is required to induce ΔV_{th} in suspended graphene sheet devices where the SiO_2 film has been removed. With the help of Raman spectra, the shifts in the device characteristics have been attributed to p-type doping effects from O_2 and H_2O species that exist on the SiO_2 and in the ambient for the suspended devices. This can be further understood by the high formation energies that are required for displacement damage to take place in graphene [75].

On the contrary, when irradiated in vacuum, ambipolar graphene devices on 100-nm SiO_2 exhibited negative ΔV_{th} [76]. These devices, however, also included a trimethylsiloxy (TMS) monolayer between graphene and SiO_2 in order to stabilize the polarity of the electric field at the TMS/graphene interface and subsequently reduce gate hysteresis. This allowed Coulomb potential scattering mechanisms induced by the charges trapped at the SiO_2 dielectric to be examined. In another study, the memory window of nonvolatile FETs (NVFETs) with the graphene channel transferred onto 51 nm of lead-zirconate titanate (PZT), deposited on 100/10 nm Ti/Pt gate electrode and SiO_2/Si substrate has shown to remain nearly stable after TID exposure up to 1 MRad(SiO_2) [77] consistent with older studies on PZT thin film ferroelectric capacitors [78], [79] and polysilicon-nitride-oxide-silicon nonvolatile memory transistors [80]. The PZT layer in this case introduced an antihysteretic behavior in the device whose response was dictated by trapping mechanisms at the interface with graphene that largely remained unaffected after TID exposure. CNT NVFETs, however, with similar counterclockwise hysteresis in their characteristics exhibited an increase in the memory window with increasing

total dose [81]. Generally, due to the sensitivity of graphene to dielectric and substrate charge accumulation effects, it is thought to be more appropriate for ionizing radiation sensor applications [70], although, a tunable TID response scheme has been proposed in [82] using hybrid organic-inorganic dielectrics of various thickness and composition, such as zirconia-based self-assembled nanodielectric. These schemes take advantage of the competing electron and hole charge accumulation to achieve stable device characteristics, much like the SWCNT TFTs with SiON dielectrics mentioned earlier.

In contrast to the increased contribution of Coulomb scattering mechanisms from oxide and interface trapped charges in graphene FETs, mobility in MoS_2 increases with total dose when irradiated in vacuum ultraviolet conditions [83]. Transfer characteristics also revealed negative ΔV_{th} for all bias conditions. These two effects were attributed to charges trapped inside the gate oxide and at the interface of SiO_2 with MoS_2. Furthermore, it was found that larger ΔVth was produced in FETs with flakes of six-layer MoS_2 than in monolayer MoS_2, a phenomenon that was attributed to the differences in the proximity of the channel to the SiO_2 interface. When irradiated in ambient, MoS_2 transistors of similar structure exhibit positive ΔV^{th} which, however, is observed at much lower doses than negative ΔV^{th} when irradiated in vacuum [84]. Oxygen-induced surface traps on MoS_2 are believed to be the cause of these shifts, which are also thought to cause scattering-related mobility degradation in the channel.

VII. Resistive Random Access Memory

Resistive memory or RRAM is a promising next generation nonvolatile memory with properties superior to flash memory. Resistive memory improves as it scales and can be fabricated in a high-density cross-bar array, can operate at low power and has a very simple metal/switching-layer/metal structure [86]. The resistance of a RRAM cell can be changed between a high (HRS) and a low state (LRS), by altering an applied voltage, causing a conductive filament to reversibly connect and rupture between the two metal electrodes [87].

Resistive memory can be split into two types, dependent on the filament mechanism: 1) valence change memory (VCM) and 2) electrochemical metallization memory (ECM). VCM consists of a metal/oxide/metal structure where the conducting filament is constructed from oxygen vacancies and is known as anion memory [87]. A thorough review on its operation can be found in [88]. ECM, on the other hand, is a cation based memory with a soluble electrode leading to a metallic filament. Also known as conductive-bridging random access memory (CBRAM) or programmable metallization cells (PMC), ECM memories can have different types of switching layer materials such as metal-doped oxides, metal-doped chalcogenides, and solid electrolytes like SiC [89], [90]. The switching mechanism of an ECM cell depicted in Fig. 10 [85].

With very thin switching layers, often between 10–100 nm, and a switching mechanism based on conductive filaments rather than control of charge density, RRAM cells can be considered radiation hard by process [91]–[101]. However,

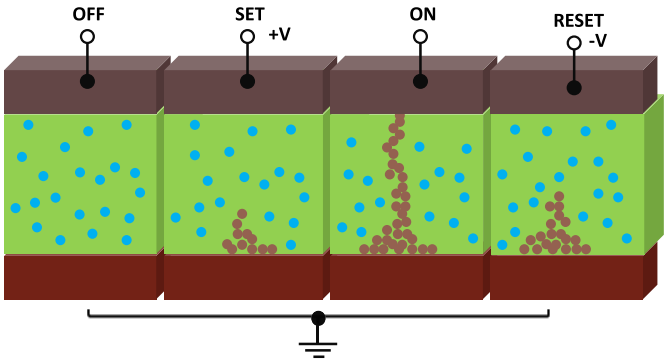

Fig. 10. Schematic representation of an ECM cell switching mechanism as suggested in [85]. During the OFF state, the Cu-doped ECM cell has no filaments present. During the SET operation, the Cu ions (blue dots) from the top electrode (Cu) dissolve into the switching layer and their number is reduced at the counter electrode (Pt) due to the applied bias. This continues until a complete metallic filament (gray dots) connects the top and bottom electrodes, resulting in the ON state. The process can be reversed by changing the applied bias, causing the filament to rupture (RESET).

such a large variety of materials, structures, and memory types leads to a variety of memory properties and radiation response.

In VCM, there are three main materials that have been the focus of research to date; TaO_x, HfO_x, and TiO_x although some research into SiO_x has also been conducted [92]–[94], [96], [99], [101]–[109]. Over the years, variations in radiation responses between different or even the same materials has been reported. Whilst some indicate VCM memory to be either completely resistant to radiation effects, other research observes changes in memory properties, although typically only at Mrad dose levels or above.

Similar to SiO_2 FETs, ionizing radiation of metal-oxides induces oxygen vacancies and charge. In the earlier work for HfO_x in particular, the lack of radiation response was attributed to the induced oxygen vacancies being too small in number comparable to the conductive filament, or that the induced charge was trapped in defect sites far from the conductive filament [107], [110].

A large amount of work, however, does report radiation effects in VCM memory at high doses which include changes in voltages, resistance, and in some cases, a complete switch of state [92], [93], [96], [102], [103], [106], [109], [111]–[114]. In these cases, it is thought that the induced charge and oxygen vacancies interfere with the conductive filament switching mechanism and/or the resistance of the oxide. Many mechanisms have been proposed. These mechanisms include trapping of radiation-induced charge at preexisting or radiation generated oxygen vacancies or defects and alteration or creation of internal electric fields and transient currents [92], [93], [96], [102], [104]–[106], [109], [111]–[114]. This can lead to obstruction of oxygen vacancy movement or joule heating which can, in turn, lead to the creation of additional oxygen vacancies [92], [102], [104], [115]. If field alterations or transient currents are large enough, state switching can occur [104], [112], [115].

A possible radiation physical mechanism for a TiN/HfO_x/Pt cell is reported in [94]. It is proposed that Hf-O bonds are broken upon radiation leading to the creation of oxygen

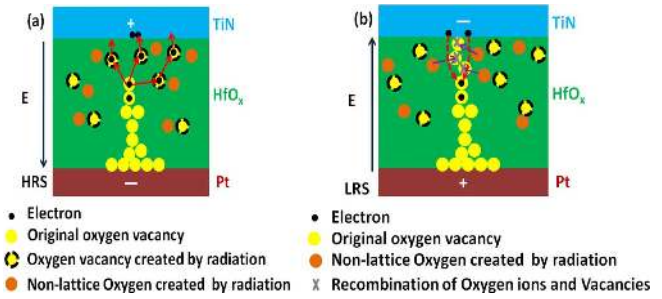

Fig. 11. Schematic of radiation effect mechanism when device is in (a) HRS or (b) LRS during irradiation of gamma rays. Electrons follow the red line and oxygen follows the purple line. Reprinted from [94], with the permission of AIP Publishing.

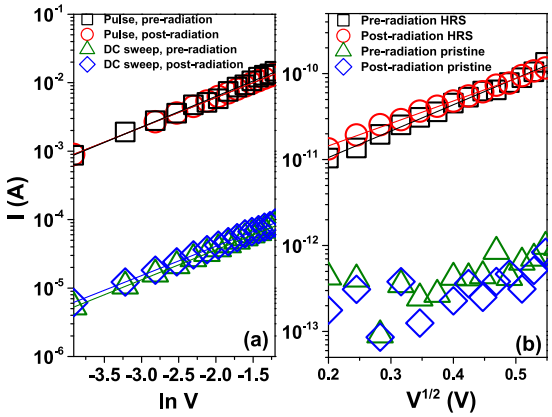

Fig. 12. Solid electrolyte SiC ECM memory cells exhibiting stable conduction mechanisms and resistance states following exposure to 2 Mrad of gamma radiation with (a) displaying LRS after pulsed and dc measurements with a gradient of 1.00+/−0.02, indicating Ohmic conduction and (b) displaying HRS and pristine state with a linear fit for I–$V^{1/2}$, indicating Schottky emission [130].

vacancies and nonlattice oxygen (Fig. 11). Upon cycling after radiation, the radiation vacancies in HfO_x, located far from the filament, are not recovered, and therefore lead to an average decrease of HRS resistance. When in HRS [as shown in Fig. 11(a)], with a partial filament present, the induced oxygen vacancies aid connection of the filament upon SET. When in LRS [Fig. 11(b)], nonlattice oxygen can recombine with oxygen vacancies in the filament and cause rupturing. Changes in crystallisation phase, dependent on radiation dose, in TiO_x have been reported more recently [114]. The radiation effect on crystallisation is an interesting topic on its own right, and shedding light on this mechanism can further aid in choosing appropriate materials for TID hardened applications.

One of the challenges that arises when creating a complete model of radiation effects of RRAM memory originates from variation that occurs at device-to-device level. When forming a VCM memory cell, variations in oxygen vacancy density and distribution impacts the formation, location, and number of conductive filaments [104], [115]. As this variation exists device-to-device prior to radiation, differences after radiation will only worsen [92], [104], [115]. If radiation responses vary from device-to-device, this makes comparing the same materials from different sources very challenging. Further factoring in different materials makes a unified theory of VCM radiation effects extremely difficult and is still being actively studied.

Despite this, two dependencies of radiation hardness on VCM cells are well known: 1) circuit set up and 2) oxide thickness [93], [101], [104], [115]–[117]. Thinner devices that are not left floating are thought to be the ideal set up in a radiation environment and can be used to select radiation tolerant designs.

Whilst the mechanisms behind TID effects of VCM memory is still in discussion, VCM memory can be seen as a radiation hard memory where memory property alterations are usually only seen at Mrad dose levels which are much higher than required for space applications [115]. Thin oxide grounded VCM cells are promising for radiation environments, although evident switching of states indicates other types of RRAM may be preferable. This other type is ECM.

For metal-oxide ECM cells, e.g., Cu-doped HfO_2, changes in HRS and V_{set} are reported [91], [93], [95], [107], [118]. Similar to VCM memory, oxygen ions, oxygen vacancies, and charge are induced in the oxide layer of oxide ECM memory. Radiation-induced oxygen vacancies can inhibit formation of metallic filament, resulting in increase in V_{set}, attributed to either scattering of Cu ions or internal field reduction [91], [95], [93], [107]. Induced traps can also reduce HRS [95], [107], [118]. Unlike VCM memory, once a metallic filament is formed, the radiation induced oxygen vacancies have less impact on the filament, resulting in a higher radiation resilience when in LRS [91], [93].

For metal-doped chalcogenide ECM cells, e.g., Ag-doped $Ge_{30}Se_{70}$, a process known as photo doping can occur. Well known in the literature, electron hole generation in chalcogenides can lead to Ag diffusion in the chalcogenide matrix [119]–[121]. Applications such as sensors are made based on this photo-induced effect via thin film exposure to UV radiation [121], [122]. Electron-hole pairs generated by high energy ionizing radiation could also trigger photo-doping effects that then may lead to changes in the resistive state of a metal-doped chalcogenide ECM cell [123], [124].

Despite the photo-doping process, metal chalcogenide cells have shown a high radiation tolerance, although this is dependent upon the fabrication method and composition of the switching layer [97], [98], [124]–[128]. During fabrication, a sufficient UV/thermal doping step prior to radiation will leave the chalcogenide layer fully saturated with Ag, and thus further doping from radiation will not occur [124], [125], [129]. The structure, bonds, and arrangement of chalcogen atoms can also affect the ionic motion of silver, effecting the memory properties [129]. Therefore, differences in composition will result in further variation from radiation.

For the majority of metal chalcogenide ECM cells studied, LRS states are mainly unaffected whilst the pristine and HRS states have exhibited sensitivity to radiation, albeit at high doses [97], [98], [124]–[126]. It is hypothesized that when in the pristine state, nanosized clusters of highly conductive Ag ChG with a less conductive silver-doped ChG layer could occur due to ionizing radiation [117]. In the HRS state, it is thought that radiation induced electron holes activate

Ag surface agglomeration, reducing the Ag concentration in the layer below [98], [117], [125], [127]. Either way, careful selection of a fabrication process and chalcogenide material could possibly reduce these effects, leading to highly radiation tolerant RRAM cells.

In 2015, high radiation tolerance of an un-doped solid electrolyte SiC ECM cell was reported [130]. Unlike a vast number of metal-oxide and chalcogenide ECM memories that report changes to HRS or pristine resistance states [95], [97], [98], [107], [118], [125], [127], [131], the SiC ECM cells showed no changes to any resistance states, nor conduction mechanisms, as seen in Fig. 12. The radiation stability could be attributed to a high diffusion barrier of SiC for Cu, meaning that photo doping from radiation-induced electron-hole pairs is suppressed or it could be attributed to a large band gap, resulting in a lower number of radiation induced carriers. Selecting a nonoxide switching layer also removes any undesired effects caused by radiation induced oxygen vacancies. Further investigations into the radiation effects of other nonchalcogenide solid-state ECM could lead to the identification of a new type of radiation hard resistive memory.

VIII. Conclusion

We have described TID response mechanisms in various CMOS technologies and beyond. Up until the latest Si-based CMOS commercial processes, the thick field oxides play a major role in the TID device characteristics, while for 2-D channel and thin film transistors, the focus shifts to the interplay between semiconductor surface, semiconductor/oxide interface, and bulk oxide charge trapping mechanisms.

Some technologies have shown exceptional hardness against TID radiation. These are the PDSOI MOSFET at the 45- and 35-nm nodes with high levels of body doping, bulk FinFETs of various gate lengths where the leakage paths are formed deep inside the neck region of the fin, GAA FETs where the channel is completely wrapped by the gate as well as NVFETs with single-layer graphene on PZT.

TID hardening solutions have also been proposed for CNT TFTs that include covering the film with a dielectric material to reduce surface adsorption mechanisms, reducing the thickness of the gate dielectric, and using alternative materials such as SiON. Organic-inorganic self-assembled nanodielectrics as gate insulation have also shown to increase radiation hardness of graphene back-gated transistors. This has been attributed to the competing mechanisms of aggregating interface and bulk oxide traps and charges, a process that can be proven useful for UTBB designs.

All RRAM cells, whether VCM and ECM, generally show very high tolerance to TID with negligible or no memory property changes seen until the Mrad regime. Compared to traditional memory or floating gate transistors, which can withstand 10–100 krad, RRAM is a superior radiation hard memory. Specifically, ECM cells show superior radiation hardness to VCM with no state switching seen, whilst solid-state electrolyte ECM cells could provide even more radiation resistant memory cells, with no changes to any memory properties.

It is generally expected that miniaturization will bring many interesting concepts on radiation hardened devices that include and take advantage of the many novel material properties and physical phenomena that arise from their combinations.

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