Towards Industrial Exploitation of THz Frequencies: Integration of SiGe MMICs in Silicon-Micromachined Waveguide Systems

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***Abstract*—A new integration concept for THz systems is presented, wherein patterned silicon-on-insulator wafers form all DC, IF and RF networks in a homogeneous medium, in contrast to existing solutions. Using this concept, silicon-micromachined waveguides are combined with silicon germanium (SiGe) microwave monolithic integrated circuits (MMICs) for the first time. All features of the integration platform lie in the waveguide's H-plane. Heterogeneous integration of SiGe chips is achieved using a novel in-line H-plane transition. As an initial step towards complete systems, we outline the design, fabrication and assembly of back-to-back transition structures, for use at D-band frequencies (110 – 170 GHz). Special focus is given to the industrial compatibility of all components, fabrication and assembly processes, with an eye on the future commercialisation of THz systems. Prototype devices are assembled via two distinct processes, one of which utilises semi-automated die-bonding tools. Positional and orientation tolerances for each process are quantified. An accuracy of $\pm$3.5 µm, $\pm$1.5° is achieved. Measured S-parameters for each device are presented. The insertion loss of a single-ended transition, largely due to MMIC substrate losses, is 4.2 – 5.5 dB, with a bandwidth of 25 GHz (135 – 160 GHz). Return loss is in excess of 5 dB. Measurements confirm the excellent repeatability of the fabrication and assembly processes and thus their suitability for use in high-volume applications. The proposed integration concept is highly scalable, permitting its usage far into the THz frequency spectrum. This work represents the first stage in the shift to highly-compact, low-cost, volume-manufacturable THz waveguide systems.**

***Index Terms*—micromachined waveguide, silicon germanium, terahertz, integrated circuit packaging, MMIC.**

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I. Introduction

THE terahertz (THz) frequency spectrum, lying between 0.3 – 10 THz, is increasingly attractive for low-cost, high-volume applications. Advances in semiconductor technology, integration and packaging techniques make such usage feasible [19]. THz systems find application across a wide range of scenarios, including wireless communication, sensing, imaging and life science [20]. Of these, use of the THz spectrum for fixed wireless communication is among the most promising. Industry forecasts indicate continued growth in this sector [21], [22], whereby new solutions will be required to meet future demand for higher data-rates. Wireless links operating at D-band frequencies (110 – 170 GHz) support spectral efficiencies of up to 10 Gb/s/GHz [23], with practical data-rates of up to 48 Gb/s reported [24], while advancements made above 200 GHz enable data-rates in excess of 100 Gb/s [25]. Spectral allocations by the Federal Communications Commission assign multiple bands between 100 – 300 GHz for such use [26], providing a clear pathway for commercial development. Future commercialisation of the THz spectrum will rely on the development of affordable, scalable circuits and systems to facilitate market growth.

Conventional THz technology is dependent on expensive serial manufacturing and integration techniques, suitable only for high-end scientific instrumentation or one-off prototypes. Previous generations of THz systems relied on thin, volume-limited semiconductor substrates and fabrication techniques [27], [28]. Indium phosphide heterojunction-bipolar- [29] and high-electron-mobility- [30] transistors (HBTs and HEMTs, respectively) provide signal gain up to 1 THz, with complete front-ends and transceivers reported up to 300 GHz [31], [32], [33]. The extreme cost of such technologies massively restricts their range of applications, driving the search for low-cost alternatives, where silicon-based devices are the leading candidate. Silicon Germanium (SiGe) BiCMOS and HBT transistors have undergone continued improvement over the past decade, achieving an f_{max} of up to 720 GHz [34]. Equivalent circuit models indicate a physical f_{max} limit above 2 THz [35], [36]. These devices enable the large-scale realisation of cost-effective, multi-functional monolithic microwave integrated circuits (MMICs) at THz frequencies [37]. Multiple transceivers based on such have

Table I: THz Packaging and Waveguide Technologies

Technology	Ref.	Cost	Feature Size	Tol.	Scalability	λ (W/mK)	Reconfig.[1]	DC/RF Routing	IL (dB/mm) [2]
SU-8	[1], [2]	Low	$<1\,\mu$m	$10\,\mu$m [1] [3]	Medium	0.2 – 0.3 [3]	Hetero.	Hetero.	0.03 – 0.05 [2]
LTCC	[4]	Low	- [4]	0.5 % [5] [5]	Medium	3.3 – 4.6 [5]	Hetero.	Homo.	1.36 [4] [6]
Injection Moulding	[6]	Low	- [7]	- [7]	High	0.1 – 0.5 [7] [8]	Hetero.	Hetero.	- [7]
3D Printing	[8], [9]	Medium	$>10\,\mu$m [9]	$>10\,\mu$m [9]	Low	0.12 – 0.24 [10]	Hetero.	Hetero.	0.018 – 0.02 [8]
CNC Milling	[11], [12]	High	$<10\,\mu$m	2.5 µm [11]	Low	10 – 500 [13] [10]	Hetero.	Hetero.	0.014 – 0.018 [12]
Silicon-micromachining	**This Work**	**Low [11]**	**$<1\,\mu$m**	**$<1\,\mu$m**	**High**	**149 [14]**	**Homo. [15]**	**Homo. [16]**	**0.02 – 0.07 [17]**

[1] Homo.: homogeneous; hetero.: heterogeneous. [2] Measured waveguide insertion loss, 220 – 330 GHz. [3] Mean of values in Table II.
[4] Dependent on method of patterning. [5] Material shrinkage. Additional tolerances dependent on patterning. [6] Mean of values in Fig. 18.
[7] Dependent on master, material, aspect ratio, etc. [18]. [8] Non-filled polymers. [9] Dependent on printer, material, nozzle, etc.
[10] Typical machineable metals/alloys. [11] At high-volume scale.

been demonstrated between 100 – 300 GHz [38], [39], achieving data-rates up to 120 Gb/s. Led by the demands of the digital IC market, scaling of traditional CMOS transistors has also pushed their operation into the THz region [40], [41], [42]. Although individual device performance cannot match their III-V counterparts, CMOS circuits open new usage scenarios due to their affordability and potential complexity [43]. Novel architectures and spatial combining of densely-packed devices, be they CMOS or SiGe, make such technologies highly-suited for use in sensing and imaging [44]. By combining HBTs and CMOS, high-performance THz front-ends with integrated digital circuitry are also possible [45], [46].

Any system incorporating active devices must provide three core capabilities: a suitable packaging environment, a transmission medium for RF interconnection and external connections to supply bias voltages, control signals, etc. Waveguides are the transmission medium of choice in THz systems, as planar transmission lines suffer from prohibitively high losses at such frequencies [17]. Interconnection of ICs to waveguides is achieved using external or integrated coupling structures. External E-plane probes fed by bond-wires [47] require compensation techniques [48] and suffer from poor repeatability above 100 GHz. Flip-chip mounting [49] introduces an additional ground plane which affects any guiding structures in the MMIC, requiring co-design of MMIC and package; an external waveguide coupling structure is also needed. Out-of-plane interconnects [50], [40] are impractical to assemble and require complex multi-layer architectures. Integrated structures, such as a dipole antennas [51] and E-field probes [52] are significantly more compact, without sacrificing performance. E-plane transitions impose constraints on chip size; laser dicing [53] or chemical etching [28], [54] of non-rectangular dies and alternative designs requiring precision machining [55] allow these to be overcome but are not suitable for industrial scale use.

THz waveguides typically use split-block designs, whereby components are split into multiple parts, each fabricated by CNC milling. In a waveguide system, the packaging environment is traditionally formed by the body of the split-blocks, while all other connections are made heterogeneously. The high cost of such components greatly limits the potential applications of THz technology and is regarded as the primary bottleneck preventing its wide-spread adoption [56]. A variety of alternative THz waveguide and packaging technologies exist, as outlined in Table I, which summarises the key performance metrics. For high-volume applications, the chosen technology must be affordable, repeatable and compatible with industrial processes. Although low-cost, LTCC components [4] suffer from large fabrication tolerances and high insertion loss, while the limited ceramic sheet thickness requires stacking of multiple layers. The same is true of SU-8 [1], which can only be accurately applied to a certain thickness. Polymer-based approaches, including SU-8, 3D-printing [8] and injection moulding [6], are inherently hindered by their low thermal conductivity, particularly at THz frequencies, where DC-RF conversion efficiencies are low. Injection moulding can produce low-cost components offering good performance [6] but suffers further from restrictions in aspect ratio and demoulding defects [18]. Feature sizes and tolerance levels are dependent on the initial master, necessitating the use of CNC milling or silicon-micromachining. 3D-printing of metals [9] is hindered by high tolerances and poor feature sizes. The serial nature of such processes, along with CNC milling, prevents scaling to high-volumes. Silicon-micromachining [17] is currently the most appealing alternative, offering high uniformity, small feature sizes, suitable thermal capabilities and outstanding surface roughness [57]. Existing micromachining techniques and infrastructure enable batch production, with billions of silicon-micromachined components in use today. Vertically-stacked silicon-micromachined packages in [58], [59] utilised thin active devices ($\leq 25\,\mu$m), which are both too costly and overly fragile for volume manufacturing.

This work seeks to merge SiGe MMICs with silicon-micromachined waveguides for the first time to realise low-cost, volume-manufacturable THz devices and systems. As a first step towards complete systems, we present a new system integration and packaging concept based on silicon-micromachined components, which allows for the creation of DC, RF and IF networks in a single homogeneous medium. A novel in-line H-plane MMIC to waveguide transition forms the interconnection between the two media. Fabrication and assembly processes compatible with industrial tools and infrastructure are developed. The focus on industrial scale processes and techniques is a move away from the classical approach to waveguide components and systems. Such a shift is necessary to support the foreseen expansion of THz technology and its applications.

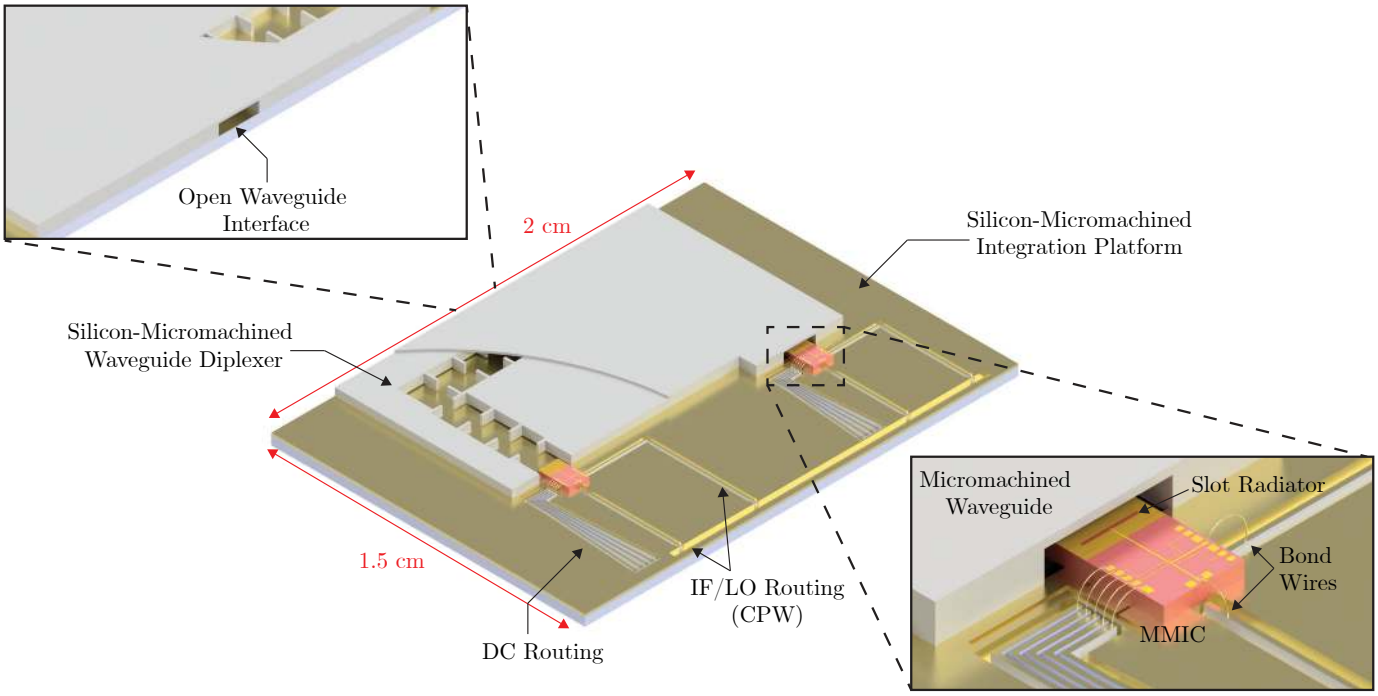


Fig. 1: THz microsystem integration concept. A diplexer front-end incorporating two MMICs and a micromachined waveguide diplexer is shown. The waveguide metallisation is omitted for clarity. Figure 5 shows a cross-sectional view of system.

II. THz Microsystem Concept

The novel approach to THz systems, herein referred to as THz microsystems, is conceptually illustrated in Fig. 1, which shows a fully micromachined waveguide diplexer front-end with integrated MMICs, DC and LO/IF routing. The integration platform consists of two separate silicon-micromachined components, each fabricated in a silicon-on-insulator (SOI) wafer, bonded together to form all necessary biasing, signal routing and waveguide networks. Unlike existing solutions, the package is thus composed of a single homogeneous medium. Heterogeneous interconnection between MMIC and waveguide is provided by an in-line H-plane transition (Section III). This transition permits usage of MMICs of width equal to that of the waveguide, overcoming the limitations of traditional E-plane designs. The non-galvanic nature of the interconnect removes the need for any such connection at RF frequencies. As all features lie in the H-plane of the waveguide, vertical stacking of multiple layers and through-substrate waveguides are eliminated. Insertion of the MMIC is uncomplicated, as the waveguide is open-ended and the system is not enclosed inside a metallic block. Standard bond wires are used to connect all other DC or low-frequency circuitry to the MMICs. The thickness of the SiGe MMIC (180 µm) allows it to be handled by automated assembly tools. All other components are also compatible with such tools. Compatibility with industrial fabrication and assembly processes enables volume production of complete microsystems.

Waveguides remain a key part of many THz systems, despite significant progress in silicon-based system-on-chip (SOC) solutions (Section I). Practical transceiver systems require channel-selection filters with high stop-band rejection. Such filters are only possible in high-Q transmission media, preventing on-chip integration. To this end, THz transceivers often incorporate a separate waveguide filter [60]. The increased free-space path loss at THz frequencies and limited gain of on-chip antennas makes them best suited for short-distance scenarios, where their compactness is of value. On-chip electronic tuning in phased-array systems also allows for beamforming, albeit with limited antenna gain. High-gain antennas are required to overcome the increased path-loss in medium- and long-distance applications, such as wireless backhaul. This requires the use of external waveguide or lens antennas which must be interfaced with the rest of the system.

The proposed integration concept provides the low-loss of waveguide technology along with the compactness of silicon-micromachined components and packaging. The low insertion loss of the double H-plane split micromachined waveguide [17] allows passive components with very high Q [61] to be realized in the package itself. Corporate feed antenna arrays with high gain [62] and other state-of-the-art passive components [63] are also enabled by the low insertion loss. High-aspect-ratio co-planar-waveguide structures [16] can also be implemented, providing low RF and ohmic losses for feeding and biasing networks. Re-configurability through integrated RF MEMS components [15] enables the creation of tunable, compact systems with this approach. The planar nature of the platform allows multiple ICs to be integrated on a single homogeneous carrier in this manner. An open waveguide interface connects the system to an antenna or other waveguide components, further increasing integration. Although initially designed for D-band frequencies (110 – 170 GHz), all micromachined components of the concept are highly scalable, extending its applicability to frequencies bey-

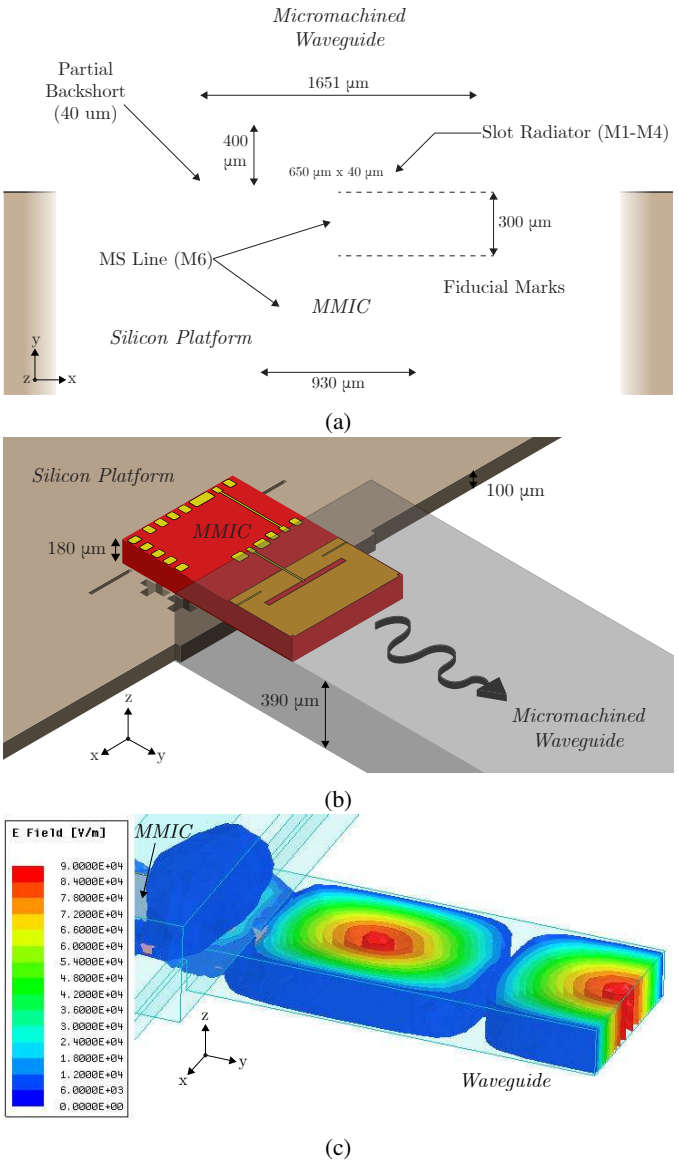


Fig. 2: (a), (b) MMIC to waveguide transition diagram. (c) The transition's simulated E-field distribution.The direction of propagation is y.

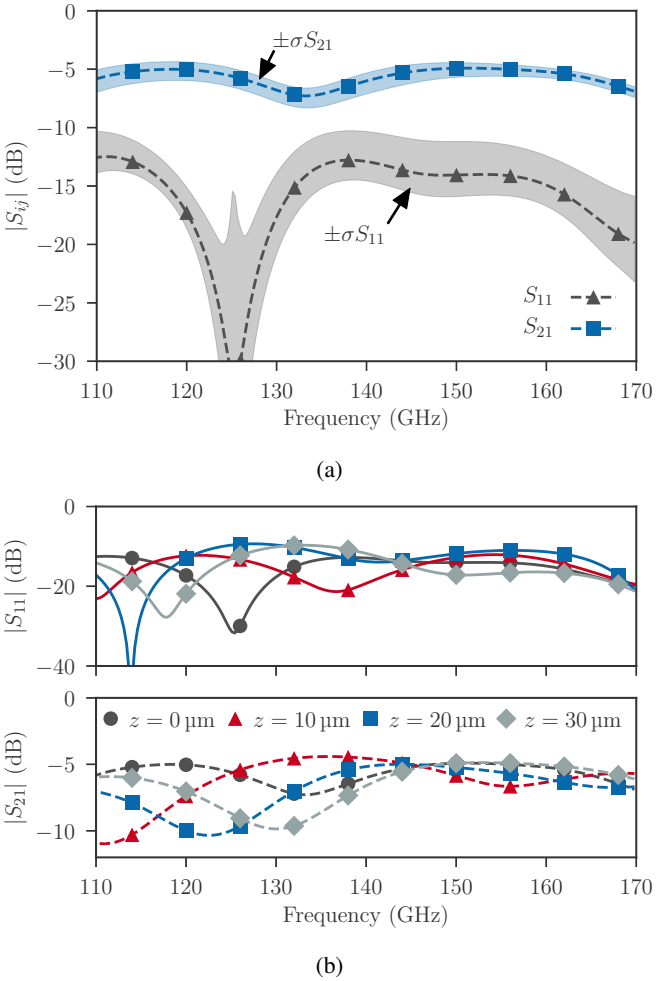


Fig. 3: Simulated S-parameters of the single-ended MMIC to waveguide transition. (a) The nominal S-parameters are indicated by the dashed traces. Shaded areas indicate the standard devation of S_{11}, S_{21} given $\pm 10\,\mu m$ x, y and $\pm 10°$ offsets. (b) Influence of the MMICs position in the z-axis on its performance.

ond 1 THz. Here, we focus on the integration and packaging aspects of the proposed concept. Passive MMIC-waveguide-MMIC structures are implemented to demonstrate the concept and assess its performance.

III. MMIC - Waveguide Transition Design

In silicon-based IC technologies, metal fill-factor design rules prevent the use of classical chip-to-waveguide transitions unless filling structures are used to achieve process compliance. To overcome this issue, we propose a novel in-line MMIC-to-waveguide transition, comprising of an on-chip slot radiator mounted in the waveguide's H-plane, as illustrated in Fig. 2. This allows for metal filling and substrate doping requirements to be adhered to across the entire chip, providing a packaging solution suitable for high-volume IC technologies.

A H-plane transition also allows one to double the width of the MMIC, greatly increasing its potential complexity. H-plane transitions utilising stepped impedance transformations [64] or folded waveguides [65] are precluded due to their complex fabrication and assembly. The transition is realized in a commercial, production-qualified SiGe BiCMOS technology (Infineon BHFC11). It was recently utilised to measure the output power of a D-band transmitter implemented in the same process [66].

The BHFC11 process offers f_t, f_{max} of 250 GHz/400 GHz, a breakdown voltage of BV_{CEO} =1.5 V [37] and six metal layers in its back-end-of-line (BEOL). The metal layers are separated by silicon dioxide ($\varepsilon = 4$) and silicon nitride ($\varepsilon = 6$) intermediate layers of thicknesses up to 2.6 µm. By stacking layers M1-M4 and using M6 (the topmost layer) to form a microstrip line, a slot radiator structure can be implemented, as shown in Fig. 2a. Capacitive coupling of the E-field to the waveguide top and bottom walls transfers energy from

the MMIC to the waveguide. A partial waveguide backshort formed by the silicon platform on which the MMIC is placed reduces undesired back-radiation. The platform also places the slot radiator in the required z-position inside the waveguide. Fig. 2c shows the coupling between MMIC and waveguide. A parametric analysis in Ansys HFSS was performed to optimize the transition, seeking to minimize its insertion loss while achieving maximum bandwidth. The process back-end was represented by a single 6.3 µm thick layer with a permittivity of 4 in all simulations. Substrate conductivity was set to 6.67 S/m, with a thickness of 180 µm. The slot radiator was fed by a 2 µm thick microstrip line on top of the MMIC substrate. This microstrip line was in turn connected to GSG probe pads and a model of the relevant probe tips. A waveguide port was used to excite the required mode in the probe tips. The simulated transition exhibits an average insertion loss of 5.6 dB with return loss greater than 10 dB across the entire D-band (Fig. 3a).

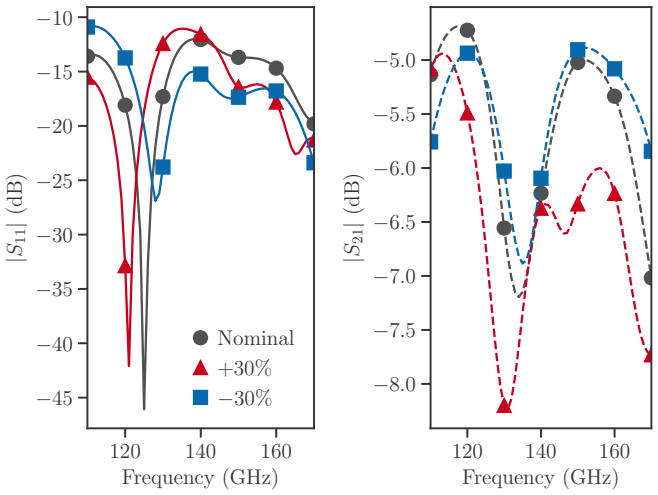
The sensitivity of the transition to positional tolerances was analysed to determine its compatibility with automated assembly procedures. MMIC positional offsets up to ±10 µm in $x-$, $y-$directions and in-plane (xy) rotation up to ±10° were simulated, using 10 evenly distributed samples for each parameter. The combined standard deviation of its insertion loss (±0.02) and return loss (±0.0225) is plotted in Fig. 3a. The transition is largely insensitive to any offset within these ranges. Out-of-plane positional tolerance of 0 – 30 µm in the z-direction was also investigated. The transition is most sensitive to its position in the z-axis, as seen in Fig. 3b. This informed the design and implementation of the semi-automated assembly process, described in Section V-B.

Much of the insertion loss of the transition is due to dielectric loss in the thick silicon substrate, as concluded from a loss analysis (Table II). Simulation of the transition with a lossless substrate reveals that substrate dielectric loss accounts for 1.2 dB of the transition's overall insertion loss. Backwards radiation from the slot antenna, visible in Fig. 2c, contributes an additional 0.8 dB of loss. This value was determined by simulation of the transition with a complete waveguide backshort in place of the partial one. Additional back-radiation occurs in the substrate, the effect of which is included in the substrate's dielectric loss. Ohmic losses in the microstrip feed line (0.7 dB) and CPW pads (0.2 dB) further degrade the transition's performance. The remaining 2.3 dB can be attributed to numerous other factors including mode matching between antenna and waveguide. The effect of loading the waveguide with the lossy MMIC substrate was examined by simulating the nominal transition after a increase/decrease in MMIC width by 30 %. A significant increase in insertion loss occurs when the MMIC is widened (Fig. 4), reaffirming that substrate loss is the primary loss mechanism. Minimal change occurs when the width is reduced. As such, arbitrary chip sizes, up to a point, can be used without drastically altering the transition's performance, providing significant design freedom. The transition's loss could be reduced by incorporating additional structures to block back-radiation from the MMIC (such as a bed-of-nails [67]), using a thinner substrate or, alternatively, a BEOL with increased resistivity. A BEOL permitting through-silicon-vias would allow for an on-chip backshort to be implemented, eliminating energy leakage into the substrate and any excited substrate modes.

Table II: MMIC to Waveguide Transition Loss Analysis

Mechanism	Contribution to overall loss
Reflection Loss	0.5 dB
Substrate Dielectric Loss	1.2 dB
Radiation Loss	0.8 dB
Ohmic Loss (MS line, CPW pad)	0.9 dB
Other [1]	2.3 dB
Total [2]	**5.6 dB**

[1] Mode mismatch in transition, finite ground plane conductivity, etc.
[2] Mean loss across the entire band.



(a) (b)

Fig. 4: Simulated (a) S_{11} and (b) S_{21} of the transition with (1) nominal MMIC width, (2) an increase in width by 30 % and (3) a corresponding decrease by 30 %.

IV. Microsystem Fabrication

A. Fabrication of Micromachined Components

All micromachined components are fabricated following [17], using silicon-on-insulator wafers patterned via deep reactive ion etching (DRIE). The main process steps are illustrated in Fig. 5. Two distinct wafer configurations, Wafer 1 and Wafer 2, are used, providing design flexibility. Both wafers have a 100 µm thick device layer (DL). Wafer 1's buried oxide (BOX) layer is 1 µm thick, while its handle layer (HL) is 350 µm thick. The corresponding values for Wafer 2 are 2 µm and 390 µm, respectively. The DL of Wafer 1 acts as the platform structure required to place the MMIC in the correct z-axis position. Precise control of this parameter is achieved by using low-tolerance SOI wafers (±2 µm). The large "pocket" etch in Wafer 1 accommodates a reciprocal piece from Wafer 2 (Fig. 5c). Fiducial marks for alignment of the MMIC are also etched in this layer. The pocket structure consists of a large open area, in contrast to the fiducial

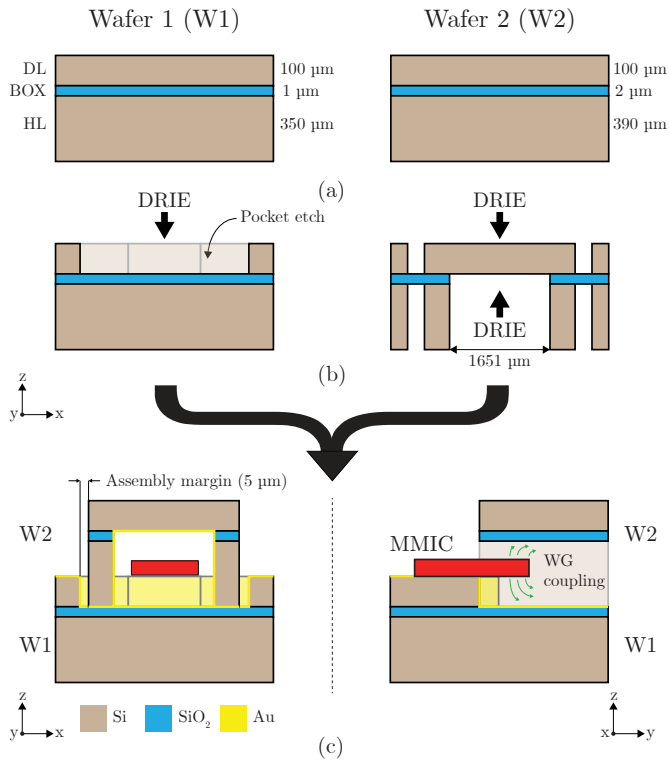
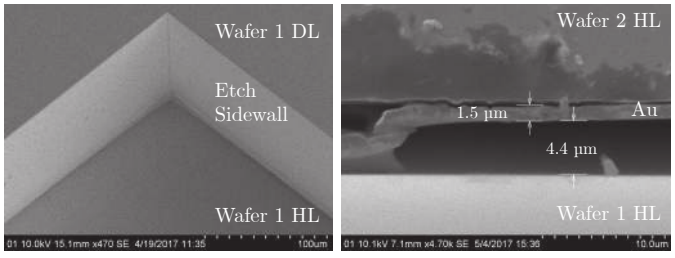


Fig. 5: Fabrication process flow diagram. (a) Layer stack of the SOI wafers, detailing device (DL), buried oxide (BOX) and handle layer (HL) thicknesses. (b) DRIE processing of each wafer (c) Cross-sectional profiles after metallisation and assembly. The direction of propagation is y.



(a) (b)

Fig. 6: SEM images of (a) a corner of the pocket structure in Wafer 1 and (b) delamination occuring post thermo-compression bonding of Wafer 1 to Wafer 2.

marks. Sufficient over-etching certifies that its corners are fully etched (Fig. 6a), allowing for insertion of Wafer 2.
Trenches etched in the HL layer of Wafer 2 form the waveguide sidewalls and roof. Due to its open-ended nature, the waveguide roof acts as a membrane, supported on either side by the HL. Individual components are created by etching from both sides of the wafer (Fig. 5b). Both wafers are coated with 1 µm of gold via sputter deposition prior to assembly.

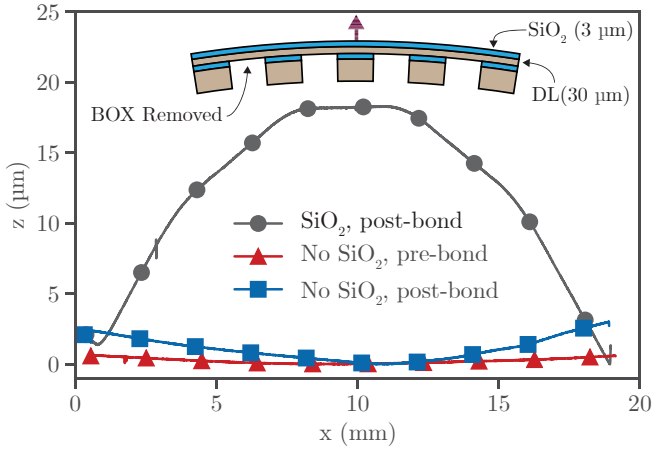


Fig. 7: Measured deflection of Wafer 2 after BOX removal and Au deposition, under the following configurations: (1) SiO_2 mask not removed, post-bonding, (2) SiO_2 mask removed, pre-bonding and (3) SiO_2 mask removed, post-bonding. The inset figure shows the cross-section of the analysed chip (1.9 cm $\times$ 3.8 mm), with the direction of deflection indicated. Four waveguide structures are etched in the chip.

B. Assembly of Micromachined Components

The micromachined components are bonded together using thermo-compression bonding at 200 °C. The pressure applied during bonding must be controlled to avoid damage to the membrane structure in the DL of Wafer 2. Self-alignment by the pocket structure etched in Wafer 1 greatly simplifies assembly. Typical assembly procedures for micromachined components require manual manipulation and precision vernier scales [58], [68]. A 5 µm assembly margin eases insertion of Wafer 2 into the pocket in Wafer 1 (Fig. 5c). Following successful assembly the MMICs must then be placed. Two different procedures for doing so, one manual and one semi-automated, were developed. These are described in detail in Section V. Automated assembly of the micromachined components is also possible: the fiducial marks in each wafer facilitate alignment. This approach was not tested here, however. Fig. 5c provides cross-sectional views of a complete single-ended transition.

C. Delamination of Thermo-Compression Bonded SOI Wafers

Thermally grown oxide hard masks are used to define all features, with thicknesses between 2 – 3 µm. Growth of thick thermal oxide layers creates a large strain in the substrate on which they are grown. Each silicon layer is sandwiched between two oxide layers of differing thickness; one being the SOI's BOX layer, the other an oxide mask. Wafer 2's BOX layer is removed following DRIE (Fig. 5b), creating a force imbalance in its DL due to strain from the oxide mask [14]. This causes the membrane structure to deflect. The magnitude of the deflection is dependent on the thickness of the oxide and that of the layer itself. Residual strain can be released when pressure is applied during bonding, shattering Wafer 2. Bending of Wafer 2 also places strain on

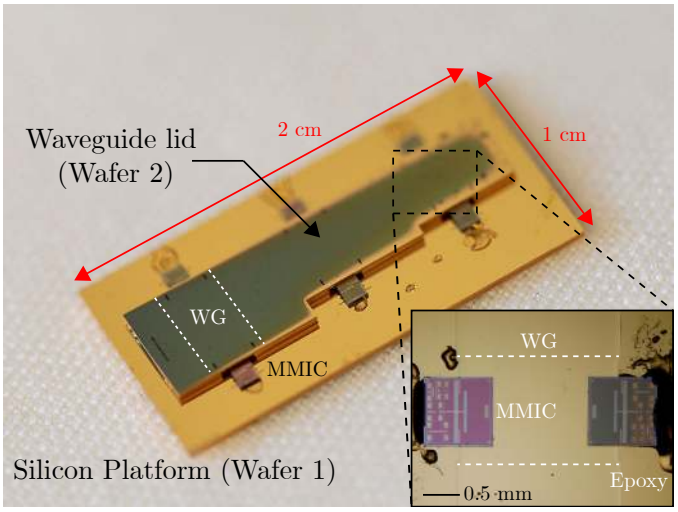


Fig. 8: Photograph of the manually assembled back-to-back prototype module, with a microscopy image of a single waveguide inset. The waveguide lid has been removed for clarity.

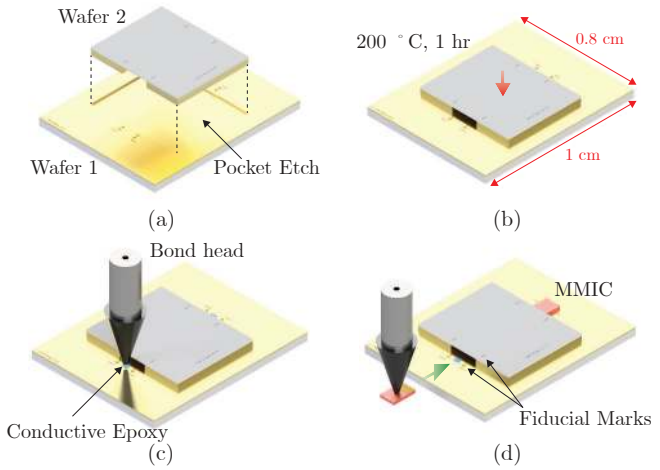


Fig. 9: Semi-automated module assembly process. (a) Wafers 1 and 2 aligned using the pocket structure. (b) Thermo-compression bonding. (c) Conductive epoxy is applied by the bond head. (d) The MMIC is aligned to the fiducial marks and then pressed into the epoxy, where it is held in position during curing.

the bonding interface between the wafers, pulling them apart. If the adhesion strength of this interface is insufficient the two layers will delaminate (Fig. 6b). Electrically, this corresponds to a gap between the side and bottom walls of the waveguide, preventing proper operation.

An initial Wafer 2 DL thickness of 30 µm resulted in large numbers of broken devices. Chips with an area of 1.9 cm × 3.8 mm with four etched waveguide structures deflected by up to 18.5 µm after Au deposition (Fig. 7), as measured via a Veeco Wyko white-light interferometer. Removal of all oxide layers prior to metallisation releases any strain in the wafers, reducing this deflection to a maximum of 0.3 µm. Deflection of 2.8 µm in the opposite direction was recorded post thermo-compression bonding. Enlarging the DL thickness to 100 µm increases the spring constant of the membrane by a factor of $(100/30)^3 = 37$, greatly limiting the possible deflection and eliminating all delamination issues. Both of these solutions were used for the prototype devices presented here.

V. Microsystem Assembly

A. Manual Assembly

For initial proof-of-concept verification, three back-to-back prototype devices were fabricated and assembled, following Section IV. To complete the modules, the required SiGe MMICs were mounted on the device layer of Wafer 1 and secured in place. Positioning of the MMICs was performed manually, using probe needles for manipulation. Alignment was facilitated by the fiducial marks etched into the wafer's surface. Soluble epoxy was used to fixate the MMICs, allowing for removal and re-placement if necessary. Positional accuracy of the order of ±10 µm was achieved. An image of a prototype back-to-back module, containing three back-to-back transitions with a waveguide section in between, is shown in Fig. 8. The RF performance of this module is reported in Section VI.

Table III: Semi-automated MMIC assembly positional/rotational tolerances

MMIC	Δx (µm)	Δy (µm)	Δz (µm)	$\Delta\theta_x$ (°)	$\Delta\theta_y$ (°)	$\Delta\theta_z$ (°)
1	1	1.1	3.5	0.19	0.29	0.28
2	1	2	3.4	0.07	0.08	0.09
3	2	1.8	2.7	0.04	0.13	0.42
4	1.95	2.6	2.95	0.21	0.04	1.53
Mean	**1.49**	**1.88**	**3.14**	**0.13**	**0.14**	**0.58**

B. Semi-Automated Assembly

Following initial verification of the MMIC to waveguide transition, a specialised assembly procedure using semi-automated die bonding tools (Finetech Femto) was developed. The process, illustrated in Fig. 9, begins with alignment and thermo-compression bonding of the micromachined waveguide parts (Section IV-B). A known volume of conductive epoxy (Loctite Ablestik 8177) is then applied to the MMIC's target location by the bond head of a die-bond tool. The MMIC is picked up by the bond head and moved to its nominal position. The z-position of the MMIC during alignment requires careful control; it must be positioned without touching either the epoxy or the waveguide. Alignment to the fiducial marks etched in wafers 1 and 2 is achieved using computer vision software. Once aligned, the MMIC is pressed into the epoxy. The die-bonder holds the MMIC in its target position during temperature ramping and curing of the epoxy, prohibiting movement due to shrinkage. This process is repeated until the module is complete.

Application of a known, repeatable volume of epoxy is crucial, as it affects the z-position of the MMIC. This parameter has a large influence on the MMIC-waveguide transition, as Fig. 3b highlights. Its tolerance must be tightly controlled to

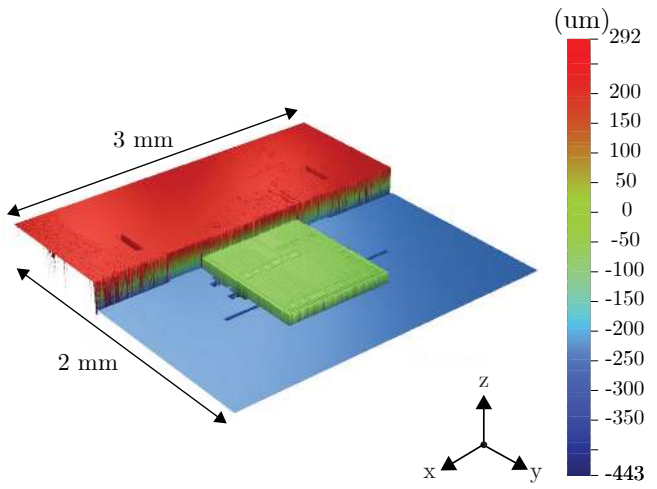


Fig. 10: White-light interferometry scan of MMIC 2, following semi-automated assembly. Positional tolerances for each MMIC are listed in Table III.

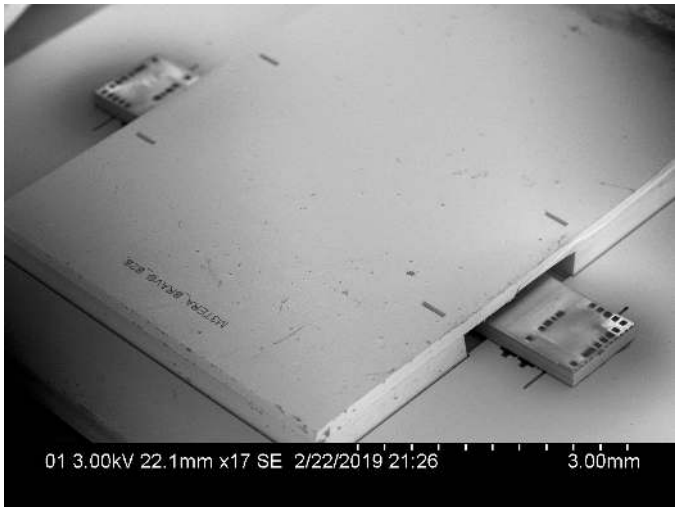


Fig. 11: SEM image of a single back-to-back device.

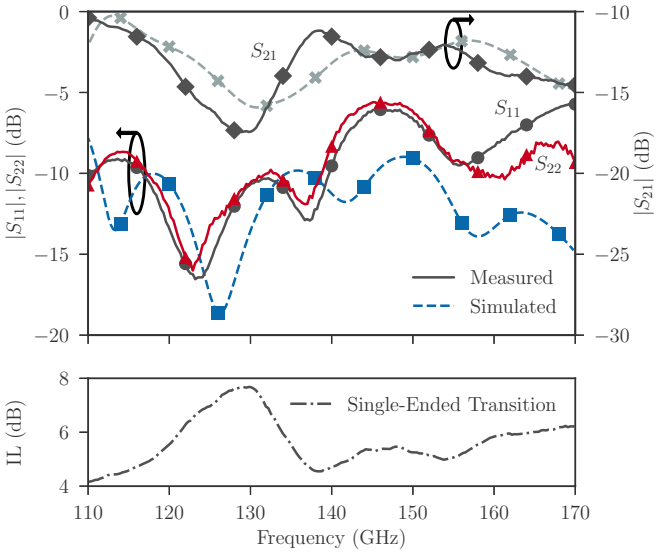


Fig. 12: Comparison of simulation and measurement results for a single back-to-back module, with a waveguide length of L1 = 3.4 mm. The estimated insertion loss of a single-ended transition is shown in the lower figure.

ensure repeatability; epoxy thickness tolerance of 1 µm was achieved. A target height of 10 µm above the Wafer 1's DL was used throughout. Wetting of the epoxy occurs due to the heat applied by the bond head. The applied volume of epoxy must cover the MMIC's bottom surface while avoiding epoxy wetting inside the waveguide itself. Suitable volumes were ascertained through a series of preliminary experiments.

A further two back-to-back devices were assembled using this procedure. Their measured S-parameters are detailed in Section VI. To determine the accuracy and repeatability of the assembly process, the final position of each MMIC was analysed using a white-light interferometry. This information is tabulated in Table III. All four MMICs were within ± 3.5 µm and $\pm 1.5°$ of their nominal position and orientation, respectively. Thermal expansion during epoxy curing causes the z-position of the bond head to drift from its initial position, resulting in a slightly greater z-axis tolerance than the 1 µm achieved upon initial epoxy deposition. Three-dimensional scans (Fig. 10) reveal the flatness of the MMIC relative to the waveguide. An SEM image of a single back-to-back device assembled using this procedure is shown in Fig. 11.

VI. RF Characterization

The RF performance of the proposed MMIC-waveguide transition was determined using standard S-parameter measurements. Initial verification was performed on the manually assembled module (Section V-A), containing back-to-back structures with waveguides of three different lengths (L1 = 3.4 mm, L2 = 3.9 mm, L3 = 4.9 mm). CPW probes (Cascade Infinity) were used to feed the microstrip line in layer M6 of the MMIC. Calibration was performed at the probe tips using a commercial calibration substrate (GGB CS-15 SOLT). The measured S-parameters of a single L1 device are plotted in Fig. 12. The insertion loss of the back-to-back structure is between 10 – 16 dB. Its 3 dB bandwidth is 25 GHz (17 %, 135 – 160 GHz), centred at 148 GHz, with an in-band ripple of 1 dB. Return loss at both ports is very similar and is 5 dB or greater across the band. Given that the insertion loss of the micromachined waveguide at D-band is between 0.008 – 0.016 dB/mm [61], its contribution to the total insertion loss is negligible. The 300 µm long microstrip feed line has a measured insertion loss of 2 – 3 dB/mm, while the CPW probe pads add an additional 0.2 dB loss. As such, the insertion loss per transition in the passband is approximately 4.2 – 5.5 dB, as plotted in Fig. 12. The measured device exhibits a frequency downshift as compared to simulations (Fig. 12). This discrepancy may be due to inaccuracy in the simulation model (Section III) or the sidewall angle of the micromachined waveguide. The spike in both return and insertion loss at 125 GHz is likely due to the presence of substrate modes in the MMIC. Additional simulations showed

Table IV: Packaged Silicon-Based IC to Waveguide Transitions

Ref.	Freq. (GHz)	Topology	Min. IL (dB)	Min. RL (dB)	Δf_{3dB} (%)
[4]	300	Vertical, backshort	4	5	13
[50]	110 – 170	Vertical, DRW	3.4	5	26
[69]	400	Vertical, patch antenna	5	10	10
[70]	110 – 170	Bond-wire	2.2	10	40
This Work	**110 – 170**	**H-plane, slot antenna**	**4.2**	**5**	**17**

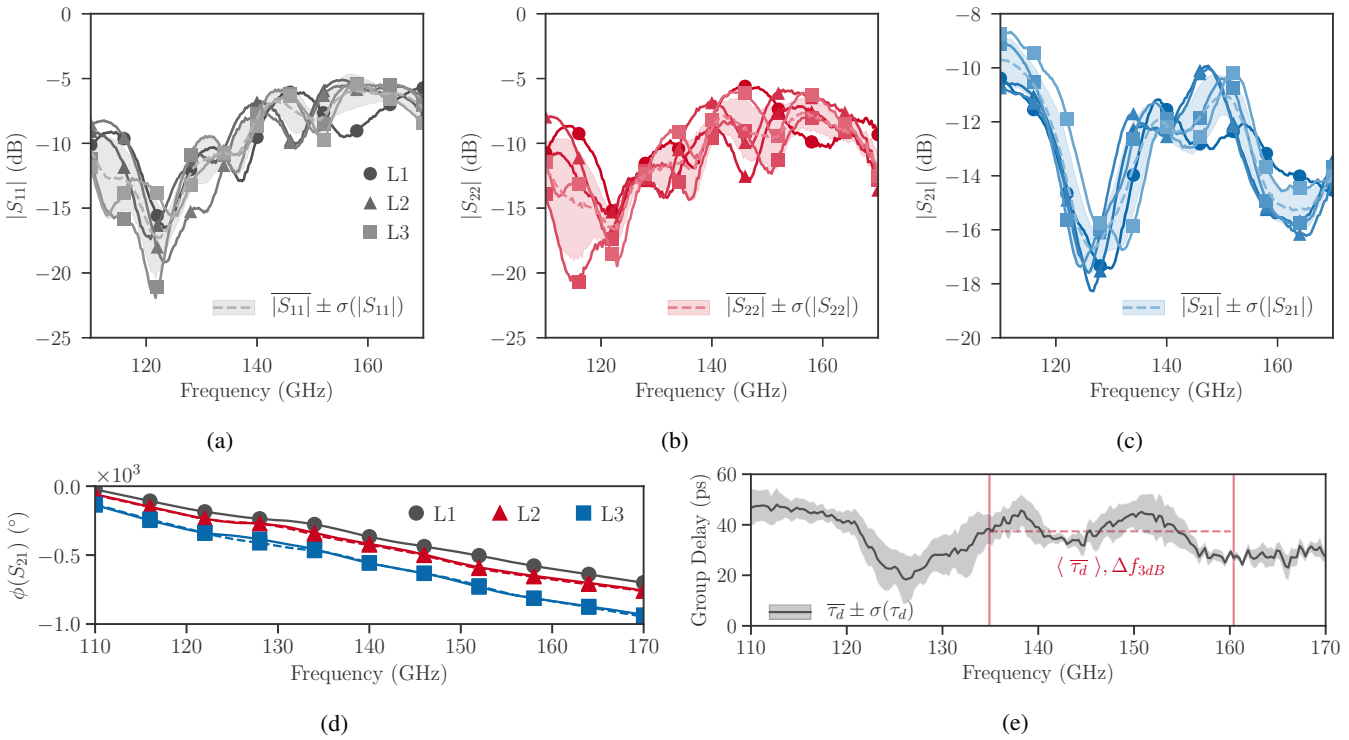


Fig. 13: Measured S-parameters of five different back-to-back modules of varying length (L1 = 3.4 mm, L2 = 3.9 mm, L3 = 4.9 mm), assembled using both the manual and semi-automatic assembly procedures. (a) S_{11}, (b) S_{22} and (c) S_{21}. Each unique device is represented by a single trace. The standard deviation of the measurement results is indicated by the shaded area. The mean is indicated by the dashed traces. (d) Measured phase response of the five modules and (e) their mean group delay. The average passband group delay is represented by the dashed line.

that this behaviour is independent of waveguide length but is suppressed following a reduction in MMIC length. The performance of the transition is benchmarked against other relevant transitions for use in packaging of silicon-based circuits in Table IV.

All five back-to-back devices, with waveguides of varying lengths, were characterised in this manner, allowing their sensitivity to fabrication and assembly tolerances to be analysed. The collated measurement results are plotted in Fig. 13. No correlation between the insertion loss and the waveguide length was found. As the devices were co-fabricated, any variance in their performance can be attributed to the MMIC, assembly process and probe position. The difference in electrical length between L1-L3 is visible from the measured phase response, which is largely linear across the entire band (Fig. 13d). For communication applications, the resulting group delay is also of interest. The mean group delay for all five samples $\overline{\tau_d}$, plotted in Fig. 13e, has a passband ripple of 20 ps. The low standard deviation of the S-parameters, plotted in Fig. 13, indicates that the fabrication and assembly processes developed here are highly repeatable and thus suitable for industrial scale applications.

VII. Conclusion

This paper presented a new concept for the integration of industrial-grade SiGe MMICs with silicon-micromachined waveguide components, herein referred to as THz microsystems. All components of the THz microsystem concept are compatible with existing industrial tools and automated manufacturing processes, enabling future commercialisation of such systems. Two SOI wafers are bonded together to form the micromachined waveguide, all other electrical networks and the mechanical integration platform, providing a complete packaging solution for THz systems. A novel MMIC to waveguide transition suitable for commercial silicon IC processes

was implemented, using a slot radiator mounted in the H-plane of the waveguide. The transition is the first in-line H-plane MMIC to waveguide transition reported to date. Its measured insertion loss is 4.2 – 5.5 dB between 135 – 160 GHz, while its return loss is greater than 5 dB. Specialised assembly procedures were developed to permit semi-automatic assembly of complete THz microsystem modules. These procedures utilise industrial die-bond tools to accurately place the MMIC in its required position and eliminate the need for manual handling. Assembled devices show excellent repeatability, with all MMICs within $\pm 3.5\,\mu$m, $\pm 1.5°$of their nominal position and orientation. As such, the proposed transition and assembly procedure are suitable for large-scale industrial use. The repeatable RF performance of prototype devices re-affirms the suitability of this approach.

While initially demonstrated here at D-band, the proposed concept is well suited for scaling to higher frequencies. As the dimensions of the micromachined waveguide decrease a corresponding reduction in MMIC volume is expected. However, although the waveguide width is constrained, waveguide height can be freely scaled up to twice its nominal value (avoiding TE_{01} excitation), providing additional volume for MMIC integration. Substrate thinning of the corresponding MMIC may reduce the transition's insertion loss while also facilitating integration. If large MMICs are to be integrated they may extend beyond the bounds of the waveguide. Additional structures, such as substrate vias or PMCs, could be used to create artifical waveguide walls/backshorts (c.f. Section III), preventing signal leakage. The reduction in lateral and transverse dimensions at higher frequencies will simplify fabrication of the micromachined components.

The use of standard bond-wire interconnects to feed IF and LO signals to the MMIC (Fig. 1) restricting the potential transceiver architectures and frequency schemes suitable for use with this concept. In [66], the authors demonstrate a complete D-band transmitter based on the proposed integration scheme, which utilises IF/LO frequencies of 6 and 21 GHz, respectively, far below the cut-off frequency of bond-wire interconnects, which have been demonstrated above 100 GHz [48]. IF frequencies above the cut-off of the bond-wires should be avoided. The use of moderate IF and LO frequencies eases the requirements of both the baseband and oscillator hardware, which is valuable in systems applications. On-chip frequency multipliers, such as the sextupler in [66], permit the use of relatively low LO frequencies. Frequency multipliers with larger multiplication factors may be necessary when upscaling the proposed approach beyond 300 GHz. This may require MMICs of increased complexity and size and may also limit the phase noise performance of the packaged components. Alternatively, higher frequency LO signals generated on a separate MMIC could then be fed to the main transceiver MMIC via the transition proposed here.

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