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Toward Nanowire Electronics

Joerg Appenzeller, *Senior Member, IEEE*, Joachim Knoch, Mikael T. Björk,
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(Invited Paper)

Abstract—**This paper discusses the electronic transport properties of nanowire field-effect transistors (NW-FETs). Four different device concepts are studied in detail: Schottky-barrier NW-FETs with metallic source and drain contacts, conventional-type NW-FETs with doped NW segments as source and drain electrodes, and, finally, two new concepts that enable steep turn-on characteristics, namely, NW impact ionization FETs and tunnel NW-FETs. As it turns out, NW-FETs are, to a large extent, determined by the device geometry, the dimensionality of the electronic transport, and the way of making contacts to the NW. Analytical as well as simulation results are compared with experimental data to explain the various factors impacting the electronic transport in NW-FETs.**

Index Terms—**Impact ionization, MOSFET, nanowire FET, nanowire growth, Schottky-barrier, steep slope transistors, tunnel FET, VLS growth.**

I. INTRODUCTION

THE FIELD of nanoelectronics has seen an enormous increase in popularity over the last ten years or so. Material scientists, as well as physicists, chemists, and engineers, are equally curious to explore the potential of various nanomaterials in terms of their fundamental properties and possible applications. A subgroup of researchers is focusing on the usefulness of these novel materials for future nanoelectronics. Because of their intrinsic smallness, a natural choice seems to be employing nanomaterials for high-performance logic applications that have been striving since decades based on continuous scaling of critical dimensions. With channel lengths of transistors in the nanometer regime, replacing the active component of a field-effect transistor (FET) device by a semiconducting nanomaterial occurs to be a logic choice [1]–[10].

However, taking a closer look at the scaling of transistors, it is more than just the intrinsic smallness of the gated channel region that matters. Indeed, an unimpeded current flow from the source terminal to the drain for high on-currents has to be combined with excellent gate control to enable fast switching and low off-currents. It is this combination of requirements that immediately limits the number of suitable nanomaterials for device applications.

A 1-D (or quasi-1-D) semiconductor offers the right mix of properties for a high-performance FET [11]. In terms of electrostatic integrity of the device, a small channel defined by the body of the semiconductor, i.e., the diameter of a nanotube or nanowire (NW), prevents electrons and holes from "escaping" the gate control [12], [13]. Since a transistor with the desired type of device characteristics is defined by electrostatic conditions that ensure that the gate potential rather than the drain potential controls the charge state inside the device channel of length L, a tight gate control is critical. The important—yet often ignored—argument is that the close vicinity of the gate to the channel that is enabled by the small NW diameter is the key to allow for the desired channel length reduction. Note, that scaling of L can be accomplished without the introduction of dopants. This is a further advantage of NW structures since the introduction of dopants into a small region is unavoidably random but, due to the small cross section of the channel region, results in a discrete doping distribution that impacts the device current. Individual devices show a characteristic "fingerprint," if a small number of individual dopants are present in the channel. Ultimately, it is the earlier discussed reduction of channel length without the necessity of doping that improves the device characteristics.

It is worth reflecting about how far the dimensionality impacts the aforementioned statement. Indeed, even a 2-D system consisting of a thin semiconducting channel between the electrodes would allow for more aggressive scaling of the transistor channel than a bulk-type device layout. As will be discussed later, the characteristic screening lengths λ's in 1-D and 2-D systems are not too different (typically, they differ by a factor of 4–5) if the body thickness is comparable. The comparison between λ and L allows deciding whether the device is still effectively in the long-channel regime (the gate control is still dominant) or whether short-channel effects (SCEs) dominate. This means that the minimum achievable channel length L would not be vastly different in 1-D and 2-D.

The dimensionality, however, does become critical if we look into the details of the gate potential impact on the band movement inside the channel region and when it comes to scattering inside the semiconductor [14]. As will be discussed in detail in succeeding discussions, the quantum capacitance C_q

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and associated density of states (DOS) are important for these arguments [14], [16]. The small and with energy-decreasing 1-D DOS $D_{1D}(E)$ allows reaching the quantum capacitance limit (QCL) for realistic gate capacitances C_{ox}, as will be discussed later. The same, however, is not true for 2-D and 3-D systems making a 1-D semiconductor particularly relevant for nanoelectronics applications [17].

Last, it is important to put the term "quasi-1-D," in the right prospective. NWs with diameters between 10 and 50 nm are frequently employed for device applications [10], [18]. Depending on the effective mass associated with the chosen semiconductor and whether electrons or holes are considered, a few to several tens of 1-D modes are involved in current transport [19]. The discussion about 1-D transistor action hereinafter has to be viewed in this context. Populating one 1-D mode after the other, e.g., by means of varying the gate voltage, impacts the band movement and can ultimately result in a situation that has to be captured by a 2-D or 3-D description. However, for an energetic spacing between modes larger than k_BT, the discreteness of those 1-D levels still impacts the device performance and a superposition of 1-D modes occurs to be the appropriate way of capturing the transistor action. With the current trend of growing ever smaller NWs, the following sections are believed to describe the essentials of what already now characterizes state-of-the-art NW devices and even more so capture the device physics of future NW-based devices with more aggressively scaled body thicknesses.

Among the potential semiconducting nanostructures, silicon NWs (SiNWs) seem particularly attractive since they can, in principle, be incorporated into existing processing flows and can be grown epitaxially at predefined locations [20], [21]. A large portion of this paper therefore deals with transistor devices based on SiNWs. However, it should be emphasized here that most of the concepts discussed and conclusions drawn equally hold for other semiconducting nanostructures as well.

The aim of this paper is to explore the potential of NW-FETs from a device point of view and to study and explain the electronic transport phenomena involved. It is therefore organized as follows: After a brief introduction into some basic device concepts, we present details on how to model and simulate NW-FETs, followed by experimental results on the growth of SiNWs. Subsequently, Schottky-barrier (SB) and conventional NW-FETs are discussed. Finally, we introduce two "steep slope," NW-FETs: a vertical NW impact ionization (II) FET and a tunnel NW-FET (T-NW-FET) where switching occurs via field-controlled band-to-band tunneling (BTBT). We show experimental as well as simulation results of the electrical behavior of all four transistor concepts and discuss device physics aspects with respect to the application of these NW-FETs for future nanoelectronics.

Major conclusions of this paper can be summarized as follows.

1) Contacts dominate the electrical behavior of SB and even conventional SiNW-FETs. Experiments show that one cannot regard such devices as a series of simple resistors, and as a result, intrinsic NW properties from FET devices cannot be extracted easily.
2) Vertical NW II FETs show extremely steep turn-on characteristics and enable an efficient suppression of hot electron degradation.
3) SiNWs with *in situ* doped n-i-p structure can be grown with the vapor–liquid–solid (VLS) technique, and T-NW-FETs based on such structures are demonstrated.
4) Scaling down the NW diameter potentially enables T-NW-FETs with inverse subthreshold slopes steeper than 60 mV/dec.
5) Device operation in the QCL, where the potential distribution in the channel is determined by the gate potential and not the channel charge anymore, is desirable. Particularly for tunnel FETs, we show that BTBT does not deteriorate the ON-state performance (as measured by the gate delay) if the device is scaled toward the QCL.

As a result, NWs with thin diameter are a premier choice for future nanoelectronics applications since they do not only enable a continuation of scaling due to the improved electrostatics but also provide additional benefits for alternative device concepts that are not accessible with today's planar technology.

II. SCALING, SCEs, AND WHY NWs

A proper FET should exhibit low off-currents as well as a high ON-state performance. Insights into the FET performance can be obtained by describing the electrostatics of ultrathin-body devices such as NW-FETs by a surface potential method which captures all relevant aspects related to the scaling of the gate oxide thickness d_{ox}, the body thickness (i.e., NW diameter) d_{nw}, and, of course, the appearance of SCEs in laterally scaled devices. The approach leads to a 1-D Poisson equation for the potential at the channel–dielectric interface $\Phi_f(x)$ [12], [22], [23] given by

$$\frac{d^2\Phi_f(x)}{dx^2} - \frac{\Phi_f(x) - \Phi_g - \Phi_{\mathrm{bi}}}{\lambda^2} = -\frac{q(\rho \pm N)}{\varepsilon_0 \varepsilon_{\mathrm{nw}}}. \qquad (1)$$

Here, Φ_g and Φ_{bi} are the gate and the built-in potentials, respectively. Furthermore, ρ is the density of mobile carriers, and N is a constant charge background due to a doping of the NW with either donors ("+" sign) or acceptors ("−" sign). For constant charge density, (1) can be solved analytically, leading to a solution of the form $\Phi_f(x) \propto \exp(-x/\lambda)$ showing that λ is the relevant length scale for potential variations. This screening length λ is a function of d_{nw} as well as d_{ox} and reflects the device geometry under consideration. For a wrap-gate device structure as shown in the top part of Fig. 2, it is given by $\lambda = \sqrt{\varepsilon_{\mathrm{nw}} d_{\mathrm{nw}}^2 \ln(1 + 2d_{\mathrm{ox}}/d_{\mathrm{nw}})/8\varepsilon_{\mathrm{ox}}}$ [12], where $\varepsilon_{\mathrm{nw,ox}}$ are the relative dielectric constants of the NW and the gate oxide.[1]

In the case of a device with a large-area back gate as shown in Fig. 1, we found by comparison with experiment that the screening length is rather of the form $\lambda = \sqrt{(\varepsilon_{\mathrm{nw}}/\varepsilon_{\mathrm{ox}}) d_{\mathrm{nw}} d_{\mathrm{ox}}}$, which was originally derived for a planar-gate planar-channel geometry such as a single-gated MOSFET on silicon on insulator (SOI) [23]. The present approach based on (1) has been

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[1] Note that the difference between the expression for λ used here and in [12] is due to the fact that, in the present case, (1) is derived for the surface potential at the gate insulator–nanowire interface, whereas in [12], the potential in the center of the circular channel is calculated.

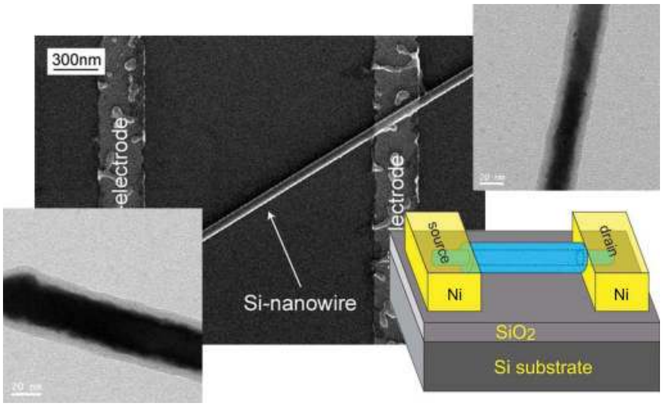

Fig. 1. Scanning electron micrograph of the finished device as well as transmission electron micrographs of SiNW with gate dielectric (SiO_2). The schematic of the device layout is shown in the lower right corner.

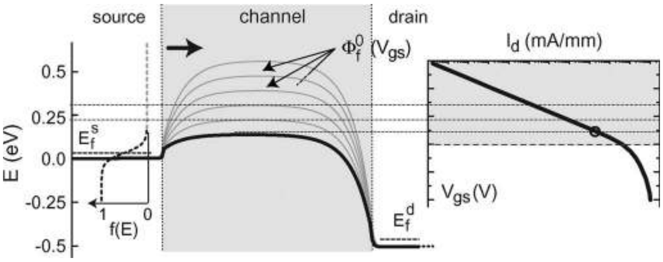

Fig. 2. (Top) Illustration of the device geometry under consideration. Bottom left shows the conduction band along current transport direction, and at the bottom right, a cut along the r-direction is displayed. Vertical quantization leads to a discrete number of subbands E_i contributing to the current.

successfully applied to a variety of fully depleted FETs such as SOI MOSFETs, NWs, and nanotube transistors [24], [25].

It has been noted that the electrical behavior of FETs is determined by the potential maximum in the channel—called Φ_f^0 in the following—that mediates the injection of carriers from the source into the channel [26] (see bottom left of Fig. 2). Solving (1), Φ_f^0 can be obtained as a function of the terminal voltages. For instance, in the device's OFF state, an analytical expression can be found if the channel length L is larger than λ, yielding $\Phi_f^0 \approx 2\sqrt{-(\Phi_{\rm bi} + \Phi_g)(\Phi_d - (\Phi_{\rm bi} + \Phi_g))}\exp(-L/2\lambda) + \Phi_g + \Phi_{\rm bi}$, where $\Phi_d = -qV_{\rm ds}$ is the drain potential [23]. For ideal MOSFET (OFF-state) performance, Φ_f^0 should not depend on Φ_d which is attained if $L \gg \lambda$; since then, the first term in the aforementioned expression can be neglected. In this case, $\Phi_f^0 = \Phi_g + \Phi_{\rm bi}$ implying that $\delta\Phi_f^0 = \delta\Phi_g$ or $\partial\Phi_f^0/\partial\Phi_g \approx 1$. As a result, the surface potential maximum that determines the injection of carriers can be moved one-to-one by the gate voltage, yielding ideal turn-off characteristics with an inverse subthreshold slope of $S = \ln(10)((\partial I_d/\partial V_{\rm gs})(1/I_d))^{-1} = k_BT/q \cdot \ln(10) \approx 60$ mV/dec at room temperature, where q is the electron charge. In other words, when the gate moves the conduction band and therefore Φ_f^0 downward, a larger fraction of the exponential tail of the source Fermi function can contribute to the current, giving rise to the exponential increase of the current in the device's OFF state; this scenario is schematically shown in Fig. 3. At room temperature, the steepest possible S is therefore 60 mV/dec, which is true for *any* FET that relies on the injection of carriers from a thermally broadened Fermi distribution function.

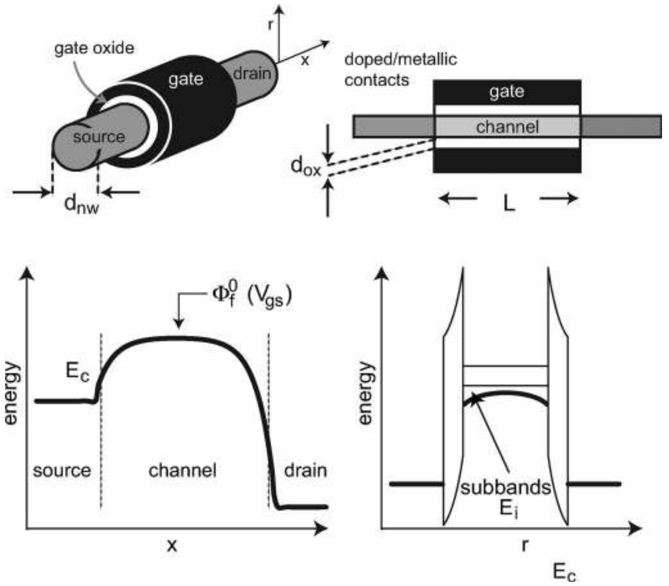

Fig. 3. (Left) Conduction band profile along current transport direction for various $V_{\rm gs}$'s in a conventional FET. (Right) Transfer characteristic showing an exponential increase of current in the device's OFF state.

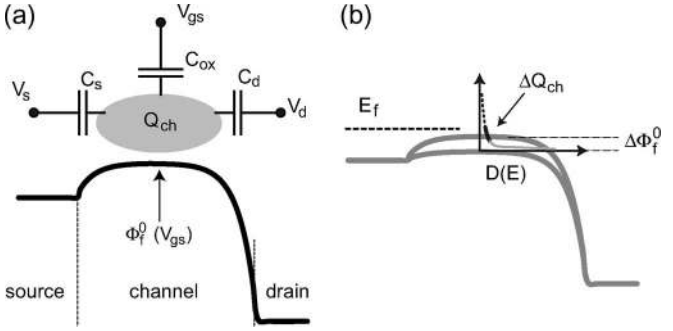

Fig. 4. (a) Conduction band profile along the current transport direction displaying the potential maximum Φ_f^0. The top part shows the relevant capacitances in a MOSFET. (b) Conduction band profile for two different $V_{\rm gs}$'s with 1-D DOS.

Furthermore, in the case $L \gg \lambda$, Φ_f^0 becomes independent of the drain potential, i.e., $\partial\Phi_f^0/\partial\Phi_d \approx 0$. Since Φ_f^0 is the potential barrier that mediates the current flow, drain-induced barrier lowering is efficiently suppressed. In order to avoid the appearance of SCE when scaling down the channel length, λ has to be scaled accordingly in order to maintain the relation $L \gg \lambda$, which essentially means that both the gate oxide thickness and the channel layer thickness (NW diameter) have to be scaled down. In this respect, one of the major benefits of NWs is their cylindrical shape with a scalable diameter into a few nanometer range, making them ideally suited for ultimately scaled FET devices.

A. *Quantum Capacitance*

A MOSFET can be regarded as a combination of different capacitors as shown in Fig. 4(a). The total charge $Q_{\rm tot}$ in the channel is $-\Phi_f^0/q \cdot (C_{\rm ox} + C_s + C_d)$, where $C_{s,d}$ are the source/drain capacitances and C_{ox} is the geometrical oxide capacitance.[2] At the same time, Q_{tot} is determined by the terminal voltages, i.e., $Q_{\mathrm{tot}} = C_{\mathrm{ox}} V_{\mathrm{gs}} + C_s V_s + C_d V_d + Q_{\mathrm{ch}}$, where Q_{ch} is the mobile charge injected by the contacts into the channel. Then, differentiating Φ_f^0 with respect to Φ_g and Φ_d and noting that $q \partial Q_{\mathrm{ch}} / \partial \Phi_f^0 = C_q$, one obtains (in the following, we neglect C_s for simplicity)

$$\delta \Phi_f^0 = \frac{C_{\mathrm{ox}}}{C_{\mathrm{ox}} + C_d + C_q} \delta \Phi_g + \frac{C_d}{C_{\mathrm{ox}} + C_d + C_q} \delta \Phi_d \qquad (2)$$

where C_q is the so-called inversion layer or quantum capacitance [14]–[16], [27]. In order to suppress SCEs, we required $\partial \Phi_f^0 / \partial \Phi_g \approx 1$ and $\partial \Phi_f^0 / \partial \Phi_d \approx 0$. From (2), it is then obvious that this is fulfilled if $C_{\mathrm{ox}} \gg C_d$ and $C_{\mathrm{ox}} \gg C_q$ in the device's OFF state. In a device with $L \gg \lambda$, indeed, $C_{\mathrm{ox}} \gg C_d$ is the case. The second requirement, however, needs more consideration.

In an electrostatically well-behaved fully depleted device, such as an NW-FET, the total gate capacitance is given by $C_g = C_{\mathrm{ox}} C_q / (C_{\mathrm{ox}} + C_q)$, where C_q is again the quantum capacitance introduced earlier. On the other hand, $C_g = \partial Q_{\mathrm{ch}} / \partial V_{\mathrm{gs}} = q \cdot \partial Q_{\mathrm{ch}} / \partial \Phi_f^0 \cdot \partial \Phi_f^0 / \partial \Phi_g$. The second term of this expression can be identified by comparison with (2) to be $C_{\mathrm{ox}} / (C_{\mathrm{ox}} + C_q)$. As already mentioned previously, this means that $q \partial Q_{\mathrm{ch}} / \partial \Phi_f^0 = C_q$, i.e., the quantum capacitance is the change of the channel charge with changing surface potential. In equilibrium (i.e., in a MOS capacitor), the channel charge is given by the DOS $D(E)$ and the Fermi function, and one obtains for C_q

$$C_q = q \frac{\partial Q_{\mathrm{ch}}}{\partial \Phi_f^0} \propto -q^2 \int dE\, D(E) \frac{\partial f_s \left(E - E_f^s \right)}{\partial E} \qquad (3)$$

where E_f^s is the source Fermi level; note that a change of variables leads to the expression on the right-hand side. This integral vanishes in the device's OFF state, and hence, $C_{\mathrm{ox}} \gg C_q$ as required earlier. However, in the ON state of the transistor, one obtains, from (3), $C_q \approx q^2 D(E_f^s - \Phi_f^0)$ meaning that the quantum capacitance is proportional to the DOS within the channel [14], [16], [27]. In a conventional bulk-silicon MOSFET, the DOS approaches the 3-D limit. As a result, the DOS and hence C_q increase with increasing V_{gs}, leading to $C_{\mathrm{ox}} < C_q$, and consequently, the movement of Φ_f^0 with changing V_{gs} tends to zero. In other words, $\partial \Phi_f^0 / \partial \Phi_g \to 0$, as is well known from a conventional bulk MOSFET [28].

This situation can be very different in a FET based on an NW. If the diameter of the NW d_{nw} is sufficiently small, vertical quantization results in a substantial energetic separation of succeeding subbands as shown in the bottom right part of Fig. 2. If the subband separation becomes significantly larger than $k_B T$, the electronic transport in the NW will be 1-D. In 1-D, the DOS is proportional to $1/\sqrt{E - \Phi_f^0}$ such that the so-called QCL can be reached where $C_q^{\mathrm{1D}} < C_{\mathrm{ox}}$ [as shown in Fig. 4(b)]. Here, we want to point out that the QCL can, in principle, also be attained in a 2-D system since the DOS is constant. However, for realistic gate oxide thicknesses, this would require a channel material with a very small effective mass implying a low DOS. For instance, in a planar InAs FET, $C_{\mathrm{ox}} = C_q$ occurs at a gate oxide thickness of approximately 2 nm. Reaching the QCL requires much smaller d_{ox}, which would be technologically challenging. In contrast, in a 1-D InAs NW-FET with a diameter of 10 nm, for instance, $C_{\mathrm{ox}} = C_q$ occurs already at gate oxide thicknesses one order of magnitude larger.[3] This shows that the QCL in 1-D systems is reached much more likely and at technologically feasible device dimensions. In the QCL, the gate capacitance is dominated by C_q, and consequently, $\partial \Phi_f^0 / \partial \Phi_g$ approaches unity even in the device's ON state. This will be of importance particularly for the ON-state performance of T-NW-FETs as will be discussed in Section VIII-B.

III. MODELING TRANSPORT IN NW-FETS

In this section, a framework of a model for NW FETs and the quantum mechanical simulations of their electrical behavior will be introduced. Our model is rather general and applies to a variety of 1-D FET structures. Material-specific properties are accounted for by the effective masses of electrons and holes, the energy gap, and the diameter of the NWs. The model is able to describe the following:

1) ballistic as well as scattering-limited transport (described by Buettiker contacts) in the nanotube channel;
2) single as well as multimode transport, including several conduction and valence bands;
3) tunneling phenomena, in particular direct source-to-drain tunneling, tunneling through the gate oxide, and BTBT.

The simulations are based on a self-consistent solution of the Schrödinger equation using the nonequilibrium Green's function formalism and the modified 1-D Poisson equation discussed earlier [see (1)]. In the present approach, we do not consider any single-electron phenomena. However, as has been shown by Indlekofer *et al.*, this can be done in a similar fashion using a multiconfigurational self-consistent Green's function algorithm [29]–[31].

To numerically compute the Green's functions, we make use of Datta's approach [32]. We consider a 1-D finite difference scheme with lattice constant a and nearest neighbor hopping, as shown in the main panel of Fig. 5. A quadratic dispersion relation in the conduction and valence bands (see the inset of Fig. 5) is used, with effective masses being $m_c^\star$ and $m_v^\star$, respectively. In order to describe the complex band structure in the bandgap, we make use of Flietner's dispersion relation [33], [34]. At lattice point i, this dispersion relation is given by

$$\frac{\hbar^2 q^2}{2 m_c^\star} = \epsilon_i \left(1 - \frac{\epsilon_i}{E_g} \right) \left(1 - \alpha \frac{\epsilon_i}{E_g} \right)^{-2} \qquad (4)$$

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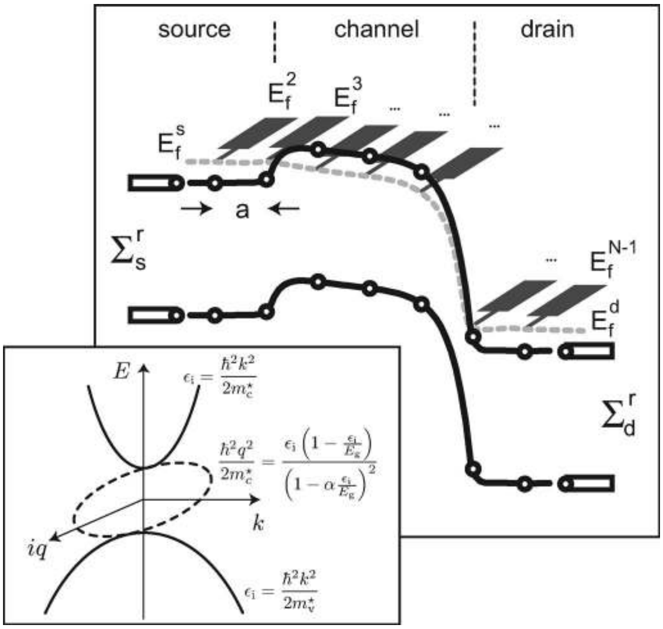
[2] Additional capacitances due to interface states, traps, etc., are neglected for simplicity.

[3] Since, in 1-D, the quantum capacitance becomes gate voltage dependent and decreases with increasing gate voltage, the maximum quantum capacitance is considered in the comparison here, which is a convolution of the thermally broadened source Fermi function with the 1-D DOS and is roughly $C_q \propto \sqrt{m^\star / 4 k_B T}$.


source
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$\epsilon_i = \frac{\hbar^2 k^2}{2m_c^\star}$
$\frac{\hbar^2 q^2}{2m_c^\star} = \frac{\epsilon_i\left(1-\frac{\epsilon_i}{E_g}\right)}{\left(1-\alpha\frac{\epsilon_i}{E_g}\right)^2}$
k
iq
$\epsilon_i = \frac{\hbar^2 k^2}{2m_v^\star}$

Fig. 5. Conduction and valence bands along the direction of current transport together with the finite difference grid with lattice spacing a. The dotted line represents the position-dependent quasi-Fermi level throughout the device. The inset shows the quadratic dispersion relation in the conduction and valence bands as well as the complex band structure in the bandgap.

where $\alpha = 1 - \sqrt{m_c^\star/m_v^\star}$, $\epsilon_i = E - \Phi_f^i$ is the kinetic energy, and E_g is the bandgap of the semiconductor under consideration. The charge neutrality or branching point E_{br} that separates electron- from hole-like states within the bandgap is at $E_{\mathrm{br}} = E_g/(2-\alpha)$; in the case of equal effective masses in the conduction and valence bands, $\alpha = 0$ and E_{br} lies at midgap. Source/drain electrodes are taken into account via retarded self-energy functions $\Sigma_{s,d}^r$ as shown in Fig. 5.

Scattering in the NW is accounted for by attaching Buettiker probes via appropriate self-energy functions to each site of the finite difference grid [35] (see Fig. 5). The difference between the source/drain contacts and the Buettiker probes is that the Fermi energy E_f^j in the Buettiker probes is not fixed by a certain terminal voltage but individually floats to a value such that the total current flowing into and out of each Buettiker probe sums up to zero. During the self-consistent calculations, the appropriate Fermi energies in the probes are found by an iterative procedure (for details, we refer the reader to [35]). Since carriers can enter one probe at a particular energy and leave it at another energy, each Buettiker probe represents a dissipative scattering site whose effectiveness is mediated by the coupling strength of the probe to the channel. As was shown by Venugopal, this coupling strength can be related to the carrier mean free path [35].

Having calculated the retarded Green's function, the local DOS (LDOS) can be determined. Fig. 6 shows a typical gray-scale image of the LDOS in a ballistic conventional-type FET with doped source/drain contacts. Dark areas refer to regions with a low DOS, whereas lighter areas indicate a high DOS. The LDOS, in turn, is used to compute the charge density ρ in the device.

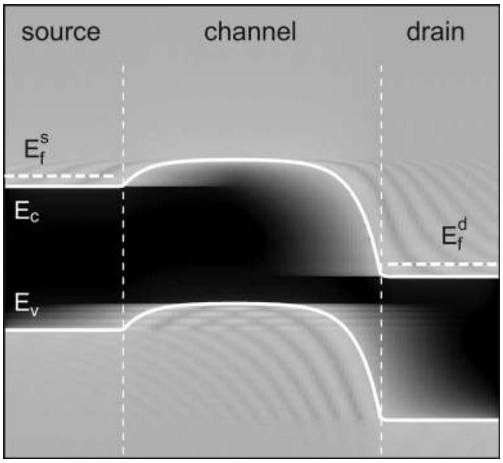

Fig. 6. Gray-scale plot of the LDOS in a conventional-type FET with doped source/drain electrodes.

The charge density ρ is used to solve the Poisson equation (1) in order to compute an update of the potential distribution within the channel, followed by recalculating ρ for the updated potential until a self-consistent solution is found. Finally, the current flowing from source to drain is computed using the Fisher Lee relation [35], [36]

$$I_d = \frac{2q}{h}\int dE \sum_{\mathrm{j}} T^{N,j}(E)\left[f\left(E - E_f^d\right) - f\left(E - E_f^{\mathrm{j}}\right)\right] \tag{5}$$

where $T^{N,j}(E)$ is the transmission coefficient between the drain contact at site N and a Buettiker probe at site j. Equation (5) is the Landauer result, where $2q/h$ is the current per energy one mode can carry, and the integral gives the number of modes times energy that contribute to the current.

IV. VLS GROWTH OF SiNWs

Let us now turn to the question of how 1-D NW structures are created. Growing SiNWs by the VLS technique has been found to be an attractive approach since VLS growth allows obtaining NWs with extremely small diameters. At the same time, there is no need for lithography and etching, which potentially leads to large surface-roughness-induced mobility degradation. Furthermore, VLS-grown SiNWs can be doped *in situ* during growth, rendering implantation and high-temperature anneals for dopant activation unnecessary. On the other hand, a bottom–up approach requires that NWs can be grown at predefined positions on a chip. Moreover, all NWs must have the same length, diameter, and crystal quality to be a viable alternative to structures obtained from top–down fabrication procedures.

We have carried out a detailed study on the VLS growth of SiNWs on (111)-oriented Si substrates using Au as catalytic seed material (called "patterned SiNW" in the following). Arrays of individual seeds were patterned by electron-beam lithography, followed by Au evaporation and liftoff (certainly, the use of gold seeds is not a successful route in terms of integrating such SiNWs into existing CMOS technology). SiNWs were grown using diluted silane as precursor gas in a low-pressure chemical vapor deposition (CVD) system [21].

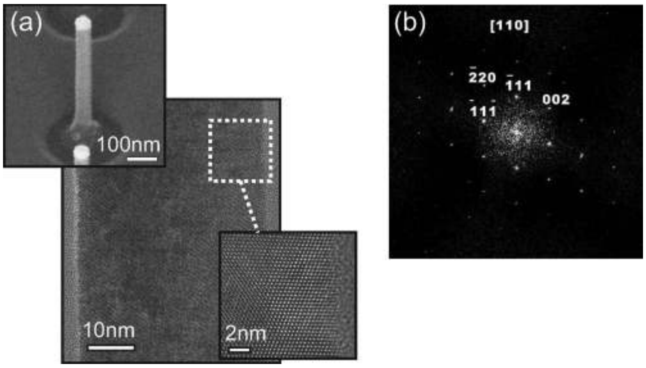

Fig. 7. (a) SEM image of a patterned epitaxially grown SiNW with gold-catalyst particle and high-resolution TEM image. (b) Diffraction pattern displaying the crystal quality of the wire and confirming the $\langle 111 \rangle$ growth direction (reprinted with permission from Schmid *et al.* [21]).

High-resolution TEM imaging and diffraction analysis on a wire grown at 470 °C and at $\mathrm{pSiH_4} = 80$ mtorr confirm the $\langle 111 \rangle$ growth direction and single crystalline nature of the SiNW [Fig. 7(a) and (b)]. The epitaxially grown SiNWs show stacking faults that range from zero to five within about 1-μm-long NWs. SiNWs are known to grow mainly in the $\langle 111 \rangle$ directions at least above a certain diameter [37], [38]. It is also observed that kinking between the equivalent directions can occur more or less frequently depending on growth conditions [39]. For integration purposes [6], [40], it is important to control growth direction and to avoid kinking during growth. To determine the conditions for kink-free epitaxial growth of patterned SiNWs, we started with the conditions proposed by Westwater *et al.* [39]. In addition, NWs with diameters larger than 50 nm were used to suppress growth directions other than $\langle 111 \rangle$. Two sets of experiments were carried out. In the first, the SiH_4 partial pressure was varied while keeping the temperature constant, and in the second, the temperature was varied at constant $\mathrm{pSiH_4}$. Fig. 8(b) shows the analysis of 20 different SiNW arrays consisting of 60-, 75-, 90-, and 105-nm-diameter wires grown at 470 °C at varying SiH_4 pressures. The yield of vertical epitaxial SiNWs increases significantly below $\mathrm{pSiH_4} = 150$ mtorr, independent of NW diameter, and approaches 60% at the lowest SiH_4 partial pressures used here. Similarly, for a constant partial pressure of 80 mtorr, the vertical epitaxial yield increases substantially for temperatures below 500 °C [21].

The possibility of creating *in situ* doping profiles along the axial direction of a SiNW is a key benefit of the VLS growth technique. The growth of n-p-n-segmented SiNWs, for example, would render ion implantation and high-temperature activation anneals unnecessary, as has already been mentioned earlier. The feasibility of *in situ* doping of SiNWs has been demonstrated using diborane (B_2H_6) and trimethylborane (TMB) for p-type and phosphine (PH_3) for n-type doping, respectively [41], [42]. Here, diborane was used at an atomic ratio of SiH_4 to B_2H_6 in the gas phase of 1000:1 for the formation of p-type source/drain sections. Doping levels in the mid-10^{18} $\mathrm{cm^{-3}}$ were achieved with only little radial silicon deposition along the SiNWs. For n-type SiNWs, PH_3 was used as dopants to grow SiNWs with an atomic ratio in the gas phase of $SiH_4 : PH_3$ of up to 333:1, which gives a phosphorus concentration in the low 10^{19} $\mathrm{cm^{-3}}$ range [43]. We did not observe any noticeable change in morphology or growth rate compared with intrinsic growth.

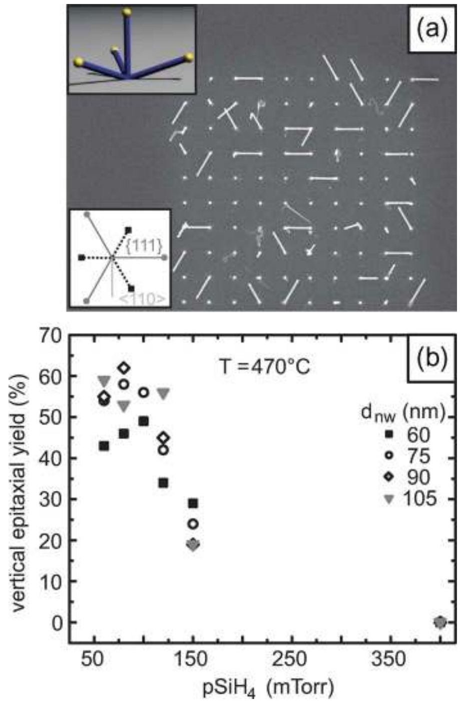

Fig. 8. (a) Top-view SEM image of an array of 60-nm-diameter SiNWs grown at 470 °C. The top inset illustrates the possible $\langle 111 \rangle$ directions out of the $\langle 111 \rangle$ substrate. The bottom inset shows three additionally observed directions (dashed) that are rotated by 60° to the three regular inclined $\langle 111 \rangle$ directions. (b) Yield of vertical epitaxial wires versus partial pressure for diameters ranging from 60 to 105 nm (reprinted with permission from Schmid *et al.* [21]).

V. NW-FETS WITH METALLIC SOURCE/DRAIN CONTACTS

The simplest approach to fabricate an NW-FET is by placing an NW on top of an oxidized silicon wafer and attaching metal contacts as source and drain electrodes; the silicon substrate then serves as a large-area back gate. A SiNW device of this type is shown in Fig. 1. While resembling a conventional MOSFET, the device shows a vastly different electrical behavior since the gate overlaps the source/drain regions resulting effectively in an SB-FET.

In case of the device shown in Fig. 1, a gate oxide was first grown uniformly around the SiNW [44] prior to deposition of the wires onto the substrate. This approach is critical in order to passivate the silicon surface and for the fabrication of top-gated NW-FETs, as will be discussed hereinafter. In order to access the SiNW for source/drain formation, the gate oxide was removed using buffered oxide etch right before nickel deposition. During this process step, the resist mask is employed to define the contact areas and to protect the gate oxide outside the source/drain regions at the same time. After a standard liftoff, a silicide is formed using rapid thermal processing. A rather low temperature of 280 °C was chosen since nickel tends to diffuse quickly into the SiNWs. In fact, we found that the nickel diffusion strongly increases with temperature and decreasing NW diameter [10]. This has to be taken into account when fabricating NW-FETs.

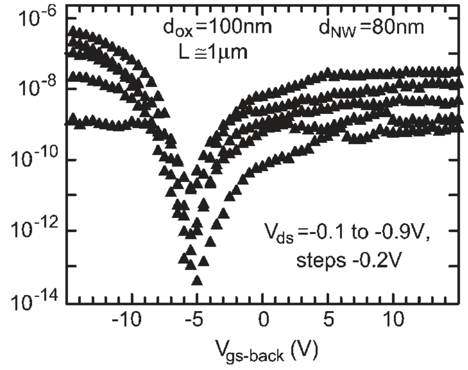

Fig. 9. Subthreshold characteristics of the device shown in Fig. 1. Clear ambipolar characteristic result from the line-up of the Fermi level of nickel source/drain contacts close to the middle of the silicon bandgap [10].

Fig. 9 shows the corresponding subthreshold characteristics of the device with $d_{\text{ox}} = 100$ nm and $L \approx 1$ μm exhibiting clear ambipolar behavior as expected for an SB-FET. Furthermore, the inverse subthreshold slope is approximately 1500 mV/dec far in excess of the thermal limit. As will become clear in the succeeding discussions, this is a consequence of the injection of carriers through the SB. With a lineup of the nickel Fermi level close to the middle of the silicon bandgap, both hole injection from the source into the valence band and electron injection from the drain into the conduction band are enabled for negative and positive gate voltages, respectively. This behavior is similar to what has been found in carbon nanotube transistors [24], [45] underlining the commonalities between the two classes of devices. Some confusion has occurred in the past when attempting to understand NW device characteristics in the context of contact switching due to the apparent presence of scattering inside the silicon channel. While it is accepted that SBs dominate transport in carbon nanotube devices, NW devices are frequently used to extract mobilities assuming that intrinsic properties dominate the device performance. In a later section of this paper (see Section VI-B), we will discuss, in more general terms, the relationship between SB impact versus scattering inside the semiconducting channel, elucidating on the necessity to create extremely long channels to extract mobility values in NW transistors. In addition, we will provide experimental evidence that the assumption of an NW-FET being dominated by its intrinsic properties is rarely justified (Section VII).

VI. TRANSPORT IN SiNW SB-FETs

In the preceding section, we observed that NW-SB-FETs exhibit ambipolar behavior due to injection of electrons and holes through the SB present at the source/drain electrode–channel interfaces. Moreover, the inverse subthreshold slopes of SB-FETs are rather large. By using a simple analytical model for the potential profile at the source Schottky diode, we will show in this section that this peculiar behavior (not expected in conventional-type FETs as long as electrostatic integrity is preserved) is a consequence of the dependence of the carrier injection through the SB on the screening length λ [46].

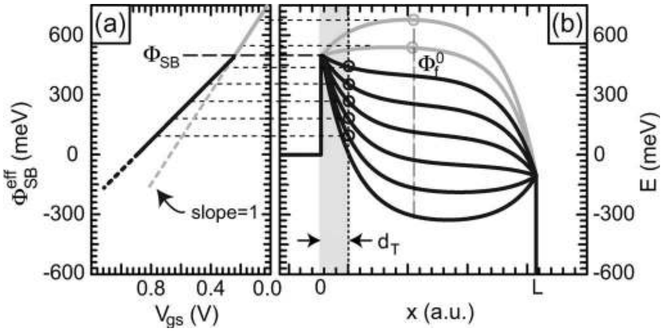

Fig. 10. (a) Effective SB height $\Phi_{\text{SB}}^{\text{eff}}$ as a function of V_{gs}. (b) Conduction band profiles for various gate voltages.

*A. Transport in SB-NW-FETs—*OFF *State*

It has been mentioned earlier that the modified Poisson equation (1) leads to an exponential screening of potential variations on the length scale λ which, in turn, depends on the channel body thickness, i.e., NW diameter and gate oxide thickness. This means that the SBs can be made "thinner" and, therefore, more transparent if d_{nw} and d_{ox} are scaled down yielding an improved electrical behavior.

Fig. 10(b) shows the conduction band in an SB-FET for various gate voltages. If V_{gs} is such that the potential lies above the SB Φ_{SB} at the source contact (gray curves in Fig. 10), then the maximum potential barrier that determines the current flow is not the SB but lies approximately in the middle of the channel, and the SB-FET in this regime behaves rather like a conventional FET. Consequently, one expects a steep inverse subthreshold slope in this regime, which is, indeed, experimentally observed [47]. Once the bands are moved below Φ_{SB}, the injection of carriers is given by thermal emission over and thermally assisted tunneling through the SB.

The actual potential profile of the source SB can be replaced with an effective SB $\Phi_{\text{SB}}^{\text{eff}}$ for thermal emission alone. To this end, a tunneling distance d_T is defined [see Fig. 10(b)], and the tunneling probability through the SB is set to unity if the barrier at some energy is thinner than d_T and zero otherwise. The exact value of d_T does not matter for the time being. However, an estimate can be obtained using the WKB approximation showing that d_T mainly depends on material-specific parameters such as $m^\star$ but only weakly depends on V_{gs}. In silicon SB-FET, a reasonable value for d_T is in the range of 3.5–3.7 nm [46], whereas, e.g., in carbon nanotubes, d_T is in the range of 5 nm due to the lighter effective mass [14]. Fig. 10(a) shows the change of the effective SB with changing V_{gs}. Obviously, the slope of $\Phi_{\text{SB}}^{\text{eff}}(V_{\text{gs}})$ is substantially smaller than unity, and since the effective SB now determines the carrier injection, one expects an inverse subthreshold slope significantly larger than 60 mV/dec.

In the OFF state, the density of mobile carriers is small, i.e., $\rho \approx 0$, and (1) can be solved, analytically leading to

$$\Phi_{\text{SB}}^{\text{eff}} = \Phi_f(d) = (\Phi_{\text{SB}} - \Phi_f^0)\exp(-d_T/\lambda) + \Phi_f^0 \qquad (6)$$

where $\Phi_f^0 = \Phi_g + \Phi_{\text{bi}}$ is the surface potential in the channel (in the case $L \gg \lambda$) several λ away from the contact interface [see dashed line in Fig. 10(b)]. Note that (6) has the

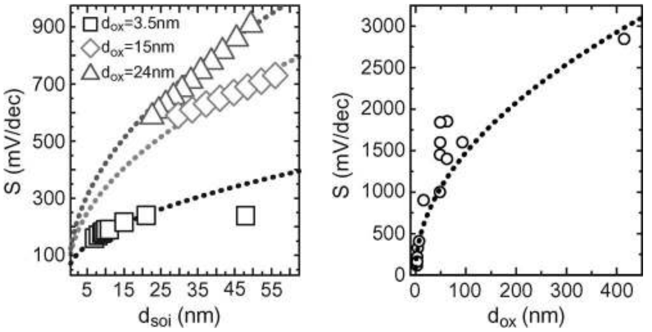

Fig. 11. Inverse subthreshold slopes as a function of the channel body thickness (a) in the case of ultrathin-body SOI [48]. (b) S as a function of d_{ox} extracted from transfer characteristics of carbon nanotube SB-FETs [24]. The dotted lines are results from an analytical calculation (see Section VI-A).

same form as given previously (see Section II) in the case of a conventional device suffering from SCEs, where $\Phi_{\mathrm{SB}}^{\mathrm{eff}}$ represents the potential barrier that determines the carrier injection. Since $\partial\Phi_{\mathrm{SB}}^{\mathrm{eff}}/\partial\Phi_g < 1$, SB devices appear to suffer from SCEs, and $S > 60$ mV/dec can be expected, although the device is electrostatically well-behaved. Fig. 10(a) and (b) shows $\Phi_{\mathrm{SB}}^{\mathrm{eff}}$ as a function of gate voltage and the corresponding conduction band profiles for various V_{gs}'s, respectively. When $\Phi_f^0 \geq \Phi_{\mathrm{SB}}$, then $\Phi_{\mathrm{SB}}^{\mathrm{eff}} = \Phi_f^0$, and consequently, $\partial\Phi_{\mathrm{SB}}^{\mathrm{eff}}/\partial\Phi_g = 1$ [gray line in Fig. 10(a)]. However, as soon as $\Phi_f^0 < \Phi_{\mathrm{SB}}$, the curve in Fig. 10(a) (black line) deviates from the one-to-one dependence (black line) with the slope given by (6). A closed expression for S can be obtained by noting that $S = \ln(10)((\partial I_d/\partial\Phi_{\mathrm{SB}}^{\mathrm{eff}})(\partial\Phi_{\mathrm{SB}}^{\mathrm{eff}}/\partial V_{\mathrm{gs}})(1/I_d))^{-1}$ and $I_d \propto \exp(-\Phi_{\mathrm{SB}}^{\mathrm{eff}}/k_BT)$

$$S = \frac{k_BT}{q}\ln(10)\frac{1}{1-\mathrm{e}^{\frac{-d_T}{\lambda}}} \overset{d_T<\lambda}{\approx} \frac{k_BT}{q}\ln(10)\left(\frac{1}{2}+\frac{\lambda}{d_T}\right). \tag{7}$$

Equation (7) suggests a square-root dependence of the inverse subthreshold slope on the channel thickness (NW diameter) and gate oxide thickness in a back-gated device configuration. Scaling down both leads to a steeper inverse subthreshold slope due to a thinner SB resulting in an increased carrier injection.

Fig. 11(a) shows extracted S values as a function of the channel body thickness for three different d_{ox}'s in the case of an SOI-SB-MOSFET [47], and Fig. 11(b) shows S as a function of d_{ox} in the case of carbon nanotube FETs [24]. In both cases, a strong dependence of S on the channel body thickness and d_{ox} is observed as expected from our analysis mentioned earlier. Decreasing both leads to significantly steeper inverse subthreshold slopes and consequently to an improved injection of carriers through the SB. Indeed, the dotted lines in Fig. 11 were calculated using (7) and show excellent agreement with the experimental data, reconfirming that the introduction of a tunneling distance d_T and thereby replacing the actual SB with a barrier for thermal emission alone are justified. Note that this pure electrostatic effect applies to all kinds of ultrathin-body FET devices such as SOI, carbon nanotube, and also NW-SB-FETs.

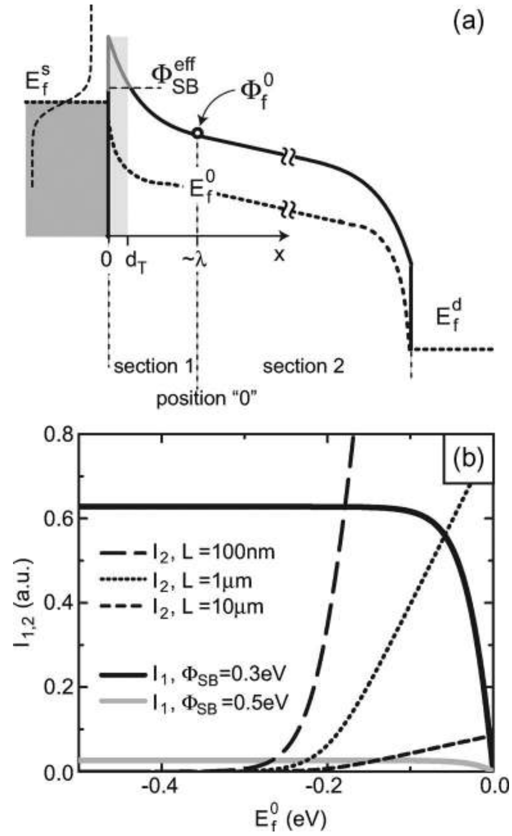

Fig. 12. (a) Conduction band in the ON state of an SB-FET. (b) Current through the Schottky diode (solid curves) and the channel (dashed and dotted curves) as a function of the quasi-Fermi level at point $x = \lambda$.

B. Transport in SB-NW-FETs—ON *State*

In the device's ON state, the charge in the channel cannot be neglected anymore since it will have a significant impact on the potential distribution within the channel and, in turn, also on the potential landscape of the source and drain Schottky diodes. In order to account for the charge in the channel and also for scattering in the channel, we subdivide the channel into two segments. The first segment (called "1," in the following) comprises the Schottky diode and has a spatial extent on the order of λ, as shown in Fig. 12(a). The second segment ("2") extends up to the drain contact (where the particular potential landscape at the drain Schottky diodes is disregarded for simplicity); the interface between segments "1" and "2" will be referred to position "0" in the following [see Fig. 12(a)]. Depending on the tunneling probability through the source SB and the scattering within the channel, part of the drain–source voltage will drop across segment 1 and the rest drops along the remainder of the channel. In order to calculate an approximate expression for the ON-state current, one has to compute the surface potential Φ_f^0, which allows obtaining $\Phi_{\mathrm{SB}}^{\mathrm{eff}}$. However, to do so, we need to know the charge density at the point $x = \lambda$ [see Fig. 12(a)]. If we know the quasi-Fermi level E_f^0 in $x = \lambda$, we can approximately calculate the charge at this position by simply integrating over the product of the DOS at this position with an equilibrium Fermi function $f(E_f^0)$. The quasi-Fermi level E_f^0 can be calculated by equating the individual current components through segments "1" and "2," $I_1 \stackrel{!}{=} I_2$, yielding[4]

$$\frac{l_{\text{scat}}}{l_{\text{scat}}+\lambda}\int\limits_{\Phi_{\text{SB}}^{\text{eff}}}^{\infty} dE\,\left(f(E_f^s)-f(E_f^0)\right) \tag{8}$$

$$\stackrel{!}{=} \frac{l_{\text{scat}}}{l_{\text{scat}}+L}\int\limits_{\Phi_f^0}^{\infty} dE\,\left(f(E_f^0)-f(E_f^d)\right) \tag{9}$$

where we have accounted for scattering in the channel with a simple energy-independent transmission function $T(E) = l_{\text{scat}}/(l_{\text{scat}}+L)$ [32]. For carriers that scatter within the steep potential variation region within segment 1, it is unlikely to be scattered back into the source contact once they have lost k_BT in energy, since the Schottky diode rapidly becomes "thicker," preventing the carriers from tunneling back [48], [49]. Thus, one has to modify the transmission function and replace the channel length L with λ in the left term in (8) [49]. Equation (8) yields a transcendent equation for E_f^0 that can be solved numerically or graphically. If we plot both current contributions in the same graph, then E_f^0 is given by the intersection of the two curves. Note that E_f^0/q is the voltage that has dropped across segment 1, i.e., at the SB. This means that if $E_f^0 \approx 0$, then almost all of the drain–source bias drops across the channel, whereas for $|E_f^0| \to qV_{\text{ds}}$, all voltage drops at the source Schottky diode. Since the tunneling probability through the SB depends on d_{ox}, d_{nw}, and the gate voltage, E_f^0 will be a function of these three quantities, and the transcendent equation has to be solved for each set of parameters individually.

To illustrate that very long channel lengths are required in order for an SB-FET to be dominated by scattering, Fig. 12(b) shows exemplarily I_1 (black curve) for a back-gated SB carbon nanotube FET with $d_{\text{ox}} = 10$ nm, a very thin diameter of $d_{\text{nt}} = 1$ nm, an SB of 0.3 eV, and a mean free path of $l_{\text{scat}} = 100$ nm. Biases of $V_{\text{ds}} = 0.5$ V and $V_{\text{gs}} = 0.5$ V, i.e., in the device's ON state, were assumed in the present case. I_2 is plotted for three different channel lengths (see the figure for details). In the present case (which is typical of back-gated carbon nanotube FETs), the largest part of the potential drops across the SB for $L = 100$ nm and $L = 1$ μm. This means that the current through SB carbon nanotube FETs is determined by the SB rather than the transport properties of the channel. As such, SB-FETs can be denoted as "contact-switching" devices. The current is dominated by scattering within the channel only for very long channels [10 μm in the present case; see the black dashed curve in Fig. 12(b)]. The same reasoning applies qualitatively to NW-FETs as well. Although the scattering mean free path will be significantly smaller in SiNW, for instance, the SB height will also be higher. The channel length for which scattering in the channel dominates over the scattering across the SB depends exponentially on the SB height and λ. The resistance of the channel, on the other hand, increases only linearly with channel length L. To illustrate the effect of a larger SB, the actual Schottky height was increased to 0.5 eV (gray solid curve): Again, a significant part of the bias drops across the Schottky diode, making even longer channel lengths necessary for the electronic transport to be solely dominated by scattering within the channel. As a result, scattering in the channel only plays a role if the following are true: 1) Φ_{SB} is rather low and/or the SB is very thin and thus highly transmissive, or 2) the channel is appropriately long. This has an important implication, namely, that care has to be taken when one extracts the mobility from nanotube or NW-SB-FETs. This is only possible if the channel length is long enough such that the electrical behavior of the device is determined by the scattering in the channel and not by the tunneling through the Schottky diodes at the contacts. The required length can be rather long.

Having determined the quasi-Fermi level, the charge at position "0" can be computed, and hence, Φ_f^0 can be determined. To do so, we assume that around the position "0," the curvature term in the modified Poisson equation can be neglected [see (1)]. Then, Φ_f^0 can be calculated, which, in turn, is employed to compute $\Phi_{\text{SB}}^{\text{eff}}$ as a function of gate voltage. This task has to be done either numerically or with some approximation for the Fermi–Dirac integral. The dependence of current on λ, however, can be stated explicitly as follows:

$$I_d \approx \frac{2q}{h}\frac{l_{\text{scat}}}{l_{\text{scat}}+\lambda}k_BT\ln\left(\frac{e^{\left(\frac{E_f^s-\Phi_{\text{SB}}^{\text{eff}}}{k_BT}\right)}+1}{e^{\left(\frac{E_f^0-\Phi_{\text{SB}}^{\text{eff}}}{k_BT}\right)}+1}\right). \tag{10}$$

Hence, the drain current strongly improves when decreasing λ even in the ballistic case due to the exponential dependence of the effective SB height on λ (see, for instance, [50]). The reason for this is again that the carrier injection into the channel is strongly improved in UTB SB-FETs with thin gate oxides. As a result, decreasing the NW diameter in a wrap-gate device layout allows obtaining strongly improved inverse subthreshold slopes and ON-state currents, which is a major benefit of SB-NW-FETs.

VII. CONVENTIONAL-TYPE NW-FETs

To eliminate the impact of contacts on the device characteristics, one can fabricate conventional-type NW-FETs by doping the source/drain contacts with ion implantation and activation annealing [9]. However, here, we have realized a conventional-type SiNW device by creating highly doped contact regions for carrier injection via "electrostatic doping." The idea is to prevent the metal/semiconductor interfaces in the source and drain regions to be impacted by the gate using a second gate that only acts on source/drain extensions. While SB-FETs frequently exhibit a linear response of the drain current to the drain voltage, the transmission through the SB and hence the injection of carriers is gate voltage dependent and *not* constant as would be the case in ohmic contacts. For this reason, we created a device with a p/i/p doping profile. Fig. 13 shows an electron micrograph of the NW transistor under consideration. The aluminum top gate is only operating on a portion of

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[4] Note that this is similar to attaching a Buettiker probe at position $x = \lambda$, i.e., we have implicitly assumed an inelastic scattering mechanism responsible for the potential drop across the Schottky barrier.

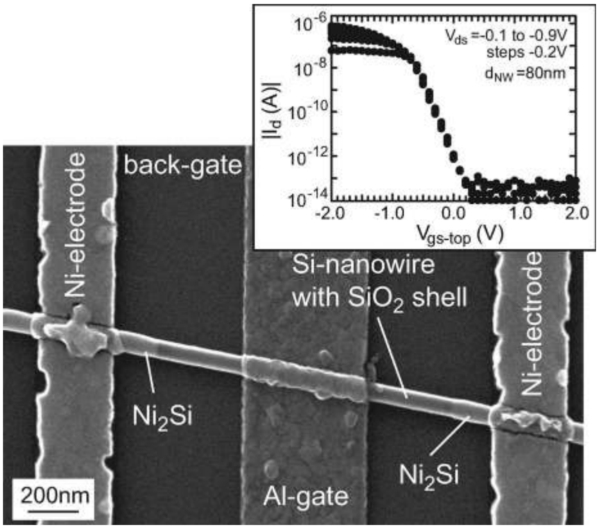

Fig. 13. NW transistor with p/i/p doping profile. A 5-nm-thick wrap-around silicon dioxide layer acts as the gate dielectric [10].

the SiNW, while the electrostatics of the FET close to the source and drain metal contacts is controlled independently by the back gate—the silicon substrate. The back gate allows simulating the situation of a partially doped NW with p-type or n-type NW segments next to the intrinsic gated portion of the same wire. In this way, it is ensured that the injection properties into the gated NW region remain unaffected by the gate voltage $V_{\mathrm{gs-top}}$. Note that for improved carrier injection, portions of the SiNW have been converted into $\mathrm{Ni_2Si}$. Details of our study on the silicide formation and NW diameter dependence can be found elsewhere [10]. By applying a sufficiently negative voltage to the substrate, holes are accumulated between the source and the gate and the drain and the gate, rendering these NW segments conducting. The aluminum gate on top of the oxidized middle region of the SiNW can then be used to turn the device on and off, resulting in conventional looking unipolar device characteristics (see inset of Fig. 13). With this type of dual-gate NW device, we are able to study the impact of contacts versus intrinsic transport properties.

In order to elucidate on the impact of contacts even in the presence of scattering inside the SiNW channel, we focused on the output characteristics. The saturation region in conventional I_d–V_{ds} characteristics is typically associated more than any other region with the intrinsic properties of the NW dominating current flow. This is the case since this high differential resistance area with dI_d/dV_{ds} around zero is commonly associated with pinchoff in the gated channel region in conventional transistors. With the highest resistance inside the channel, it seems logical to assume that this region is mainly impacted by the scattering properties of the NW material. However, our experimental results prove that this is not the case. Fig. 14 compares the output and transfer characteristics of the same device with two slightly different SBs. Experimentally, this situation has been realized by measuring the same device before and after annealing to convert the nickel electrodes into nickel silicide contacts. The annealing step changes the injection properties at the metal NW interface but leaves the gated portion of the NW unaffected. If, indeed, the intrinsic properties dominate the transport conditions inside the NW channel in the saturation region of the I_d–V_{ds} characteristics, extracting the mobility should result in the same intrinsic number. In other words, the transconductance g_m should be unaffected by changing the contacts. Our results, however, show a difference of more than one order of magnitude in g_m that cannot be explained within the framework of the classical diffusive transport picture. It is not justified to envision the transport conditions in this type of NW device as if current flows through a series of resistors. Instead, momentum is conserved even in the presence of some scattering inside the channel over distances long enough that make it necessary to look at the system as a whole. The simple model of the ON-state performance of SB-FETs discussed in the preceding section shows that intrinsic NW properties cannot easily be extracted unless contact effects are explicitly subtracted. Our experiments indicate that even in conventional-type NW-FETs, it is almost impossible to conclude from experimental data whether contact effects are or are not present due to the subtleties of transport in ultrasmall body devices.

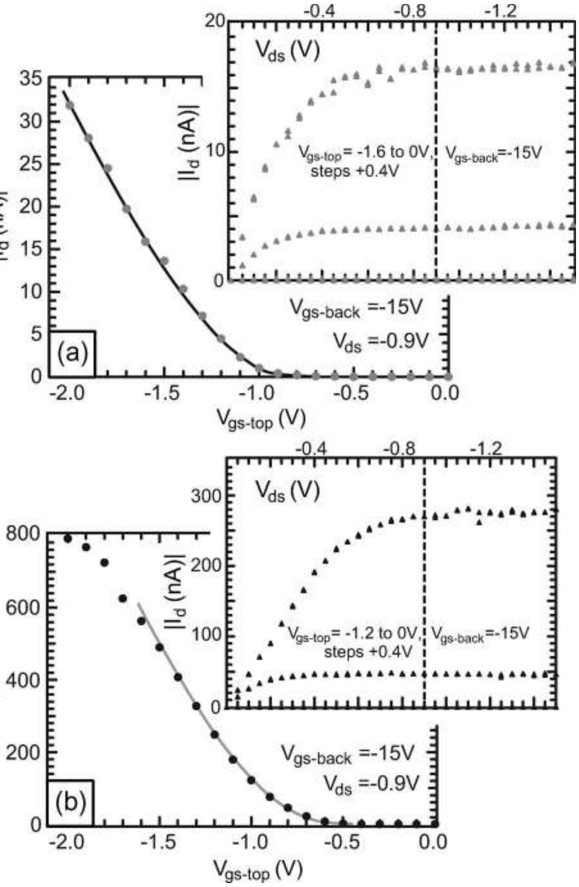

Fig. 14. Transfer and output characteristics of the device in Fig. 13(a) before and (b) after silicide formation. Lines are guides to the eye (graphs are taken from [10]).

VIII. STEEP-SLOPE NW-FETs

In the last section of this paper, we want to discuss new FET device layouts that allow realizing transistors with a superior turn-on behavior if compared to conventional FETs—so-called “steep-slope switches.” The increasing interest in such device architectures stems from the fact that conventional-type FETs with doped source–drain regions in general suffer from a fundamental problem: Irrespective of dimensionality, material in use, or device dimensions, *any* conventional FET is limited to a minimum inverse subthreshold slope of 60 mV/dec at room temperature, as has been discussed previously. This limitation is a major obstacle to further reduce the supply voltage and hence the power consumption of integrated circuits. Providing a certain ratio between the OFF-state and the ON-state current of approximately three orders of magnitude is required, and if we assume that two-third of the maximum applied gate voltage is needed to obtain a high ON-state current [28], one needs at least a gate voltage range of $3 \times (3 \cdot 60\ \text{mV/dec}) = 540\ \text{mV}$ to properly operate the device. In turn, this means that scaling down the supply voltage of devices limited to an $S = 60$ mV/dec leaves only two options: either the OFF-state leakage is increased or the ON-state performance deteriorated. Therefore, transistor devices that show an inverse subthreshold slope significantly steeper than 60 mV/dec and still provide a high ON-state performance are highly desirable.

The reason for the limit of S to a minimal value of 60 mV/dec is the fact that the switching mechanism of conventional-type devices relies on the modulation of the injection of carriers from a thermally broadened Fermi function. Hence, in order to achieve subthreshold swings below 60 mV/dec, the current injection from the source contact has to be modified in a way that it becomes independent of a thermally broadened Fermi distribution function. Recently, II and BTBT have been proposed as effective means to accomplish this [51]–[59]. In the following, we will discuss these two concepts applied to FETs, both using simulations and showing experimental results.

A. II NW-FETs

II MOSFETs (IMOS) consist of a gated reversed biased p-i-n structure where the gate covers only a part of the intrinsic (i) region [51], [53]. Applying large enough gate–source and drain–source voltages, II occurs and induces an avalanche breakdown in the intrinsic region. The avalanche multiplication of carriers results in extremely steep turn-on characteristics with inverse subthreshold slopes significantly smaller than 60 mV/dec and rather large ON-state currents due to the internal gain mechanism. However, due to the high electric fields required to induce II, IMOS devices usually need to be operated at rather large voltages of a few volts, which prevents scaling the operational voltage and, therefore, the exploitation of the steep turn-on characteristic. Moreover, IMOS transistors suffer from reliability issues because of hot carrier injection into the gate dielectric [51]. The hot carrier injection is amplified by a planar device layout that leads to a significant acceleration of carriers toward the gate dielectric. Measures to improve IMOS devices therefore necessitate a controlled reduction of the length of the intrinsic (II) region in order to obtain high electric fields at moderate voltages. Furthermore, those measures include the reduction of vertical electric fields and, hence, hot carrier degradation. In this respect, a vertical IMOS design, together with a gate-all-around device architecture, is beneficial for the performance of IMOS transistors. We have therefore fabricated vertical wrap-gate IMOS based on bottom–up grown SiNWs.

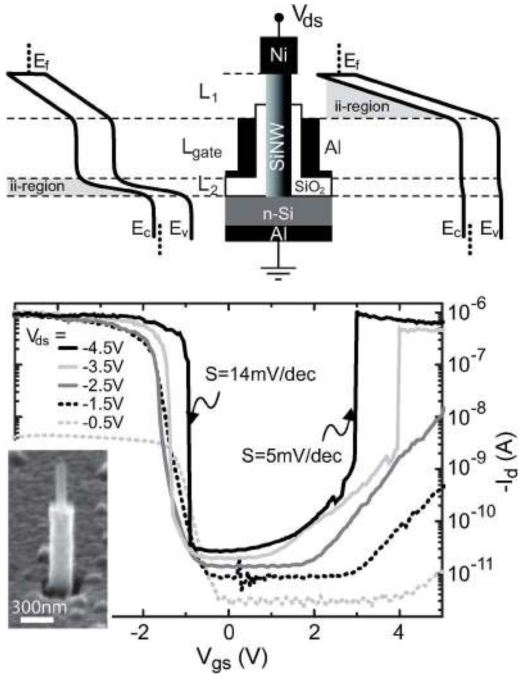

Fig. 15. (Top part) Schematics of the vertical NW-IMOS and the conduction/valence band profiles in the ON state of the device. The main panel shows transfer characteristics with inverse subthreshold slopes as small as 5 and 14 mV/dec, respectively. The inset shows a SEM of a fabricated device without top contact (reprinted with permission from Lew *et al.* [41[41]).

Undoped SiNWs were epitaxially grown on n-type (111) Si wafers leading to vertical NWs (see Section IV). After NW growth, the gate dielectric is deposited via PECVD. One advantage of this approach is that the ungated intrinsic region between bottom contact and channel is defined by the gate dielectric thickness, i.e., by a deposition technique and not by lithography (denoted as L_2 in the top part of Fig. 15), and is therefore accurately and reproducibly controlled. Conventional lithography and metallization were used to define gates and top contacts to individual NW-FETs (details of the fabrication process can be found in [40]). The inset of Fig. 15 shows an electron micrograph of a fabricated device without the top contact.

The main panel of Fig. 15 shows transfer characteristics of an IMOS device for bias voltages between -0.5 and -4.5 V. In the present case, the bottom contact (wafer) is grounded and a drain–source voltage is applied to the top nickel contact. A slight shift of the threshold voltage with changing V_{ds} can be observed; however, more importantly, subthreshold swings as low as 5 and 14 mV/dec are measured, respectively. The reason for the ambipolar behavior is the presence of two intrinsic regions in our device, one at the top of the gated region (L_1) and one between the wafer and the gate (L_2) as schematically shown in the top part of Fig. 15. II occurs in either of the two depending on the bias conditions, giving rise to the experimentally observed ambipolar behavior.

It was mentioned earlier that a major disadvantage of IMOS devices is that they are prone to degradation due to hot carrier injection into the gate dielectric. Fig. 16 shows transfer characteristics of the vertical NW IMOS device for several (>100) sweeps of gate voltage. A hysteresis is observed which is

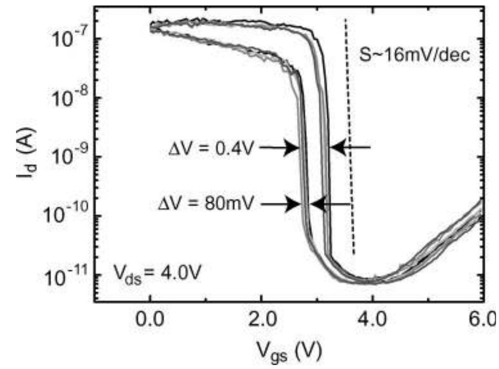

Fig. 16. Repeated measurements (more than 100 voltage sweeps) of a vertical wrap-gate SiNW-IMOS. The observed hysteresis is due to the chosen gate dielectric. A shift of the threshold voltage is not observed [61].

mainly due to the use of a low-temperature PECVD gate oxide, giving rise to a rather high number of defect/interface states. The important point, however, is that the threshold voltage (of each forward/backward sweep) remains almost unaltered while sweeping the gate voltage. Reasons for the suppression of an additional V_{th} shift and hence hot electron degradation are the lower operating voltages compared to conventional planar IMOS FETs and, equally important, the smaller vertical fields within the channel due to the use of an NW with small diameter in a wrap-gate configuration [40], [60], [61]. This means that the improvement of the present IMOS devices when compared to planar IMOS devices can be attributed to the particular device layout enabling a precise definition of the intrinsic II regions as well as a reduction of vertical fields due to the wrap gate. Considering materials such as germanium or III–V compound semiconductors with a lower bandgap, it will be possible to further reduce the operational voltages of IMOS devices. As a result, combining a low-bandgap material with a vertical wrap-gate design might enable reliable high-performance IMOS devices.

B. Tunnel FETs—Device Structure and Working Principle

Like IMOS devices, tunnel FETs are gated p-i-n structures consisting of a p-doped source(drain), an intrinsic channel, and an n-doped drain(source). In contrast to IMOS devices, however, the intrinsic part of tunnel FETs is covered completely by the gate and the switching mechanism relies on BTBT rather than II. In the following, we will investigate the electronic transport in such tunnel FETs and show that NWs and, in particular, NWs providing 1-D electronic transport are a premier choice for the realization of high-performance tunnel FETs with steep inverse subthreshold slopes and good ON-state performance.

Consider a device structure as shown in Fig. 17(a). In order to obtain an optimal gate control over the bands in the channel (NW with diameter d_{nw}), the transistor exhibits a wrap gate and a thin gate oxide of thickness d_{ox}. Fig. 17(b) shows the conduction and valence bands in a tunnel FET in the OFF state (gray dotted lines) and in the ON state (black solid lines). In the OFF state, the bandgap of the source, channel, and drain regions prevents current flow, resulting in very low OFF-state leakage currents. On the other hand, in the ON state, BTBT at the source-side n-p junction leads to injection of holes from the source contact into the channel constituting the ON-state current.

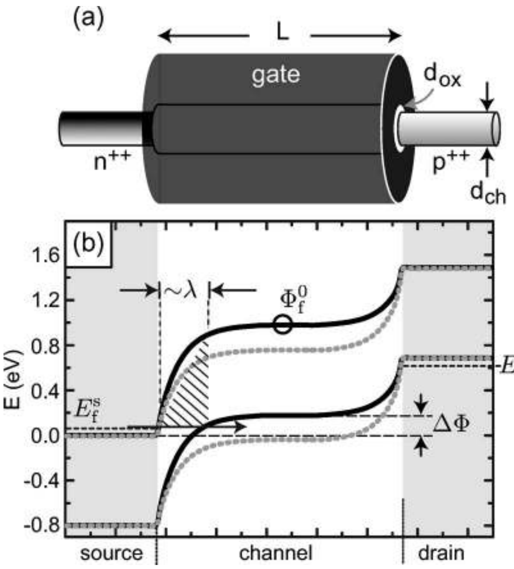

Fig. 17. (a) Schematics of a T-NW-FET with wrap-gate design. (b) Conduction and valence band profiles in the device's OFF state (gray dotted lines) and in its ON state (black solid lines).

Before investigating the electronic transport in T-NW-FETs with simulations, we will discuss the working principle of the tunnel FET and under what circumstances an S smaller than 60 mV/dec can be achieved. Looking again at the conduction and valence bands in the ON state of a tunnel FET [Fig. 17(b)], it becomes apparent that, as soon as the gate pulls the valence band in the channel above the conduction band in the source contact, a channel for BTBT is opened up. For a sufficiently "thin" BTBT barrier, the current through the device is then determined by the tunneling of carriers within the energetic window denoted as $\Delta\Phi$ in Fig. 17(b). An analytic expression for the current can be obtained using the WKB approximation for the BTBT probability [57], [62]

$$I_d \approx \frac{2e}{h} T_{\text{WKB}} k_B T \ln \left(\frac{\exp\left(\frac{\Delta\Phi - E_s^f}{k_B T}\right) + 1}{\exp\left(-\frac{E_f^s}{k_B T}\right) + 1} \right) \tag{11}$$

where we assumed a drain–source bias that is large enough to ensure that, within $\Delta\Phi$, the drain Fermi function is approximately one. The tunneling probability in WKB approximation becomes energy independent if one approximates the source-channel n-p junction with a triangular potential barrier as shown with the hatched area in Fig. 17(b) [57], [62]. In addition, we know from the discussion earlier that p-n junctions in NW transistors (and also any other ultrathin body device) have a spatial extent on the order of λ [see (1)]. As a result, T_{WKB} can be written as [57]

$$T_{\text{WKB}} \approx \exp\left(-\frac{4\lambda\sqrt{2m^\star} E_g^{3/2}}{3\hbar(E_g + \Delta\Phi)} \right). \tag{12}$$

Note that (12) considers a semiconductor with a direct bandgap. However, the expression for the BTBT probability in a

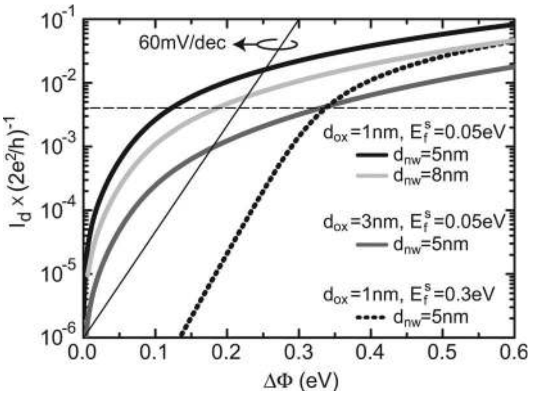

Fig. 18. Normalized drain current in a 1-D T-NW-FET with wrap-gate device layout. A constant current level (dashed line) is taken to determine the potential at threshold. Only the devices with thin $d_{\rm ox} = 1$ nm yield average inverse subthreshold slopes steeper than 60 mV/dec.

semiconductor with indirect bandgap exhibits the same dependences on λ, $m^\star$, and the bandgap [62]. A number of insights can be obtained from this simple expression together with (11): Obviously, the tunneling probability and hence I_d can be made large if λ is made small. Furthermore, the inverse subthreshold slope in a tunnel FET depends on $V_{\rm gs}$ and can either be easily calculated by noting that $S = \ln(10)(\partial I_d/\partial V_{\rm gs} \cdot 1/I_d)^{-1}$ or extracted from log-scale plots of I_d–$V_{\rm gs}$.

Fig. 18 shows the transfer characteristics of a wrap-gate T-NW-FET calculated using (11) for four different cases specified in Fig. 18 (note that for simplicity, we did not take the impact of the charge in the channel on $\Delta\Phi$ into account, meaning we assumed $\delta\Phi_f^0 = -q\delta V_{\rm gs}$; this is justified in the OFF state if $V_{\rm ds}$ is large enough).

When extracting the inverse subthreshold slope, it is important to note that the inverse subthreshold slope is no longer a constant in a BTB tunnel FET. Therefore, an averaged $\bar{S} <$ 60 mV/dec over several orders of magnitude in drain current is needed for a FET based on BTBT to exhibit an OFF state that is superior to a conventional device. If the threshold voltage is defined by requiring a certain drain current level (set by the dashed black line in Fig. 18) [63], it is apparent that only the devices with $d_{\rm ox} = 1$ nm and a low Fermi energy in the contacts provide an average S smaller than 60 mV/dec. Similar to SB-FETs (see the discussion previously), tunnel FETs are "contact switching" devices, meaning that in contrast to conventional-type devices, the gate oxide in tunnel FETs should be scaled down as much as possible in order to increase the tunneling probability. This implies different scaling rules for tunnel FETs, as will be briefly discussed hereinafter. Note that, in the present case, we did not take an increase of the effective bandgap due to vertical quantization into account [64], which is to first order justified since the main modification of the device characteristics when scaling $d_{\rm nw}$ to 5 nm stems from the enhanced gate control leading to an improved electrical behavior. However, for smaller $d_{\rm nw}$, the diameter dependence of E_g and $m^\star$ have to be taken into account [65].

In the case of $d_{\rm ox} = 3$ nm (dark gray line), S is smaller than 60 mV/dec only in a limited range of $\Delta\Phi$. It is interesting to see that with increasing Fermi energy in the contacts, the steep inverse subthreshold slope is lost (dotted black line with E_f^s) and one obtains $S \approx 50$ mV/dec. The reason for this is that, due to the large Fermi energy, the energetic window $\Delta\Phi$ in which carriers are injected into the channel now resides within the exponential tail of $f(E_f^s)$. As a result, such a tunnel FET behaves similar to a conventional MOSFET [66].

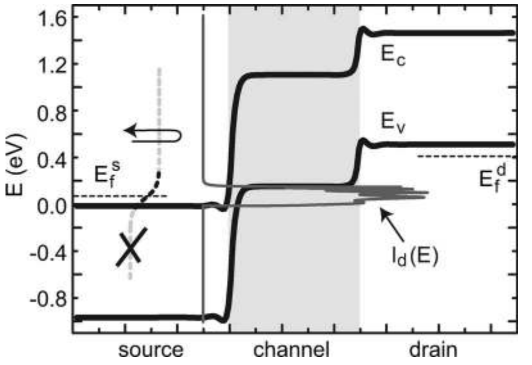

Fig. 19. Conduction and valence band profile of a T-NW-FET with thin $d_{\rm nw}$ and $d_{\rm ox}$ in the ON state. The gray line shows the current spectrum demonstrating the bandpass filter behavior as discussed in the text.

In case of a large tunneling probability and a rather small-source Fermi energy, S approaches $\ln(10)/q \cdot \Delta\Phi$, meaning that, in this case, the particular conduction and valence band profiles represent a bandpass filter effectively cutting off the high- and low-energy tails of the Fermi function. This bandpass filter behavior can be seen in Fig. 19, which shows simulated conduction and valence band profiles together with the current spectrum of a tunnel FET in the ON state. Looking at the current spectrum (gray line in Fig. 19), it becomes apparent that a significant current contribution stems exclusively from the energetic window between the valence band edge in the channel and the conduction band edge in the source contact, i.e., the bandgap in source and channel that acts as the bandpass filter mentioned earlier. Thus, in the tunnel FET, the injection of carriers occurs from an effectively "cooled" Fermi function, and therefore, the inverse subthreshold slopes steeper than 60 mV/dec are feasible.

C. *Scaling of Tunnel FETs*

In the present section, we want to address two important points related to the scaling of the channel length in tunnel FETs. First, it is often said that tunnel FETs exhibit less SCEs compared to conventional devices since the tunneling process only involves the source–channel interface. However, similar to conventional-type FETs, the n-p junctions at the contact-channel interfaces have a spatial extent which is on the order of λ [illustrated with the light-gray-shaded area in Fig. 20(a)]. For a tunnel FET to show steep inverse subthreshold slopes, it is necessary that the gate has a good electrostatic control to manipulate the bands one-to-one with changing gate voltage. This requires that the channel length must be significantly larger than λ in order to avoid a junction overlap which is the same requirement as for suppressing SCEs in a conventional-type MOSFET.

Fig. 20(a) and (b) shows conduction and valence band profiles in the case of a properly designed tunnel FET (a) and a device that exhibits SCEs (b). In the case (a), the channel

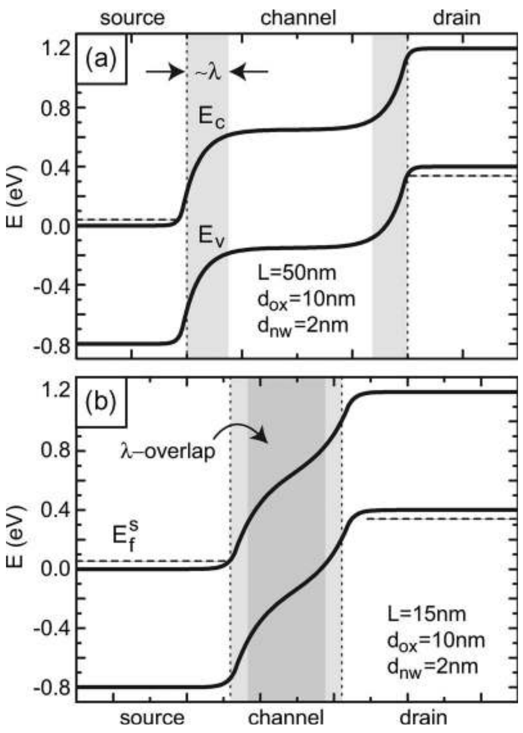

Fig. 20. Conduction and valence bands in a tunneling FET in the OFF state. (a) The case of a properly scaled long-channel device where the n-p and p-n junctions at the contact-channel interfaces do not overlap. (b) Short-channel tunnel transistor: In the present case, the junctions overlap, significantly leading to a loss of gate control.

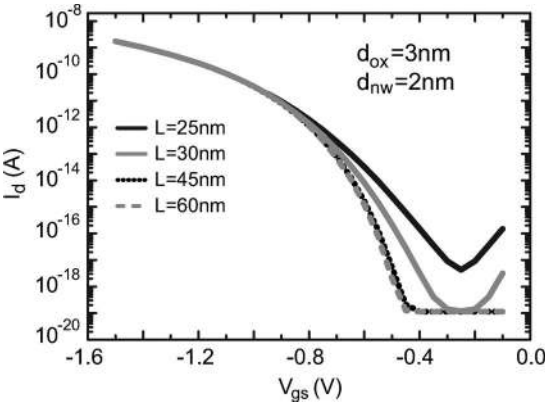

Fig. 21. Transfer characteristics of tunneling NW-FETs with different channel lengths. Devices with small channel length exhibit SCEs yielding larger inverse subthreshold slopes and OFF-state leakage.

length is significantly larger than the two n-p and p-n junctions (light-gray-shaded area) such that a good gate control of the bands in the channel area is obtained. In the device (b), on the other hand, the junctions significantly overlap (dark-gray-shaded area), leading to a potential profile in the channel that is, to a large extent, determined by the drain potential rather than the gate. As a result, device (b) exhibits SCEs leading to a much larger inverse subthreshold slope and drain-induced barrier thinning. Due to the n-i-p structure, however, a tunnel transistor that suffers from SCEs can still exhibit small OFF-state currents (if the device is not scaled to such small channel lengths that direct source-to-drain tunneling leads to an increase of the OFF-state current). The averaged inverse subthreshold slope, on the other hand, will in the case of SCEs be significantly larger than 60 mV/dec. Fig. 21 shows the transfer characteristics of tunnel FETs for different channel lengths; the smaller the channel lengths, the more pronounced SCEs appear. Obviously, tunnel FETs that are not properly scaled show an increase of the inverse subthreshold slope diminishing the major benefit of the tunnel FET architecture.

Up to now, we considered transport in the T-NW-FETs as being ballistic. We will now argue that this is very often justified unless the devices under investigation exhibit extremely long channel lengths. A tunnel FET is a contact-switching device that is very similar to an SB-FET. Hence, the same argument about the relevance of scattering applies in the present case: If the BTBT is the main scattering event, then scattering within the channel does not play a role anymore unless the channel is made sufficiently long. Again, the smaller the BTBT probability, the longer the channel has to be in order for the scattering in the channel to dominate. An estimate of the channel length required for the scattering transport in the channel to become dominant can be obtained as follows: The transmission function due to scattering for carriers flowing through the channel can be estimated to be $T_{\mathrm{scat}} \approx l_{\mathrm{scat}}/(l_{\mathrm{scat}} + L)$, where l_{scat} is the scattering mean free path [32], [67]. Then, the overall transmission function is given as

$$T_{\mathrm{tot}} = \frac{T_{\mathrm{WKB}} T_{\mathrm{scat}}}{T_{\mathrm{WKB}} + T_{\mathrm{scat}} - T_{\mathrm{WKB}} T_{\mathrm{scat}}} = \frac{1}{e^{\left(\frac{4\lambda\sqrt{2m^\star}E_{\mathrm{g}}^{3/2}}{3\hbar(E_g+\Delta\Phi)}\right)} + \frac{L}{l_{\mathrm{scat}}}}. \tag{13}$$

This means that scattering in the channel becomes significant only for minimum channel lengths $L_{\mathrm{min}} \geq l_{\mathrm{scat}} \exp(4\lambda\sqrt{2m^\star}E_g^{3/2}/(3\hbar(E_g + \Delta\Phi)))$. The exponential dependence of L_{min} on λ, on the other hand, shows that for a realistic device geometry, the minimum channel length can be rather long. In particular, if one considers planar tunnel FETs in SOI, for instance, the minimum channel length can easily be in a few micrometer range [68]. Therefore, scattering in tunnel FETs usually can be neglected. However, one has to keep in mind that this implies a deteriorated ON-state current due to a small BTBT probability.

D. Scaling Toward the QCL

The one-dimensionality of the T-NW-FET has an interesting consequence which makes a 1-D system very attractive for the realization of tunneling devices [14]. For realistic systems, the BTBT probability will always be smaller than unity, and hence, the on-current of a tunnel FET is deteriorated compared to a conventional-type transistor. However, the gate delay $\tau = C_g V_{\mathrm{dd}}/I_d$ is a much more appropriate measure to quantify intrinsic device performance. Assuming the long-channel case (i.e., $\lambda \ll L$), the gate capacitance is given by $C_g = C_{\mathrm{ox}} C_q/(C_{\mathrm{ox}} + C_q)$. For large enough V_{ds} (see above), C_q can be calculated using (3) together with the WKB approximation.

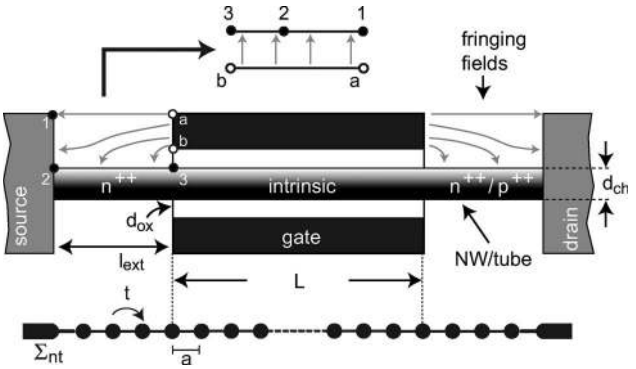

Fig. 22. Schematics of the simulated device structure. The effect of fringing fields is accounted for using conformal mapping.

Since T_{WKB} is an exponential, after differentiation, it turns out that $C_q \propto T_{\mathrm{WKB}}$

$$C_q \approx \frac{4\lambda\sqrt{2m^\star} E_g^{3/2}}{3\hbar(E_{\mathrm{g}}+\Delta\Phi)^2} T_{\mathrm{WKB}} \int dE D(E)\left(1-f\left(E-E_f^s\right)\right) \tag{14}$$

$$+\, qT_{\mathrm{WKB}} \frac{\partial}{\partial \Phi_f^0} \int dE D(E)\left(1-f\left(E-E_f^s\right)\right) \tag{15}$$

where, now, $D(E)$ is the 1-D DOS. We have discussed that in 1-D systems, the QCL can be reached where $C_{\mathrm{ox}} \gg C_q$ due to the decreasing DOS. In a T-NW-FET, C_q will be even smaller than in a conventional NW-FET due to the proportionality of C_q to T_{WKB}. Note that this is only true as long as E_f^d is larger than the valence band in the channel (see [14] for a detailed discussion.). As a result, in a wrap-gate T-NW-FET with thin gate dielectric, it is very likely that the QCL is reached and thus $C_g \approx C_q$ (for a detailed study on the scaling of 1-D FETs toward the QCL, see [17]). At the same time, $I_d \propto T_{\mathrm{WKB}}$ [cf. (11)], and therefore, the gate delay τ becomes independent of T_{WKB}. **This means that to first order the presence of the BTBT barrier** ***does not*** **deteriorate the ON state of 1-D tunnel FETs as measured by the gate delay**. Consequently, 1-D systems such as NWs and carbon nanotubes are ideally suited for the realization of tunnel FETs since they allow combining a high ON-state performance with steep subthreshold swings.

Next, we study the effect of scaling tunnel FETs toward the QCL on their ON-state performance using simulations [69]. To this end, we employ the model presented in Section III. Although this model considers a semiconductor with a direct bandgap, the main dependences on the geometrical parameters of the device, the effective mass, and the bandgap remain practically the same [62]. Phonons, however, play an important role in the OFF state of tunnel FETs as was pointed out by Koswatta *et al.* [71]. Since, in the following, we focus on the ON-state performance, the impact of phonons is neglected. For a proper comparison of conventional NW-FETs and T-NW-FETs, it is important to account for the fringing fields in the source/drain extensions. We therefore simulated the NW-FET structure shown in Fig. 22 as n-i-n and n-i-p device. In order to keep the computational burden as small as possible, (1) is used to describe the electrostatics of the devices under consideration.

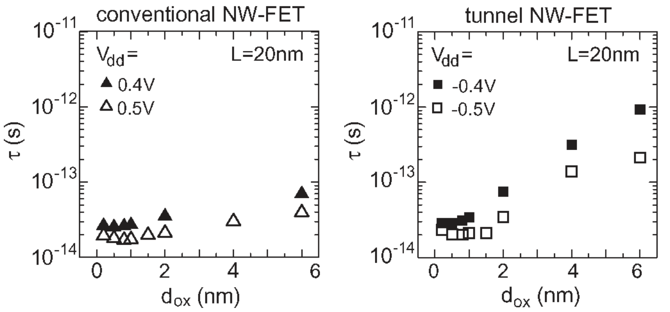

Fig. 23. Gate delay of a conventional NW-FET and T-NW-FET as a function of d_{ox}. Simulations were carried out with as follows: $E_{\mathrm{f}}^{s,d} = 0.1$ eV, $m^\star = 0.1\, m_0$, and $d_{\mathrm{ch}} = 3$ nm [70].

A conformal mapping technique is used to take the effect of the gate fringing fields on the source/drain extensions into account. As shown in Fig. 22, the area of the source/drain extension is mapped onto a parallel-plate capacitor. Then, transforming back the field lines allows obtaining a spatially dependent $d_{\mathrm{ox}}(x)$ in the source/drain extension that is used to compute λ in (1) [71].

Simulations were performed for a constant channel length of $L = 20$ nm and different d_{ox} (all other parameters are given in the caption of Fig. 23). In both cases, conventional-type NW-FET and T-NW-FET, the V_{dd} window was shifted along the I_d–V_{gs} curves in order to obtain the smallest τ and, at the same time, a minimum on/off current ratio of five orders of magnitude. Fig. 23 shows the extracted values of τ for the conventional NW-FET (left) and for the T-NW-FET (right). As expected, in the case of conventional NW-FETs, τ only slightly depends on d_{ox} since both current and capacitance scale equally with the oxide thickness. In the T-NW-FET, however, τ is almost constant only for the thinnest d_{ox}. For thicker gate oxides, τ shows a significant dependence on d_{ox} leading to a substantial performance loss. For the thinnest oxides, the device is in the QCL and first shows the weak dependence on d_{ox} expected from the discussion earlier. Second, and more importantly, the T-NW-FET exhibits the same ON-state performance in the QCL as the conventional NW-FET as measured by τ, although the ON-state current is about one order of magnitude lower (not shown here).

In summary, our simulation support that improved the OFF-state performance without loss of ON-state performance makes BTBT devices the superior choice of transistor structure in NW devices.

E. Tunnel FETs—Experimental Results

In a first attempt to realize tunnel FETs, we fabricated lateral SiNW devices with *in situ* doped source and drain contacts. To this end, SiNWs with a diameter of 60 nm were grown by CVD at a wafer temperature of 450 °C and a total pressure of 25 torr using silane $(\mathrm{SiH_4})$ diluted in Ar/He/H_2 to a partial pressure of 500 mtorr. The wires consist of a 2-μm p-doped segment, a 1-μm intrinsic segment, and a 2-μm n^+-segment. Doping was realized using phosphine as n-type dopant and diborane as the p-type dopant (see Section IV). The addition of B_2H_6 to SiH_4 lowers the thermal stability of the gas mixture and leads to a nonspecific deposition resulting in a p-doped shell

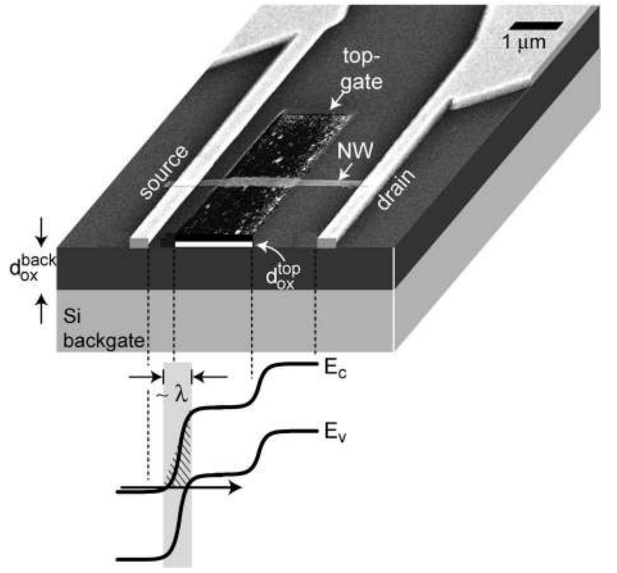

Fig. 24. SEM image of a Si T-NW-FET. The top-gate metal is Al; the bottom- and top-gate oxides ($d_{\mathrm{ox}}^{\mathrm{back}}$ and $d_{\mathrm{ox}}^{\mathrm{top}}$) are 100 and 20 nm thick, respectively. Below, the band diagram throughout the device is shown under reverse bias, i.e., the source is on ground and a negative V_{ds} is applied. The gray-shaded area is the source side p-n junction where BTBT occurs [73].

around the SiNW. To avoid this growth was started with the p-segment using a gas phase ratio of 1150:1 (Si:B). At these conditions, a thin p-doped shell (≈3 nm) is still present on the p-segment preventing an accurate determination of the resistivity. The fairly low gas phase ratio was used to make the doping concentration in the p-segment lower than in the n$^+$-segment to suppress ambipolar behavior of the tunnel FET [72]. For device fabrication, the wires were mechanically removed and transferred to a highly doped Si wafer with a 100-nm-thick top SiO$_2$ layer serving as a back gate and gate dielectric, respectively. Ti and Au metal was used as an electrode material. The entire device was thereafter covered with 20-nm SiO$_2$, and an Al top gate was added. The top gate overlaps the doped source/drain contacts in order to ensure that the gate has optimum control over the entire intrinsic region; test devices with n-type doping throughout the NW showed that at the dimensions considered here, the gate has no impact on the n-doped source contact. This is important since, in the present case, BTBT occurs at the n-doped—intrinsic interface (for more details, see [73]).

A combined scanning electron micrograph and schematic drawing showing the device layout is shown in Fig. 24. At the bottom, the conduction/valence band profiles are shown in the device's ON state. Fig. 25 shows the transfer characteristics for a reversed biased (i.e., the p-segment is biased negatively) device in the case of a back gate (a) and top gate (b). We will first focus on the device with the back gate in use. A strong dependence of the drain current on gate voltage is observed with several orders of magnitude between ON- and OFF-state currents. Measurements of the devices under forward bias (not shown here), however, show a very weak dependence of the drain current flowing through the device on the gate voltage but, at the same time, show a strong dependence on V_{ds}, typical of a forward bias diode. These two facts indicate that BTBT occurs in our device and is responsible for the switching in reverse bias. Note that the OFF-state leakage between $V_{\mathrm{gs}} = 5$ V and $V_{\mathrm{gs}} = 7$ V is entirely due to leakage currents through the bottom-gate oxide. In the V_{gs} range where the current rises ($V_{\mathrm{gs}} < 5$ V), on the other hand, the gate leakage current does not affect the behavior of the characteristics. From the forward biased measurements, a parasitic series resistance in the 10^9 Ω range is observed which limits the current drive capability in the device's ON state. This series resistance is likely due to the low doping level of the p-type segments. Increasing the p-doping concentration potentially allows obtaining significantly larger current levels.

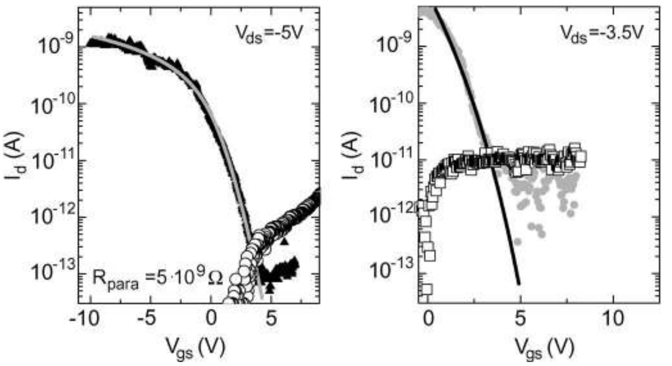

Fig. 25. (a) Transfer characteristics of the T-NW-FET using the back gate. The gray solid line is calculated from a WKB approximation. The inverse subthreshold slope is measured to be $S = 1200$ mV/dec. (b) Transfer characteristics of the same device after processing a top gate separated from the channel by 20-nm PECVD SiO$_2$. In this case, S decreased to 800 mV/dec. The black solid line is calculated using the WKB approximation [73]. The open symbols in (a) and (b) display the gate current showing significant gate leakage in the present devices.

Next, we focus on the OFF state of the devices. The inverse subthreshold slope of the T-NW-FETs using the back gate [Fig. 25(a)] lies between $S = 1200-1500$ mV/dec, much larger than 60 mV/dec expected in a conventional NW-FET. The drain current can be approximately calculated using (11). To do so, we consider the NW as a rolled-up 2-D system which is justified in the present case due to the relatively large NW diameter of 60 nm. Averaging (11) over transverse k-vectors then yields[5]

$$I_d \approx \frac{16q\sqrt{m^\star}}{3h^2} W \left(-q(V_{\mathrm{gs}}+V_{\mathrm{th}})\right)^{\frac{3}{2}} \tag{16}$$

$$\exp\left(-\frac{4\lambda\sqrt{2m^\star E_g^{3/2}}}{3h\left(E_g - q(V_{\mathrm{gs}}+V_{\mathrm{th}})\right)}\right) \tag{17}$$

where W is the width of the device, i.e., the circumference of the NW [72]. Scattering in the channel can be neglected here as has been argued earlier. Note that there is no V_{ds} dependence since we consider the transistor to be in the current saturation regime. If, in addition, we take the large series resistance into account, we can very well reproduce the experimentally measured I_d–V_{gs} [solid gray line in Fig. 25(a)]. In particular, the large inverse subthreshold slope is exactly what one would expect from such a device (note that in order to obtain this result, we only had to adjust the threshold voltage to match experimental data with the analytical calculation).

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[5] The source/drain Fermi functions are approximated with step functions in the present case.

As already mentioned previously, scaling down d_{ox} should result in steeper inverse subthreshold slopes and higher on-currents. To demonstrate this, a top gate was added to the devices separated from the NW channel by a 20-nm-thick PECVD SiO_2 gate dielectric as described earlier. Although the PECVD is not ideal in terms of leakage currents, it was used in order to prevent any dopant diffusion in the NWs that might occur during an oxidation at elevated temperatures and to ensure that no other thermally activated mechanism obscures the impact of a decreased d_{ox}. In Fig. 25, the transfer characteristics of the same device are plotted for both back gate (a), as discussed earlier, and top gate (b). We observe that the ON-state current, indeed, increases markedly. This increase is attributed in part to a decreased parasitic contact resistance due to annealing at 300 °C during the PECVD growth and to the improved gate control of the top gate. More importantly, the inverse subthreshold slope decreases to 800 mV/dec. By using again the analytical calculation based upon (16), we obtain the same improvement as observed in the experiment [solid line in Fig. 25(b)].

Decreasing the parasitic resistances by increasing the dopant concentration in the p-segment and eliminating contact resistances as well as decreasing the NW diameter and the gate dielectric thickness will allow obtaining substantially larger current levels. Furthermore, extrapolating the analytical calculation to smaller NW diameters and gate oxide thickness in a wrap-gate architecture, we find that for feasible oxide thickness and NW diameter of $d_{\mathrm{ox}} \leq 2$ nm and $d_{\mathrm{nw}} \leq 10$ nm in a wrap-gate architecture, tunnel Si NW-FETs exhibiting an S smaller than 60 mV/dec in a limited V_{gs}-range can be obtained.

IX. CONCLUSION

NW-FETs represent a relatively new class of FET devices exhibiting very promising electrical characteristics as well as new and interesting device physics aspects. In this paper, we studied the electronic transport in four different application-relevant NW-FET architectures. As it turned out, the characteristics of all four device concepts strongly depend on the NW diameter. Scaling down d_{nw} results in an increasing gate control over the potential within the channel which, in turn, enables ultimately scaled conventional FETs. In the case of SB-FETs, IMOS devices and tunnel FETs employing an NW with small diameter yield additional benefits for the device functionality: A substantially increased injection of carriers from the source into the channel leads to significantly steeper inverse subthreshold slopes and improved on-currents in SB-NW-FETs. In addition, scaling down the NW diameter results in substantial improvements of the current drive capability of T-NW-FETs and potentially enables the realization of FET devices with an inverse subthreshold slope steeper than 60 mV/dec. First experimental results in this direction were presented in this paper, too. Furthermore, in wrap-gate IMOS devices based on thin NWs, the vertical electric fields are lowered, resulting in a reduction of hot carrier degradation. Vertical IMOS NW-FETs have been demonstrated that exhibit very steep turn-on characteristics but, at the same time, no indication of hot carrier degradation. Apart from these pure geometrical effects, 1-D transport occurs in NWs of sufficiently thin diameter. In a 1-D system, on the other hand, the QCL becomes attainable, which renders the ON-state performance of T-NW-FETs as measured by the gate delay to be similar to conventional NW-FETs.

As a result, NWs appear to be a premier choice for future nanoelectronics applications since they enable a continuation of device scaling and, at the same time, provide additional benefits for device functionality and performance not accessible in planar FET architectures.

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