# THE END OF CMOS SCALING

## Toward the Introduction of New Materials and Structural Changes to Improve MOSFET Performance

*Thomas Skotnicki, James A. Hutchby, Tsu-Jae King, H.-S. Philip Wong, and Frederic Boeuf*




The rapid cadence of metal-oxide semiconductor field-effect transistor (MOSFET) scaling, as seen in the new *2003 International Technology Roadmap for Semiconductors* (ITRS) [1], is accelerating introduction of new technologies to extend complementary MOS (CMOS) down to, and perhaps beyond, the 22-nm node. This acceleration simultaneously requires the industry to intensify research on two highly challenging thrusts: one is scaling CMOS into an increasingly difficult manufacturing domain well below the 90-nm node for high performance (HP), low operating power (LOP), and low standby power (LSTP) applications, and the other is an exciting opportunity to invent fundamentally new approaches to information and signal processing to sustain functional scaling beyond the domain of CMOS. This article is focused on scaling CMOS to its fundamental limits, determined by manufacturing, physics, and costs using new materials and nonclassical structures. The companion articles in this issue address possible approaches for extending information processing into new realms of performance and application using new memory devices, logic devices, and architectures. The primary goal of these articles is to stimulate invention and research leading to feasibility demonstration for one or more roadmap-extending concepts.

The following provides a brief introduction to each of the new nonclassical CMOS structures. This is followed by a presentation of one scenario for introduction of new structural changes to the MOSFET to scale CMOS to the end of the ITRS. A brief review of electrostatic scaling of a MOSFET necessary to manage short channel effects (SCEs) at the most advanced technology nodes is also provided.

## NONCLASSICAL CMOS STRUCTURES

Nonclassical CMOS includes those advanced MOSFET structures shown in Table 1(a) and (b), which, combined with material enhancements, such as new gate stack materials, provides a path to scaling CMOS to the end of the roadmap. For digital applications, scaling challenges include controlling leakage currents and short-channel effects, increasing drain saturation current while reducing the power supply voltage, and maintaining control of device parameters (e.g., threshold voltage and leakage current) across the chip and from chip to chip. For analog/mixed-signal/RF applications, the challenges additionally include sustaining linearity, low noise figure, high power-added efficiency, and good transistor matching.

The industrial and academic communities are pursuing two avenues to meeting these challenges—new materials and new transistor structures. New materials include those used in the gate stack (high-$\kappa$ dielectrics and electrode materials), those used in the conducting channel that

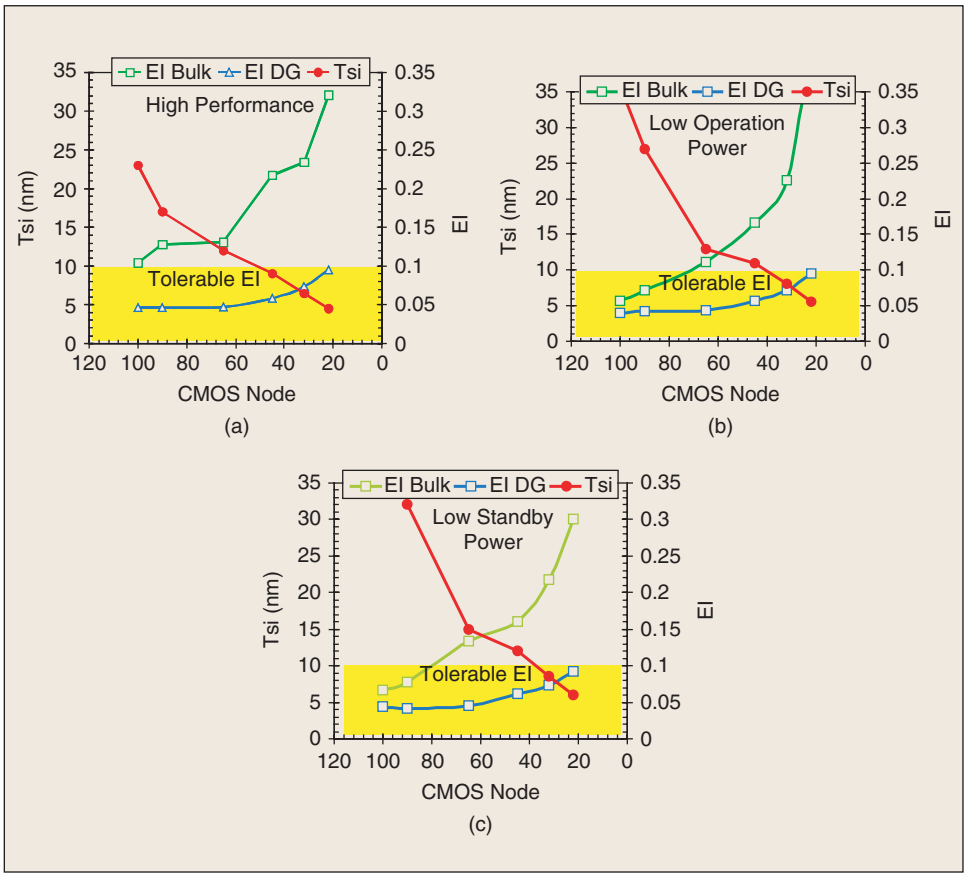

8755-3996/05/$20.00 ©2005 IEEE

have improved carrier transport properties, as well as new materials used in the source/drain regions with reduced resistance and improved carrier injection properties. New transistor structures seek to improve the electrostatics of the MOSFET, provide a platform for introduction of new materials, and accommodate the integration needs of new materials. The following provides a brief introduction and overview to each of these nonclassical CMOS structures given in Table 1(a) and (b).

Transport-enhanced MOSFETs [2]–[16] are those structures for which increased transistor drive current for improved circuit performance can be achieved by enhancing the average velocity of carriers in the channel. Approaches to enhancing transport include mechanically straining the channel layer to enhance carrier mobility and velocity, and employing alternative channel materials such as silicon-germanium, germanium, or III-V compound semiconductors with electron and hole mobilities and velocities higher than those in silicon. A judicious choice of crystal orientation and current transport direction may also provide transport enhancement [17]. However, an important issue is how to fabricate transport enhanced channel layers (such as a strained Si layer) in several of the nonclassical CMOS transistor structures [e.g., the multiple gate structures discussed in Table 1(b)]. Researchers have recently demonstrated that a strained Si-on-insulator (SOI) substrate technology can be used to combine the advantages of the ultra-thin body (UTB) structure and enhanced carrier transport [18]–[20].

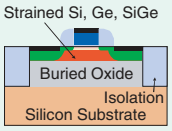
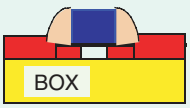
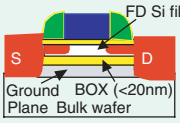
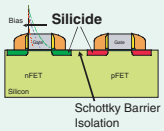
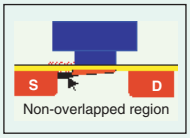
The UTB SOI MOSFET [21]–[31] consists of a very thin ($t_{Si} \leq 10$ nm), fully depleted (FD) transistor body to ensure good electrostatic control of the channel by the gate in the off state. Typically, the ratio of the channel length to the channel thickness will be $\geq 3$. Therefore, an extremely thin ($t_{Si} < 4$ nm) Si channel is required to scale CMOS to the 22-nm node. The use of a lightly doped or undoped body provides immunity to $V_t$ variations due to statistical dopant fluctuations, as well as enhanced carrier mobilities for higher transistor drive current. The localized and ultra-thin buried oxide (BOX) FET [32]–[40] is an UTB SOI-like FET in which a thin Si channel is locally isolated from the bulk-Si substrate by a thin (10–30 nm) buried dielectric layer. This structure combines the best features of the classical MOSFET (e.g., deep source/drain contact regions for low parasitic resistance) with the best features of SOI technology (improved electrostatics). The increased capacitive coupling between the source, drain, and channel with the conducting substrate through the ultra-thin BOX has the potential of reducing the speed of the device, and improving it's electrostatic integrity. The former may be traded against the latter by reducing the channel doping, which eventually leads to moderately improved speed for a constant $I_{off}$.

Engineering the source/drain is becoming critically important to maintaining the source and drain resistance to be a reasonable fraction (~10%) of the channel resistance. Consequently, a new category of source/drain engineered MOSFETs [41]–[52] is introduced to address this issue. Two sub-category structures are described for providing engineered source/drain structures. First is the Schottky source/drain structure [41]–[48]. In this case, the use of metallic source and drain electrodes minimizes parasitic series resistance and eliminates the need for ultra-shallow p–n junctions. Metals or silicides that form low (near zero) Schottky barrier heights in contact with silicon (i.e., a low-work-function metal for NMOS, and a high-work-function metal for PMOS) are required to minimize contact resistance and maximize transistor drive current in the on state. A UTB is needed to provide low leakage in the off state. Second is the reduced fringing/overlap gate FET [49]–[52]. As MOSFET scaling continues, the parasitic




*1. Estimation of electrostatic integrity (EI) for bulk and double-gate FETs.*

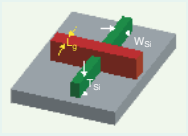
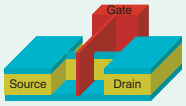
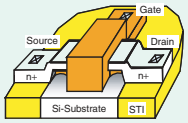
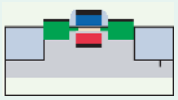
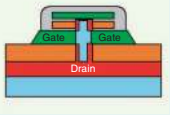
**Table 1(a). Single-gate Nonclassical CMOS Technologies.**

| Device | Transport-Enhanced MOSFETs | UTB SOI MOSFETs | | Source/Drain Engineered MOSFETs | |
|---|---|---|---|---|---|
| |  |  |  |  |  |
| Concept | Strained Si, Ge, SiGe, SiGeC or other semiconductor; on bulk or SOI | Fully depleted SOI with body thinner than 10 nm | Ultra-thin channel and localized ultra-thin BOX | Schottky source/drain | Non-overlapped S/D extensions on bulk, SOI, or DG devices |
| Application/Driver | HP CMOS [2] | HP, LOP, and LSTP CMOS [2] | HP, LOP, and LSTP CMOS [2] | HP CMOS [2] | HP, LOP, and LSTP CMOS [2] |
| Advantages | • High mobility | • Improved subthreshold slope<br>• No floating body<br>• Potentially lower $E_{eff}$ | • SOI-like structure on bulk<br>• Shallow junction by geometry<br>• Junction silicidation as on bulk<br>• Improved S-slope and SCE | • Low source/drain resistance | • Reduced SCE and DIBL<br>• Reduced parasitic gate capacitance |
| Particular Strength | • High mobility without change in device architecture | • Low diode leakage<br>• Low junction capacitance<br>• No significant change in design with respect to bulk | • Quasi-DG operation due to ground plane effect enabled by the ultra thin BOX<br>• Bulk compatible | • No need for abrupt S/D doping or activation | • Very low gate capacitance |
| Potential Weakness | • Material defects and diode leakage (only for bulk)<br>• Process compatibility and thermal budget<br>• Operating temperature | • Very thin silicon required with low defect density<br>• $V_{th}$ adjustment difficult<br>• Selective epi required for elevated S/D | • Ground plane capacitance<br>• Selective epi required for channel and S/D | • Ultra-thin SOI required<br>• NFET silicide material not readily available<br>• Parasitic potential barrier | • High source/drain resistance<br>• Reliability<br>• Advantageous only for very short devices |
| Scaling Issues | Bandgap usually smaller than Si | Control of Si film thickness | Process becomes easier with Lg down-scaling (shorter tunnel) | No particular scaling issue | Sensitivity to $L_g$ variation |
| Design Challenges | Compact model needed | None | None | Compact model needed | Compact model needed |
| Gain/Loss in Layout compared to Bulk | No difference | No difference | No difference | No difference | No difference |
| Impact on $I_{on}/I_{off}$ compared to Bulk | • Improved by 20–30% (from MASTAR supposing $\mu_{eff}$X2) | • Improved by 15–20% (from MASTAR supposing $E_{eff}/2$ and S = 75 mV/decade) | • Improved by 15–20% (from MASTAR supposing $E_{eff}/2$ and S = 75 mV/decade) | • Improved by 10–15% (from MASTAR supposing $R_{series} = 0$) | • Both shifted to lower values |
| Impact on CV/I compared to Bulk | • Lowered by 15–20% (from MASTAR supposing $\mu_{eff}$X2) | • Lowered by 10–15% (from MASTAR supposing $E_{eff}/2$ and S = 75 mV/decade) | • Lowered by 10–15% (from MASTAR supposing $E_{eff}/2$ and S = 75 mV/decade) | • Lowered by 10–15% (from MASTAR supposing $R_{series} = 0$) | • Constancy or gain due to lower gate capacitance |
| Analog Suitability $G_m/G_d$ advantage compared to Bulk | Not clear | Potential for slight improvement | Potential for slight improvement | Not clear | Not clear |

capacitance between the gate and source/drain detrimentally affects circuit performance, and its impact becomes more significant as the gate length is scaled down. For gate lengths below ~20 nm, transistor optimization for peak circuit performance within leakage current constraints will likely dictate a structure wherein the gate electrode does not overlap the source or drain to minimize the effect of parasitic fringing/overlap capacitance. Due to lengthening of its electrical channel, the nonoverlapped gate structure does not require ultra-shallow source/drain junctions in order to provide good control of short-channel effects. Also, the increase of source/drain resistance usually expected for the nonoverlap transistor is reduced with decreasing gate length, thus providing a new optimization paradigm for extremely short devices.

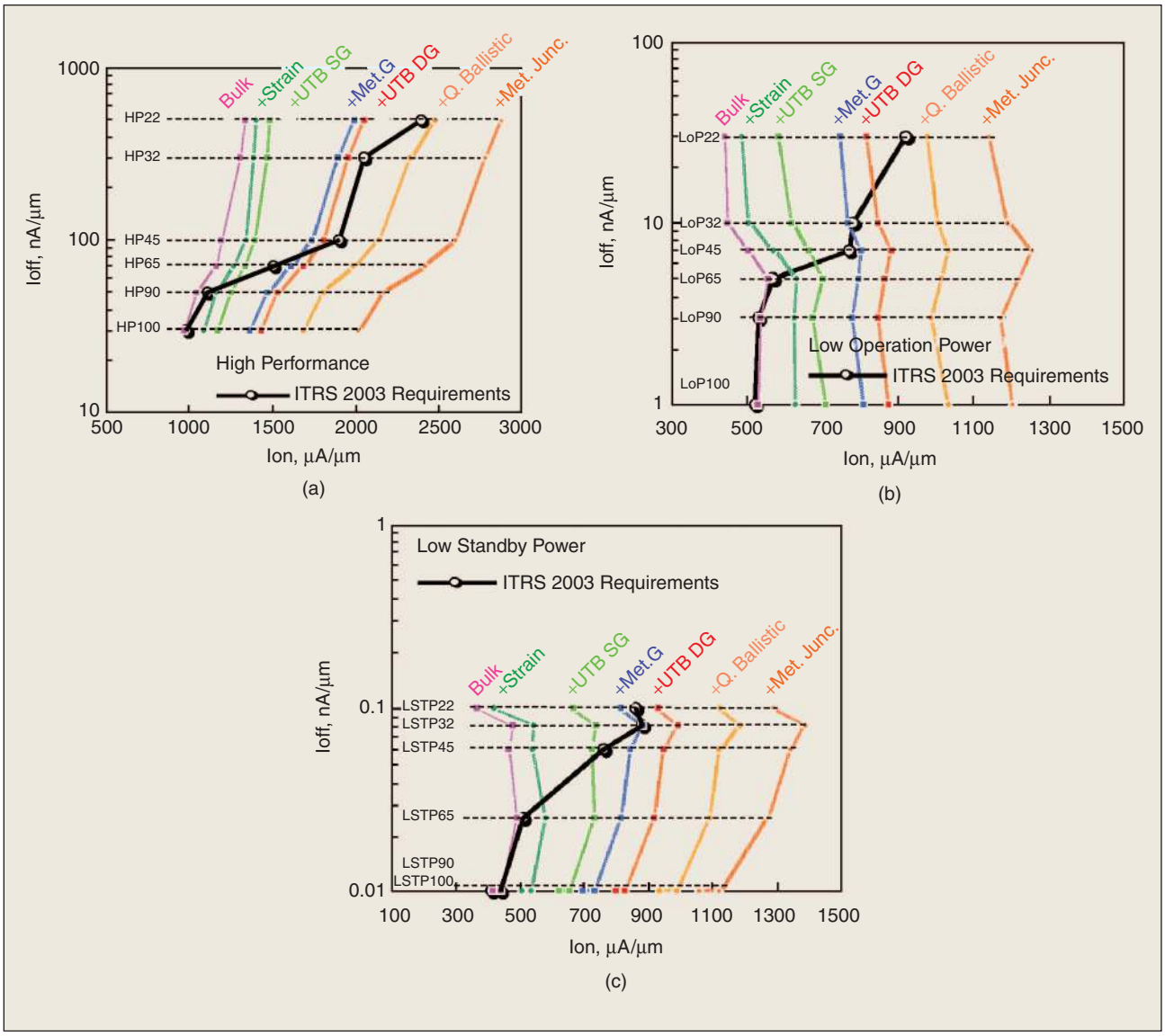
As illustrated in Table 1(b) and described in the following, a variety of multiple-gate nonclassical CMOS structures [53]–[92] have been proposed and demonstrated to help manage electrostatic integrity (i.e., SCEs) in ultra scaled CMOS structures. In the first of these structures, the $N$-gate ($N > 2$) MOSFET [53]–[59], current flows horizontally (parallel to the plane of the substrate) between the source and drain along

**Table 1(b). Multiple-gate Nonclassical CMOS Technologies.**

| | Multiple Gate MOSFETs | | | | |
|---|---|---|---|---|---|
| | N-Gate ($N > 2$) | | Double-gate | | |
| Device |  |  |  |  |  |
| Concept | Tied gates (number of channels >2) | Tied gates, side-wall conduction | Tied gates planar conduction | Independently switched gates, planar conduction | Vertical conduction |
| Application/Driver | HP, LOP, and LSTP CMOS [2] | HP, LOP, and LSTP CMOS [2] | HP, LOP, and LSTP CMOS [2] | LOP and LSTP CMOS [2] | HP, LOP, and LSTP CMOS [2] |
| Advantages | • Higher drive current<br>• 2 × thicker fin allowed | • Higher drive current<br>• Improved subthreshold slope<br>• Improved short channel effect | • Higher drive current<br>• Improved subthreshold slope<br>• Improved short channel effect | • Improved short channel effect | • Potential for 3D integration |
| Particular Strength | • Thicker Si body possible | • Relatively easy process integration | • Process compatible with bulk and on bulk wafers<br>• Very good control of silicon film thickness | • Electrically (statically or dynamically) adjustable threshold voltage | • Lithography independent $L_g$ |
| Potential weakness | • Limited device width<br>• Corner effect | • Fin thickness less than the gate length<br>• Fin shape and aspect ratio | • Width limited to <1 $\mu$m | • Difficult integration<br>• Back-gate capacitance<br>• Degraded subthreshold slope | • Junction profiling difficult<br>• Process integration difficult<br>• Parasitic capacitance<br>• Single-gate length |
| Scaling Issues | • Sub-lithographic fin thickness required | • Sub-lithographic fin thickness required | • Bottom gate larger than top gate | • Gate alignment | • Si vertical channel film thickness |
| Design Challenges | • Fin width discretization | • Fin width discretization | • Modified layout | • New device layout | • New device layout |
| Gain/Loss in Layout compared to Bulk | • No difference | • No difference | • No difference | • No difference | • Up to 30% gain in layout density |
| Advantage in $I_{on}/I_{off}$ compared to Bulk | • Improved by 20–30% (from MASTAR assuming $E_{eff}/2$ and S = 65 V/decade) | • Improved by 20–30% (from MASTAR assuming $E_{eff}/2$ and S = 65 V/decade) | • Improved by 20–30% (from MASTAR assuming $E_{eff}/2$ and S = 65 V/decade) | • Potential for improvement | • Improved by 20–30% (from MASTAR assuming $E_{eff}/2$ and S = 65 V/decade) |
| Advantage in CV/I compared to Bulk | • Lowered by 15–20% (from MASTAR assuming $E_{eff}/2$ and S = 65 V/decade) | • Lowered by 15–20% (from MASTAR assuming $E_{eff}/2$ and S = 65 V/decade) | • Lowered by 15–20% (from MASTAR assuming $E_{eff}/2$ and S = 65 V/decade) | • Potential for improvement | • Lowered by 15–20% (from MASTAR assuming $E_{eff}/2$ and S = 65 V/decade) |
| Analog Suitability $G_m/G_d$ advantage compared to Bulk | • Potential for improvement | • Potential for improvement | • Potential for improvement | • Potential for improvement | • Potential for improvement |

vertical channel surfaces, as well as one or more horizontal channel surfaces. The large number of gates provides for improved electrostatic control of the channel, so that the Si body thickness and width can be larger than for the UTB SOI and double-gate FET structures, respectively. The gate electrodes are formed from a single deposited gate layer and are defined lithographically. They are tied together electrically and are self-aligned with each other as well as the source/drain regions. The principal advantage of the structure resides in the relaxation of the needs on the thinness of the Si body or the vertical fin. The challenge is in slightly poorer electrostatic integrity than with double-gate structures, particularly in the corner regions of the channel.

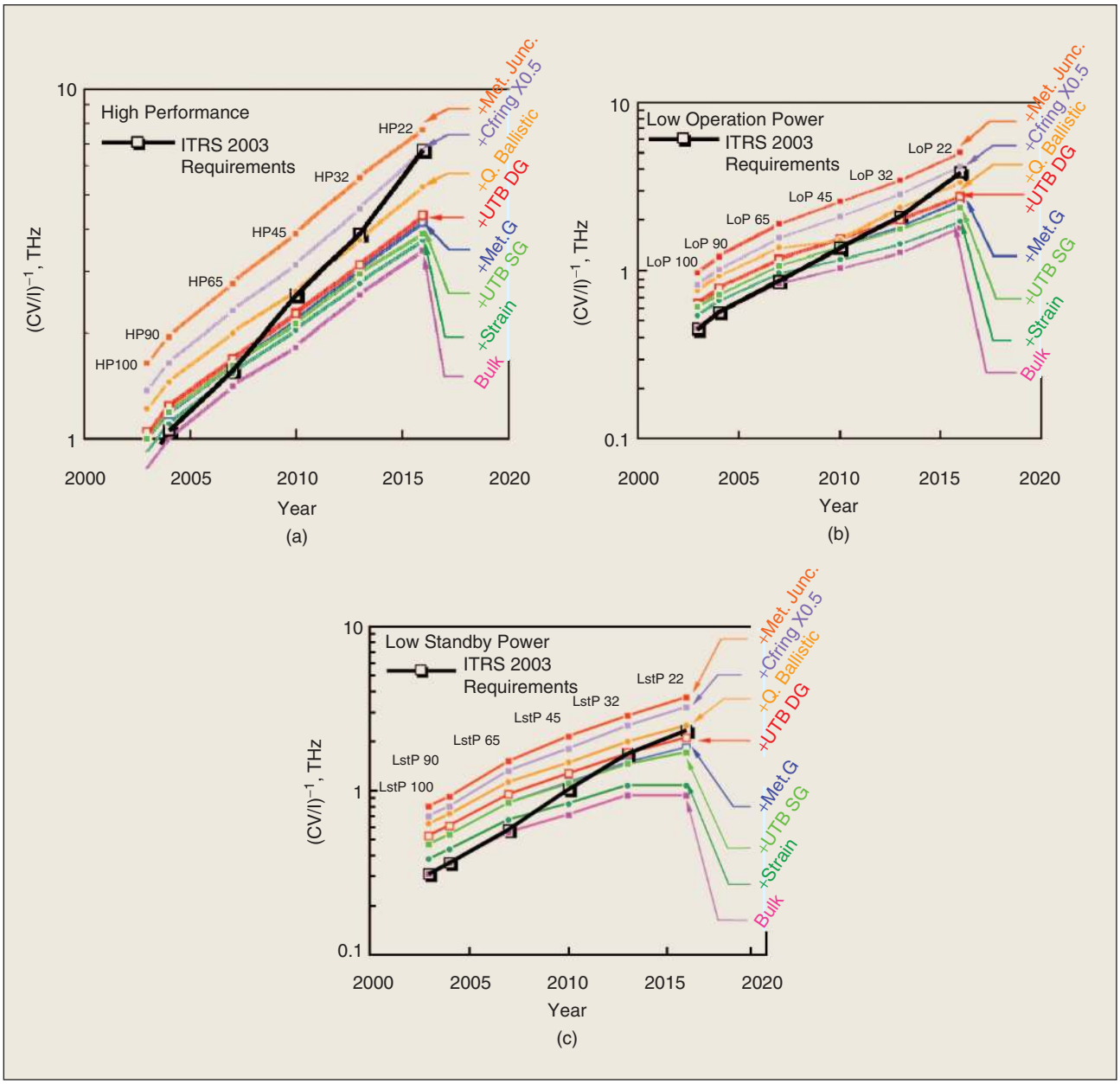
Several double-gate MOSFET structures [60]–[90] have been proposed to further improve engineering of the channel electrostatics and, in some cases, to provide independent control of two isolated gates for low-power and, perhaps, mixed-signal applications. Four typical double-gate structures are described in the following. First is the tied double-gate, sidewall conduction structure [60]–[71]. This is a double-gate transistor structure in which current flows horizontally (parallel to the plane of the substrate) between the source and drain along opposite vertical channel surfaces. The width of the vertical silicon fin is narrow (smaller than the channel length) to provide adequate control of short-channel effects. A lithographically defined gate straddles the fin, forming self-aligned, electrically connected gate electrodes along the sidewalls of the fin. The principal advantage with this structure is the planar bulk-like layout and process. In fact, this structure can be implemented on bulk Si substrates [44]. The major challenge is with fabrication of thin fins that need to be a fraction (one third to one half) of the gate length, thus requiring sublithographic techniques.




*2. Impact of the technology boosters on HP, LOP, and LSTP CMOS roadmaps in terms of $I_{on}$ : $I_{off}$ ratio. MASTAR calculation with translation of technology boosters according to Table 2.*

The second structure is the tied double-gate planar FET [72]–[78]. In this structure, current flows horizontally (parallel to the plane of the substrate) between the source and drain along opposite horizontal channel surfaces. The top and bottom gate electrodes are deposited in the same step and are defined lithographically. They may or may not be self-aligned to each other, and are electrically connected to one another. The source/drain regions are typically self-aligned to the top gate electrode. The principal advantages of this structure reside in the potential simplicity of the process (closest to bulk planar process) and in the compactness of the layout (same as for bulk planar) as well as in its compatibility with bulk layout (no need for redesigning libraries). It is also important that the channel thickness is determined by epitaxy, rather than etching, and, thus, is very well controlled. The challenge resides in the doping of the poly in the bottom gate (shadowed by the channel), but this problem disappears automatically when switching to a metal-like gate electrode. Another major challenge is in the fabrication process, particularly for those structures requiring alignment of the top and bottom gate electrodes.

The third structure is the independently switched double-gate (ground-plane) FET [79]–[84]. This structure is similar to the tied double-gate planar FET, except that the top and bottom gate electrodes are electrically isolated to provide for independent biasing of the two gates. The top gate is typically used to switch the transistor on and off, while the bottom gate is used for dynamic (or static) $V_t$ adjustment. The principal advantage is in the very low $I_{off}$ this structure offers. The disadvantage is in rather poor subthreshold behavior and in the relaxed layout. An independently switched double-gate transistor can also be implemented in a vertical structure by disconnecting the gates of the double-gate, sidewall conduction structure by chemical mechanical polishing [80].




*3. Impact of the technology boosters on HP, LOP, and LSTP CMOS roadmaps in terms of device intrinsic speed (f=1/(CV/I)). MASTAR calculation with translation of technology boosters according to Table 2.*

The fourth structure is the "vertical conduction" transistor [85]–[92]. In this case, current flows between the source and drain in the vertical direction (orthogonal to the plane of the substrate) along two or more vertical channel surfaces. The gate length, hence the channel length, is defined by the thickness of the single deposited gate layer, rather than by a lithographic step. The gate electrodes are electrically connected, and are vertically self-aligned with each other and the diffused source/drain extension regions. The principal advantage with this structure is that the channel length is defined by epitaxy rather than by lithography (possibility of very short and well-controlled channels). The disadvantage is this structure requires a challenging process and the layout is different from that for bulk transistors.

## AN EMERGING NONCLASSICAL CMOS TECHNOLOGY ROADMAP SCENARIO

As investments relative to the majority of the nonclassical CMOS structures presented previously may be very large, it would be quite helpful to assess the gain in performance they promise. This knowledge will likely contribute to the technical justification and validity of the strategic R&D decisions that will be required to develop and implement one or more of these options. For many reasons, this is a very difficult task. First, the properties of new materials may provide some surprises. For one example, knowledge of these material properties is often based on isolated large-volume samples, whereas, in CMOS, applications of very thin and low-volume layers are most common. Second, integration of these materials into a CMOS process may

**Table 2. Technology Performance Boosters.**

| Nature | Technology Performance Boosters: Translation for $I_{on}$ | Translation for $C_{gate}$ | Translation for $I_{off}$ | MASTAR Default Value |
|---|---|---|---|---|
| Strained-Si, Ge, etc. | $\mu_{eff} \times B_{mob}$ | NA | NA | Strained-Si, $B_{mob} = 2$ |
| UTB (Single Gate) | $E_{eff} \times B_{field}$ and $d \times B_d$ | NA | S = 75 mV/decade and $X_j = T_{dep} = T_{si}$ | $B_{field} = 0.5$ $B_d = 0.5$ |
| Metal Gate/High-$\kappa$ Gate Dielectric | $T_{ox\_el} - B_{gate}$ | $T_{ox\_el} - B_{gate}$ | $T_{ox\_el} - B_{gate}$ | $B_{gate}$ = 4Å NMOS |
| UTB (Double Gate) | $E_{eff} \times B_{field}$ and $d \times B_d$ | NA | S = 65 mV/decade and $X_j = T_{dep} = T_{si}/2$ | $B_{field} = 0.5$ Bd = 0 |
| Ballistic | $V_{sat} \times (B_{ball})$ | NA | NA | $B_{ball} = 1.3$ |
| Reduced Gate Parasitic Capacitance (Fringing and/or Overlap) | NA | $C_{fringe} \times B_{fring}$ | NA | $B_{fring} = 0.5$ |
| Metallic S/D Junction | $R_{sd} \times B_{junc}$ | NA | NA | $B_{junc} = 0.5$ |

The boosters used in Table 2 are defined as follows:
$B_{mob}$—the effective mobility ($\mu_{eff}$) improvement factor (long channel mobility) used for example to account for strained-Si channel material.
$B_{field}$— the effective field ($E_{eff}$) reduction factor used to account for lower effective field (and thus higher mobility) in UTB devices.
$B_{gate}$—the reduction in the effective electrical oxide thickness in inversion ($T_{ox\_el}$) accounting for cancellation of the poly-Si gate depletion effect and thus used to account for a metallic gate.
$B_d$—the body effect coefficient (d) reduction factor used to account for smaller d in UTB devices.
$B_{ball}$—the saturation velocity ($V_{sat}$) effective improvement factor used to account (artificially) for (quasi-) ballistic transport.
$B_{fring}$—the fringing capacitance ($C_{fring}$) reduction factor used to account for reduced fringing capacitance.
$B_{junc}$—the series resistance ($R_{sd}$) reduction factor used for example to account for metallic (Schottky) junctions.

reveal undesirable interactions and place these materials under mechanical stress or lead to their inter-diffusion, which may alter their properties. Third, the physics of new device structures is not always completely understood. Lastly, even the validity of numerical simulation results and tools are subject to debate, sometimes leading to large discrepancies, depending on the choice of tools, models, and parameters. Frequently, a new structure or material gives mediocre results from first attempts at integration, thus precluding the possibility of calibration of simulation tools and of experimental verification of predictions. Years of difficult R&D efforts are sometimes necessary to prove the real value of a technological innovation.

Given the strategic importance of this task, an example of one possible emerging device architecture roadmap scenario is offered and discussed. Considering the precautions and uncertainties previously discussed, qualitative guidelines and relative estimations are sought rather than quantitative accuracy.

The methodology employed for this task consists of using simple and widely recognized analytical expressions describing the conventional planar MOSFET physics. A set of equations (MASTAR) [93]–[94] served as a backup to an Excel spreadsheet used for the development of the logic technology requirements tables in the "Process Integration, Devices and Structures" (PIDS) chapter of the 2003 ITRS [1]. [The MASTAR executable code file along with the User's Guide are available as part of the ITRS 2003 background documentation via the metalink located in the text of the ITRS 2003 online documentation (at the end of the Nonclassical CMOS section of the Emerging Research Devices Chapter), or on request from thomas.skotnicki @st.com or frederic.boeuf@st.com.] The main equations have been aligned and calibrated between both tools so as to ensure very close agreement for all three PIDS ITRS technology tables (HP, LOP, and LSTP) [1]. The methodology used in the spreadsheet model to assemble the PIDS technology requirements tables consists in satisfying the intrinsic speed $(CV/I)^{-1}$ improvement rate (17% per year) by requiring the necessary values of $I_{on}$ (transistor "on"-current) but without linking these requirements to a given technological realization. Nonetheless, the required current $I$ resulting from the $(CV/I)^{-1}$ is matched with the $I_{on}$ value resulting from the spreadsheet model (very close to MASTAR) in which some parameters are boosted to account for new materials and novel device structures in an implicit way (without making any direct link between those two). Such an approach is believed to help the reliability of predictions. The values of the boosters were agreed between the ITRS PIDS and Emerging Research Devices (ERD) working groups, but their nature was left to be established through the more in-depth analysis carried out by the ERD group. In contrast, the following analysis is aimed at finding this link and at assessing the magnitude of improvement of the entries presented in the nonclassical CMOS Table 1(a) and (b).

In order to do so, a table of modifications was established titled "Technology Performance Boosters," given in Table 2. These modifications used in the MASTAR equations allow rough estimations of the performance gains in terms of $I_{on}$, $C_{gate}$, and $I_{off}$. Therefore, in addition to the precautions due to new materials and structures, one needs to be aware that the employed methodology cannot give more than a first-order estimate. The effect of the technology performance boosters is discussed on electrostatic integrity of the device, on the $I_{on}$–$I_{off}$ ratio, and on the $(CV/I)^{-1}$.

## Sustaining the Electrostatic Integrity of Ultra-Scaled CMOS

The electrostatic integrity (EI) of a device reflects its resistance to parasitic two-dimensional (2-D) effects such as SCE and drain-induced barrier lowering (DIBL). SCE is defined as the difference in threshold voltage between long-channel and short-channel FETs measured using small $V_{ds}$. DIBL is defined as the difference in $V_t$ measured for short-channel FETs using a small and a nominal value for $V_{ds}$.

A good EI means a one-dimensional (1-D) potential distribution in a device (as in the long-channel case), whereas poor EI means a 2-D potential distribution that results in the 2-D parasitic effects. A simple relationship between SCE and DIBL on one hand and EI on the other has been established, as follows [94]–[95]:

$$\text{SCE} \approx 2.0 \times \Phi_d \times \text{EI}$$
$$\text{DIBL} \approx 2.5 \times V_{\text{ds}} \times \text{EI},$$

where $\Phi_{\text{d}}$ is the source-to-channel junction built-in voltage, $V_{\text{ds}}$ is the drain-to-source bias, and EI is given by:

$$\text{EI} \equiv \left(1 + \frac{x_{\text{j}}^2}{L_{\text{el}}^2}\right) \frac{T_{\text{ox\_el}}}{L_{\text{el}}} \frac{T_{\text{dep}}}{L_{\text{el}}}.$$

In this expression, $x_{\text{j}}$ denotes the junction extension depth, $L_{\text{el}}$ denotes the electrical channel length (junction-to-junction distance), $T_{\text{ox\_el}}$ denotes the effective electrical oxide thickness in inversion (equal to the sum of the equivalent oxide thickness of the gate dielectric, the poly-Si gate depletion depth, and the so-called "dark space"), and $T_{\text{dep}}$ denotes the depletion depth in the channel. ("Dark space" is the distance the inversion charge layer peak is set back in the channel from the $SiO_2$/Si interface due to quantization of the energy levels in the channel quantum well.)

The strength of nonclassical CMOS structures, in particular of UTB devices, is clearly shown by this expression when applying the translations of parameters relevant to UTB devices (refer to Table 2). Replacing $x_{\text{j}}$ and $T_{\text{dep}}$ by $T_{\text{Si}}$ (UTB single gate) or $T_{\text{Si}}/2$ (UTB double gate) permits a considerable reduction in the $x_{\text{j}}/L_{\text{el}}$ and $T_{\text{dep}}/L_{\text{el}}$ ratios, with the condition that silicon films of $T_{\text{Si}} \ll x_{\text{j}}$, $T_{\text{dep}}$ are available. The key question therefore is the extent to which body or channel thickness in advanced MOSFETs must be thinned to sustain good EI.

Figure 1 compares the EI between bulk planar and double-gate devices throughout the span of nodes for the *2003 ITRS*. It is encouraging to see that the $T_{\text{Si}}$ scaling, although very aggressive (4- and 5-nm Si films are required at the end of the roadmap for HP, and LOP/LSTP, respectively), has the potential to scale CMOS to the end of the roadmap with the SCE and DIBL at the same levels as the 90-nm node technologies. [EI $\leq$ 10% (meaning DIBL of < 25% $V_{\text{ds}}$) is assumed as the acceptable range as represented as a yellow region in Figure 1.] Note that the EI of planar bulk or classical devices is outside the allowed zone at the 100-nm node for HP, near the 65-nm node for LOP, and between the 90- and 65-nm nodes for LSTP products.

### Sustaining the $I_{\text{on}} - I_{\text{off}}$ Ratio

The technological maturity of some performance boosters is higher than that of others. For example, strained-silicon channel devices have already been announced as being incorporated into the CMOS 65-nm node, whereas the metallic source/drain junction concept is in the research phase. Without attempting precise predictions on the introduction node for a given technology performance booster, the following chronological sequence is suggested as a plausible scenario for their sequential introduction:

- ✦ strained-Si channels
- ✦ UTB single-gate FETs
- ✦ metallic-gate electrode (together with high-$\kappa$ dielectric)
- ✦ UTB double-gate FETs
- ✦ ballistic or quasi-ballistic transport
- ✦ reduced fringing (and/or overlap) capacitance
- ✦ metallic source/drain junction.

Figure 2 shows the evolution of the $I_{\text{off}}$–$I_{\text{on}}$ roadmaps (HP, LOP, and LSTP) [1] due to introduction of the technology performance boosters as defined in Table 2, according to the aforementioned sequence and in a cumulative way. The planar bulk device is basically sufficient for satisfying the CMOS ($I_{\text{on}}$–$I_{\text{off}}$) specifications up to 90-nm node for HP and up to 65-nm node for LOP and LSTP. Beyond these nodes, the introduction of technology performance boosters becomes mandatory for meeting the specifications. Exceeding the specifications appears possible if all boosters considered are cointegrated. It is also to be noted that HP products use the greatest number of performance boosters (all except the metallic S/D junctions) to address the entire HP roadmap, whereas the LSTP roadmap can be satisfied with UTB single metallic gate devices.

This analysis assumes that the $I_{\text{off}}$ current is determined by the maximum allowed source/drain subthreshold leakage current. The maximum gate leakage current is related to the maximum source/drain leakage current at threshold. For this to be true, high-$\kappa$ gate dielectrics need to be introduced in 2006 for LOP and LSTP and in 2007 for high-performance logic [1].

### Boosting the Intrinsic Speed $(CV/I)^{-1}$

Certain performance boosters may lead to an increase in $I_{\text{on}}$ at the same rate as an increase in $C_{\text{gate}}$, thus producing a small or negligible effect on $CV/I$ (for example, see metallic gate in Table 2). Others, such as reduced fringing or overlap capacitance, may reduce $C_{\text{gate}}$ without altering $I_{\text{on}}$. The evolution of the intrinsic device speed $(CV/I)^{-1}$ as impacted by the performance boosters may thus be somewhat different than the evolution of the $I_{\text{on}}$–$I_{\text{off}}$. Figure 3 shows rough estimates for the evolution of the intrinsic device speed for the consecutive CMOS nodes. Up to the 65-nm node the optimized scaling strategy (basically equal to the ITRS 2001) is sufficient for the LOP and LSTP products to achieve an annual performance increase of 17%-per-year. HP products, again, require the most aggressive use of the performance boosters, such as requiring strained-Si channels beginning at the 65-nm node. Beyond this node, a sequential introduction of performance boosters is mandatory for maintaining the 17% per year performance improvement rate. At the 22 nm-node, fringing (and/or overlap) capacitance needs to be reduced to meet the speed requirements of HP and LOP products. However, cointegrating the boosters up to and including the quasiballistic transport, according to the sequence presented in Table 2, can satisfy the requirements for LSTP. It is encouraging to see

that the metallic junction booster is not employed within the current roadmap, thus leaving a margin for its prolongation beyond the 22-nm node without any loss in the performance improvement rate.

## SUMMARY AND CONCLUSIONS

Scaling CMOS to and beyond the 22-nm technology node (requiring a physical gate length of 9-nm or less) will probably require the introduction of several new material and structural changes to the MOSFET to sustain performance increases of 17% per year and to manage SCEs. Material changes will include strained silicon n- and p-channels and a new gate stack including a high-k dielectric and a metal gate electrode. Structural changes could include fully depleted UTB SOI single-gate MOSFETs, perhaps followed by fully depleted UTB double-gate structures. Attaining the performance requirements for the final node for high performance applications could further require channels providing quasiballistic carrier transport, or very low-resistance source/drain contacts provided by Schottky metal electrodes. The materials and structural changes actually introduced to advanced process technologies will depend both on their readiness for manufacture and their value in improving performance in the ultra-scaled devices. For example, a high-$\kappa$ dielectric may be needed by the 65-nm node to limit gate leakage current for LSTP applications, but a viable high-$\kappa$ metal gate technology may not be ready for manufacture until the 45-nm node. Also, different manufacturers may vary the sequence of technology introduction to manufacturing to suit their particular requirements and manufacturing readiness. One possible sequence of technology enhancements, proposed in this article, is the following:

- ✦ strained-Si channels
- ✦ UTB single-gate MOSFETs
- ✦ Metallic-gate electrode (probably integrated simultaneously with a high-$\kappa$ dielectric)
- ✦ UTB double-gateMOSFETs
- ✦ ballistic or quasiballistic carrier transport
- ✦ reduced fringing (and/or overlap) capacitance
- ✦ metallic source/drain junction.

An alternate sequence would introduce strained-Si channels, followed by new gate stack materials with UTB single-gate MOSFETs introduced sometime after the new gate stack. For high-performance applications scaled beyond the 65-nm node, a sequential introduction of performance boosters is mandatory for maintaining the 17% per year performance improvement rate. At the 22-nm node, fringing (and/or overlap) capacitance needs to be reduced to meet the speed requirements of HP and LOP products.

Successful realization of one or more technology nodes may require the introduction of two or more new process modules simultaneously to achieve the roadmap projected performance. During the past several years, the semiconductor industry, supported by their research community, has identified and demonstrated several new options for accomplishing these demanding objectives, to sustain the historical cadence of CMOS scaling during and beyond the next ten years.

## REFERENCES


[1] *Semiconductor Industry Association (SIA), International Roadmap for Semiconductors*, 2003 ed., Austin, TX., Int. SEMATECH, 2003. [Online]. Available: http: //public.itrs.net

[2] C. Chiu, "A sub-400 degree C Germanium MOSFET technology with high-$\kappa$ dielectric and metal gate." in *Proc. IEDM'02,* pp. 437–440.

[3] H. Shang, "High mobility p-channel Germanium MOSFETs with a thin Ge xxynitride gate dielectric," presented at *IEDM*, San Francisco, 2002.

[4] C.W. Leitz, "Hole mobility enhancements in strained Si/Si/sub 1-y/Ge/sub y/ p-type metal-oxide-semiconductor field-effect transistors grown on relaxed Si/sub 1-x/Ge/sub x/ (x<y) virtual substrates," *Appl. Phys. Lett.*, vol. 79, no. 25, Dec. 17, 2001.

[5] M. Lee, "Strained Ge channel p-type metal-oxide-semiconductor field-effect transistor grown on Si x Ge 1-x / Si virtual substrates," *Appl. Phys. Lett.*, vol. 79, no. 20, Nov. 21, 2001.

[6] B.H. Lee, "Performance enhancement on Sub-70 nm strained silicon SOI MOSFETs on ultra thin thermally mixed strained silicon/SiGe on insulator (TM-SGOI) substrate with raised S/D," presented at *IEDM*, San Francisco, Dec. 8–11, 2002.

[7] T. Mizuno, "High performance CMOS operation of strained-SOI MOSFETs using thin film SiGe-on-insulator substrate," presented at *VLSI Technology Symp.*, Honolulu, June 11–13, 2002.

[8] T. Tezuka, "High-performance strained Si-on-insulator MOSFETs by novel fabrication processes utilizing Ge-condensation technique," presented at *VLSI Technology Symp.*, Honolulu, June 11–13, 2002.

[9] N. Collaert, "High-performance strained Si/SiGe pMOS devices with multiple quantum wells," *IEEE Trans. Nanotechnol.*, vol. 1, pp. 190–194, Dec. 2002.

[10] T. Ernst, "A new Si:C epitaxial channel nMOSFET architecture with improved drivability and short-channel characteristics," presented at *VLSI Technology Symp.*, Kyoto, Japan, June 10–12, 2003.

[11] Qi Xiang, "Strained silicon NMOS with nickel-silicide metal gate," presented at *VLSI Technology Symp.*, Kyoto, Japan, June 10–12, 2003.

[12] J.R. Hwang, "Performance of 70 nm strained-silicon CMOS devices," presented at *VLSI Technology Symp.*, Kyoto, Japan, June 10–12, 2003.

[13] T. Mizuno, "(110)-surface strained-SOI CMOS devices with higher carrier mobility," presented at *VLSI Technology Symp.*, Kyoto, Japan, June 10–12, 2003.

[14] C.H. Huang, "Very low defects and high performance Ge-on-insulator p-MOSFETs with Al2O3 gate dielectrics," presented at *VLSI Technology Symp.*, Kyoto, Japan, June 10–12, 2003.

[15] S. Takagi, "Re-examination of sub-band structure engineering in ultra-short channel MOSFETs under ballistic carrier transport" presented at *VLSI Technology Symp.*, p. 115, 2003.

[16] S.E. Thompson, M. Armstrong, C. Auth, S. Cea, R. Chau, G. Glass, T. Hoffman, J. Klaus, Z. Ma, B. Mcintyre, A. Murthy, B. Obradovic, L. Shifren, S. Sivakumar, S. Tyagi, T. Ghani, K. Mistry, M. Bohr, and Y. El-Mansy, "A logic nanotechnology featuring strained-silicon," *IEEE Electron Device Lett.*, vol. 25, no. 4, pp. 191–193, Apr. 2004.

[17] M. Yang et al. (IBM), "High performance CMOS fabricated on hybrid substrate with different crystal orientations," in *IEDM Tech. Dig.*, 2003, p. 453.

[18] K. Rim et al., "Fabrication and Mobility Characteristics of Ultra-thin Strained Si Directly on Insulator (SSDOI) MOSFETs," in *IEDM Tech. Dig.*, Washington, DC., Dec. 8–10, 2003, pp. 49–52.

[19] L. Huang, J.O. Chu, S.A. Goma, C.P. D'Emic, S.J. Koester, D.F. Canaperi, P.M. Mooney, S.A. Cordes, J.L Speidell, R.M. Anderson, and H.S.P. Wong, "Electron and hole mobility enhancement in strained SOI by wafer bonding," *IEEE Trans. Electron Devices*, vol. 49, no. 9, pp. 1566–1571, Sept. 2002.

[20] T. Tezuka, N. Sugiyama, T. Mizuno, and S. Takagi, "Ultrathin body SiGe-on-insulator pMOSFETs with high-mobility SiGe surface chan-

nels," *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1328–1333, May 2003.

[21] B. Doris, "Extreme scaling with ultra-thin Si channel MOSFETs," in *IEDM Tech. Dig.*, San Francisco, IBM, Dec. 8–11, 2002, pp. 267–270.

[22] R. Chau, "A 50 nm depleted-substrate CMOS transistor (DST)," in *IEDM Tech. Dig.*, Washington, Intel, Dec. 2–5, 2001, pp. 621–624.

[23] H. VanMeer, "70 nm fully-depleted SOI CMOS using a new fabrication scheme: The spacer/replacer scheme, in *VLSI Symp.*, Honolulu, IMEC, June 11–13, 2002, pp. 170–171.

[24] T. Schultz, "Impact of technology parameters on inverter delay of UTB-SOI CMOS," in *Proc. SOI Conf.*, Williamsburg, Infineon, Oct. 7–10, 2002, pp. 176–178.

[25] A. Vandooren, "Ultra-thin body fully-depleted SOI devices with metal gate (TaSiN) gate, high k ($HfO_2$) dielectric and elevated source/drain extensions," in *Proc. SOI Conf.*, Williamsburg, Motorola, Oct. 7–10, 2002, pp. 205–206.

[26] B. Yu, "Scaling towards 35 nm gate length CMOS," in *Proc. VSLI Symp.*, Kyoto, AMD, June 12–14, 2001, pp. 9–10.

[27] Y.K. Choi, "Ultra-thin body PMOSFETs with selectively deposited Ge source/drain," in *Proc. VSLI symp.*, Kyoto, UCB, June 12–14, 2001, pp. 19–20.

[28] K. Uchida, "Experimental study on carrier transport mechanism in ultrathin-body SOI n and p MOSFETs with SOI thickness less than 5 nm," *IEDM Tech. Dig.*, San Francisco, Toshiba, Dec. 8–11, 2002, pp. 47–50.

[29] K. Ishii, E. Suzuki, S. Kanemaru, T. Maeda, K. Nagai, and T. Sekigawa, "Suppressed threshold voltage roll-off characteristic of 40 nm gate length ultrathin SOI MOSFET," *Electronics Lett.*, vol. 34, no. 21, pp. 2069–2070, Oct. 1998.

[30] E. Suzuki, K. Ishii, S. Kanemaru, T. Maeda, T. Tsutsumi, T. Sekigawa, K. Nagai, and H. Hiroshima, "Highly suppressed short-channel effects in ultrathin SOI n-MOSFETs," *IEEE Trans. Electron Devices*, vol. 47, no. 2, pp. 354–359, Feb. 2000.

[31] Y.-K. Choi, K. Asano, N. Lindert, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, "Ultrathin-body SOI MOSFET for deep-sub-tenth micron era," *IEEE Electron Device Lett.*, vol. 21, no. 5, pp. 254–255, May 2000.

[32] M. Jurczak, "SON (Silicon On Nothing)—A new device architecture for the ULSI era," in *Proc. Symp. VLSI Technology*, FranceTelecomR&D, June 1999, pp. 29–30.

[33] T. Skotnicki, "Heavily doped and extremely shallow junctions on insulator—by SONCTION (SilicON Cut-off junction) process," in *IEDM Tech. Dig.*, STMicroelectronics, Dec. 1999, pp. 513–516.

[34] M. Jurczak, "SON (silicon on nothing) – An innovative process for advanced CMOS," *IEEE Trans. Electron Devices*, p. 2179, FranceTelecomR&D, Nov. 2000.

[35] S. Monfray, "First 80 nm SON (silicon-on-nothing) MOSFETs with perfect morphology and high electrical performance,"in *IEDM Tech. Dig.*, STMicroelectronics, Dec. 2001, pp. 645–648.

[36] S. Monfray, "SON (silicon-on-nothing) P-MOSFETs with totally silicided ($CoSi_2$) polysilicon on 5 nm-thick Si-films: The simplest way to integration of metal gates on thin FD channels,"in *IEDM Tech. Dig.,* STMicroelectronics, Dec. 2002, p. 263.

[37] S. Monfray, "Highly-performant 38 nm SON (silicon-on-nothing) P-MOSFETs with 9 nm-thick channels," *Proc. IEEE SOI Conf.*, STMicroelectronics, Oct. 2002, p. 20.

[38] T. Sato, "SON (silicon on nothing) MOSFET using ESS (empty space in silicon) technique for SoC applications," in *IEDM Tech. Dig.*, Toshiba, Dec. 2001, p. 809.

[39] M. Jurczak, T. Skotnicki, M. Paoli, B. Tormen, J. Martins, J.L. Regolini, D. Dutartre, P. Ribot, D. Lenoble, R. Pantel, and S. Monfray, "Silicon-on-nothing (SON)-an innovative process for advanced CMOS," *IEEE Trans. Electron Devices*, vol. 47, no. 11, pp. 2179–2187, Nov. 2000.

[40] J. Pretet, S. Monfray, S. Cristoloveanu, and T. Skotnicki, "Silicon-on-nothing MOSFETs: performance, short-channel effects, and backgate coupling," *IEEE Trans. Electron Devices*, vol. 51, no. 2, pp. 240–245, Feb. 2004.

[41] J. Kedzierski, "Complementary silicide source/drain thin-body MOSFETs for the 20 nm gate length regime," presented at *IEDM*, San Francisco, Dec. 2002.

[42] R. Rishton, "New complementary metal-oxide semiconductor technology with self-aligned Schottky source/drain and low-resistance T-gates," *J. Vac. Sci. Technol.*, p. 2795–2798, 1997.

[43] J.P. Snyder, "Experimental investigation of a PtSi source and drain field emission transistor," *Appl. Phys. Lett.*, vol. 67, no. 10, Sept. 4, 1995.

[44] T. Ichimori and N. Hirashita, "Fully-depleted SOI CMOSFETs with the fully-silicided source/drain structure," *IEEE Trans. Electron Devices*, vol. 49, no. 12, pp. 2296–2300, Dec. 2002.

[45] D. Connelly, C. Faulkner, and D.E. Grupp, "Performance advantage of Schottky source/drain in ultrathin-body silicon-on-insulator and dual-gate CMOS," *IEEE Trans. Electron Devices*, vol. 50, no. 5, pp. 1340–1345, May 2003.

[46] M. Fritze, C.L. Chen, S. Calawa, D. Yost, B. Wheeler, P. Wyatt, C.L. Keast, J. Snyder, and J. Larson, "High-speed Schottky-barrier pMOSFET with $f_T$=280 GHz," *IEEE Electron Device Lett.*, vol. 25, no. 4, pp. 220–222, Apr. 2004.

[47] S. Zhu, H.Y. Yu, S.J. Whang, J.H. Chen, C. Shen, C. Zhu, S.J. Lee, M.F. Li, D.S.H. Chan, W.J. Yoo, A. Du, C.H. Tung, J. Singh, A. Chin, and D.L. Kwong, "Schottky-barrier S/D MOSFETs with high-k gate dielectrics and metal-gate electrode," *IEEE Electron Device Lett.*, vol. 25, no. 5, pp. 268–270, May 2004.

[48] B.-Y. Tsui and C.-P. Lin, "A novel 25-nm modified Schottky-barrier FinFET with high performance," *IEEE Electron Device Lett.*, vol. 25, no. 6, pp. 430–432, June 2004.

[49] F. Boeuf, "16 nm planar NMOSFET manufacturable within state-of-the-art CMOS process thanks to specific design and optimization," in *Proc. IEDM*, Washington, D.C., Dec. 2001, pp. 637–640.

[50] H. Lee, "DC and ac characteristics of sub-50-nm MOSFETs with source/drain-to-gate nonoverlapped structure," *IEEE Trans. Nanotechnology*, vol. 1, no. 4, pp. 219–225, Dec. 2002.

[51] H. Lee, J. Lee, and H. Shin, "DC and ac characteristics of sub-50-nm MOSFETs with source/drain-to-gate non-overlapped structure," *IEEE Trans. Nanotechnology*, vol. 1, no. 4, pp. 219–225, Dec. 2002.

[52] D. Connelly, C. Faulkner, and D.E. Grupp, "Optimizing Schottky S/D offset for 25-nm dual-gate CMOS performance," *IEEE Electron Device Lett.*, vol. 24, no. 6, pp. 411–413, June 2003.

[53] R. Chau, "Advanced depleted substrate transistor: Single-gate, double-gate, and tri-gate," *Solid State Device Meeting*, pp. 68–69, 2002.

[54] Fu-Liang Yang, "25 nm CMOS Omega FETs," in *Proc. IEDM* 2002 TSMC, Dec. 2002, p. 255.

[55] J. Colinge, "Silicon-on-insolator gate-all-around device," in *Proc. IEDM* 1990. IEDM 90, IMEC, Dec. 1990, p. 595.

[56] B. Doyle, "Tri-gate fully-depleted CMOS transistors fabrication, design and layout," in *Proc. VLSI* 2003, INTEL, June, 2003, p. 133.

[57] Z. Krivokapic, "High performance 45 nm CMOS technology with 20 nm multi-gate devices," in *Proc. SSDM* '03, AMD, Sept. 2003, p. 760.

[58] B.S. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, A. Murthy, R. Rios, and R. Chau, "High performance fully-depleted tri-gate CMOS transistors," *IEEE Electron Device Lett.*, vol. 24, no. 4, pp. 263–265, Apr. 2003.

[59] W.-J. Cho, C.-G. Ahn, K. Im, J.-H. Yang, J. Oh, I.-B. Baek, and S. Lee, "Fabrication of 50-nm gate SOI n-MOSFETs using novel plasma-doping technique," *IEEE Electron Device Lett.*, vol. 25, no. 6, pp. 366–368, June 2004.

[60] Y.-K. Choi, "FinFET process refinements for improved mobility and gate work function engineering," in *Proc. IEDM,* UC California (Berkeley), Dec. 2002, p. 259.

[61] J. Kedzierski, "Metal-gate FinFET and fully-depleted SOI devices using total gate silicidation," in *Proc. IEDM,* IBM, Dec. 2002, p. 247.

[62] B. Yu, "FinFET scaling to 10 nm gate length," in *Proc. IEDM* Strategic Technology, Advanced Micro Devices, Dec. 2002, p. 251.

[63] T. Park, "Fabrication of body-tied FinFETS (Omega MOSFETS) using bulk Si wafers," in *Proc. VLSI,* SAMSUNG, June 2003, p. 135.

[64] D. Hisamoto, T. Kaga, Y. Kawamoto, and E. Takeda, "A fully depleted lean-channel transistor (DELTA)-a novel vertical ultrathin SOI MOSFET," *IEEE Electron Device Lett.*, vol. 11, no. 1, pp. 36–38, Jan. 1990.

[65] D. Hisamoto, T. Kaga, and E. Takeda, "Impact of the vertical SOI 'DELTA' structure on planar device technology," *IEEE Trans. Electron Devices*, vol. 38, no. 6, pp. 1419–1424, June 1991.

[66] D. Hisamoto, W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.-J. King, J. Bokor, and C. Hu, "FinFET: A self-aligned double-gate MOSFET scalable to 20 nm," *IEEE Trans. Electron Devices*, vol. 47, no. 12, pp. 2320–2325, Dec. 2000.

[67] X. Huang, W.-C. Lee, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, E. Anderson, H. Takeuchi, Y.-K. Choi, K. Asano, V. Subramanian, T.-J. King, J. Bokor, and C. Hu, "Sub-50 nm P-channel FinFET," *IEEE Trans. Electron Devices*, vol. 48, no. 5, pp. 880–886, May 2001.

[68] N. Lindert, L. Chang, Y.-K. Choi, E.H. Anderson, W.-C. Lee, T.-J. King, J. Bokor, and C. Hu, "Sub-60-nm quasi-planar FinFETs fabricated using a simplified process," *IEEE Electron Device Lett.*, vol. 22, no. 10, pp. 487–489, Oct. 2001.

[69] Y.-K. Choi, T.-J. King, and C. Hu, "Nanoscale CMOS spacer FinFET for the terabit era," *IEEE Electron Device Lett.*, vol. 23, no. 1, pp. 25–27, Jan. 2002.

[70] G. Pei, J. Kedzierski, P. Oldiges, M. Ieong, and E.C.-C. Kan, "FinFET design considerations based on 3-D simulation and analytical modeling," *IEEE Trans. Electron Devices*, vol. 49, no. 8, pp. 1411–1419, Aug. 2002.

[71] J. Kedzierski, J. Ieong, E. Nowak, T.S. Kanarsky, Y. Zhang, R. Roy, D. Boyd, D. Fried, and H.-S.P. Wong, "Extension and source/drain design for high-performance FinFET devices," *IEEE Trans. Electron Devices*, vol. 50, no. 4, pp. 952–958, Apr. 2003.

[72] S. Monfray, "50 nm—Gate All Around (GAA)—Silicon On Nothing (SON)—Devices: A simple way to co-integration of GAA transistors with bulk MOSFET process," in *Proc. VLSI*, STMicroelectronics, June 2002, p. 108.

[73] Lee, "A Manufacturable Multiple Gate Oxynitride Thickness Technology for System on a Chip," in *Proc. IEDM* (12/1999), UC Texas, Dec. 1999, p. 71.

[74] S. Harrison et al., "Highly performant double gate MOSFET realized with SON process," in *Proc. IEDM Tech. Dig.*, Washington, DC, Dec. 8–10, 2003, pp. 449–452.

[75] H.-S. P. Wong, "Self aligned (top and bottom) double-gate MOSFET with a 25 nm thick silicon channel," in *Proc. IEDM* 1997, IBM, Dec. 1997, p. 427.

[76] G. Neudeck, "Novel silicon epitaxy for advanced MOSFET devices," in *Proc. IEDM* 2000, Purdue Univ., Dec. 2000, p. 169.

[77] S.-M. Kim, "A novel MBC (Multi-bridge-channel) MOSFET: Fabrication technologies and characteristics," in *Proc. Si-Nanoworkshop*, 2003 SAMSUNG, p. 18.

[78] F. Balestra, S. Cristoloveanu, M. Benachir, J. Brini, and T. Elewa, "Double-gate silicon-on-insulator transistor with volume-inversion: A new device with greatly enhanced performance," *IEEE Electron Device Lett.*, vol. EDL-8, pp. 410–412, Sept. 1987.

[79] I. Yang, *IEEE Trans. Electron Devices*, p. 822, 1997.

[80] Y.X. Liu, "Flexible threshold voltage FinFETs with independent double gates and an ideal rectangular cross-section Si-Fin channel," in *IEDM Tech. Dig.*, Washington, DC, Dec. 8–10, 2003, pp. 986–988.

[81] K.W. Guarini, "Triple-self-aligned, planar double-gate MOSFETs: Devices and circuits," in *Proc. IEDM* 2001, IBM, Dec. 2001, p. 425.

[82] D.M. Fried, J.S. Duster, and K.T. Kornegay, "Improved independent gate N-type FinFET fabrication and characterization," *IEEE Electron Device Lett.*, vol. 24, no. 9, pp. 592–594, Sept. 2003.

[83] Y. Liu, M. Masahara, K. Ishii, T. Sekigawa, H. Takashima, H. Yamauchi, and E. Suzuki, "A highly threshold voltage-controllable 4T FinFET with an 8.5-nm-thick Si-Fin channel," *IEEE Electron Device Lett.*, vol. 25, no. 7, pp. 510–512, July 2004.

[84] D.M. Fried, J.S. Duster, and K.T. Kornegay, "High-performance p-type independent-gate FinFETs," *IEEE Electron Device Lett.*, vol. 25, no. 4, pp. 199–201, Apr. 2004.

[85] J. Hergentother, "The vertical replacement-gate (VRG) MOSFET: A 50-nm vertical MOSFET with lithography-independent gate length," *IEDM* 1999, Dec. 1999, p .3.1.1, AT&T Bell Labs, p. 75.

[86] J.M. Hergenrother, "50 nm Vertical Replacement-gate (VRG) nMOSFETs with ALD HfO2 and AL2O3 Gate Dielectrics," in *Proc. IEDM* 2001 Dec. 2001, AT&T Bell Labs, pp. 51–54.

[87] E. Josse, "High performance 40 nm vertical MOSFET within a conventional CMOS process flow," in *Proc. VLSI* 2001, ST Microelectronics, June 2001, pp. 55–56.

[88] P. Verheyen, "A 50 nm vertical Si/sub 0.70/Ge/sub 0.30//Si/sub 0.85/Ge/sub 0.15/ pMOSFET with an oxide/nitride gate dielectric, Conf.: 2001 International Symp. on VLSI Technology, Systems, and Applications. Proceedings of Technical Papers (Cat. No.01TH8517), *IMEC*, Leuven, Belgium, pp. 15–18, B. Goebel, Fully Depleted Surrounding Gate Transistor (SGT) for 70 nm DRAM and Beyond, in *Proc. IEDM* 2002, Infineon, Dec. 2002, p. 275.

[89] B. Goebel, "Fully Depleted Surrounding Gate Transistor (SGT) for 70 nm DRAM and Beyond," in *Proc. IEDM* 2002, Infineon, Dec. 2002, p. 275.

[90] M. Masahara, "15-nm-thick Si channel wall vertical double-gate MOSFET," in *Proc. IEDM* 2002, AIST, Dec. 2002, p. 949.

[91] A. Nitayama, H. Takato, N. Okabe, K. Sunouchi, K. Hieda, F. Horiguchi, and F. Masuoka, "Multi-pillar surrounding gate transistor (M-SGT) for compact and high-speed circuits," *IEEE Trans. Electron Devices*, vol. 38, no. 3, pp. 579–583, March 1991.

[92] S.-H. Oh, D. Monroe, and J.M. Hergenrother, "Analytic description of short-channel effects in fully-depleted double-gate and cylindrical, surrounding-gate MOSFETs," *IEEE Electron Device Lett.*, vol. 21, no. 9, pp. 445–447, Sept. 2000.

[93] T. Skotnicki and F. Boeuf, "CMOS technology roadmap—Approaching up-hill specials," in *Ninth International Symp. Silicon Materials Science Technology, Process Integration*, ECS 2002.

[94] T. Skotnicki and F. Boeuf, "Optimal scaling methodologies and transistor performance," chapter in *High-K Gate Dielectric Materials for VLSI MOSFET Applications,* H. Huff and D. Gilmer, Eds. New York: Springer Verlag, in press.

[95] T. Skotnicki, in *Proc. ESSDERC 2000*, invited talk, Cork, Ireland, Sept. 2000, pp. 19–33.

*Thomas Skotnicki* and *Frederic Boeuf* are with ST Microelectronics in Crolles, France. *James A. Hutchby* is with Semiconductor Research Corp. in Durham, North Carolina. *Tsu-Jae King* is with the University of California in Berkeley, California. *H.-S. Philip Wong* is with Stanford University in Palo Alto, California. E-mail: hutchby@src.org. CD ■