Towards Highly Parallel Event Processing through Reconfigurable Hardware

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1 Real-time Event Processing Scenario

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Algorithm Trading

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Algorithmic Trading Challenges

1. Sustain a high event rate because algorithmic trading dominates financial markets and accounts for over 70% of all trading
2. Minimize matching time because every 1-millisecond generates a staggering amount of $100 million annually

Real-time Event Processing Challenges

Event Processing Requirements

An event processing platform must efficiently find all patterns or specifications (subscriptions) that match incoming events at a rate up to a million events per second.

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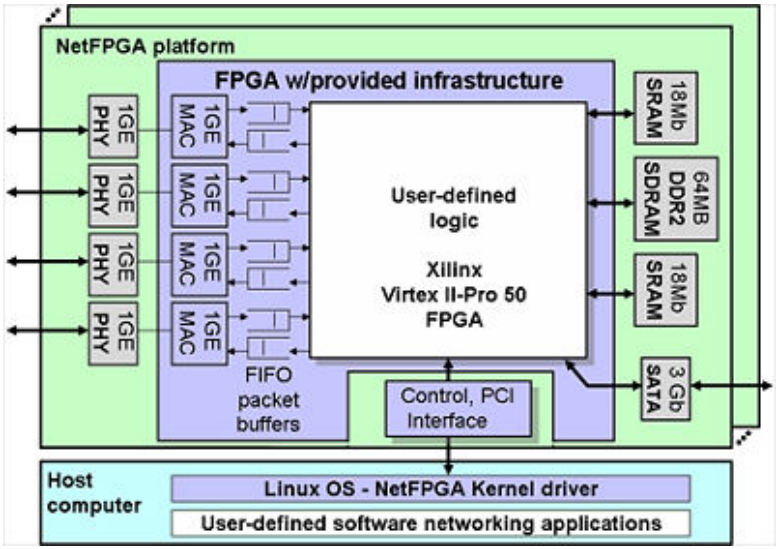
Our Solution

We propose a novel FPGA-based event processing platform to significantly accelerate event processing computations, namely, event parsing and event matching against patterns or specifications.

NetFPGA Card



Verilog Snippet

```
case (CurrentState)
        IDLE: begin
                if (Go)
                        NextState = SELECT_CLUSTER_ID;
                else
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        end
        SELECT_CLUSTER_ID: begin                        // Select a valid cluster index
                if (curCluster > LAST_CLUSTER)          // Finished reading last cluster
                                                        // When all clusters are invalid
                        NextState = WAIT;
                else
                        NextState = START_ADDRESS;
        end
        START_ADDRESS: begin                            // Select cluster address
                if (curCluster > LAST_CLUSTER)          // Finished reading last cluster
                                                        // When all clusters are invalid
                        NextState = WAIT;
                else if (can_take_more_requests)
                        NextState = MEM_BURST_WAIT;
                else
                        NextState = START_ADDRESS;      // If 'can_take_more_requests' is low, wait
        end
        NEXT_ADDRESS: begin                             // Check data from cluster terminator
                if (clusterEndFound)
                        NextState = SELECT_CLUSTER_ID;
                else if (can_take_more_requests)
                        NextState = MEM_BURST_WAIT;     // Increment curAddr by 16 bytes
                else
                        NextState = NEXT_ADDRESS;       // If 'can_take_more_requests' is low, wait
        end
        default
                NextState = IDLE;
endcase
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FPGAs Challenges

FPGA caveats

1. The latest FPGA (e.g., 800MHz Xilinx Virtex 6) operates at significantly lower speed compared to CPUs (e.g., 3.46GHz Intel i7)

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Open Problems

The true success of FPGAs is rooted in three distinctive features: hardware reconfigurability, hardware parallelism, and onboard packet processing.

Why FPGAs

FPGA distinctive features

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4. *Cost-effective and Energy-efficient*

Language and Data Model

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Definition

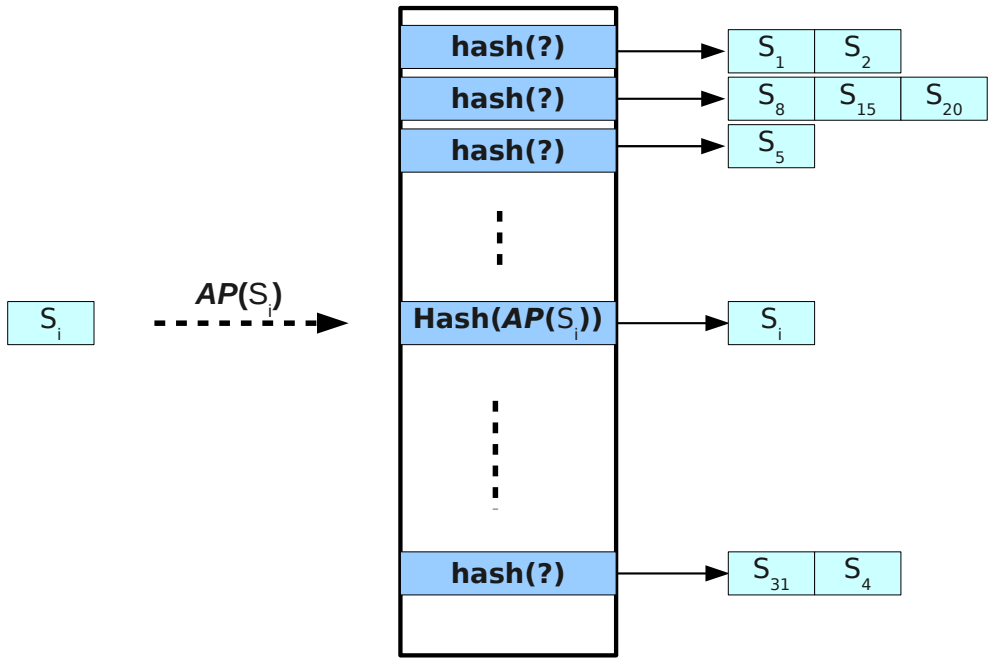
$$e = \left\{ P_1^{(\texttt{attr}_\texttt{i},\texttt{opt},\texttt{val})} \wedge \cdots \wedge P_k^{(\texttt{attr}_\texttt{j},\texttt{opt},\texttt{attr}_\texttt{l})} \right\}.$$

Matching Semantics

Matching Problem

Given a event e and a set of subscriptions $\mathbf{s}$, find all subscriptions $s_i \in \mathbf{s}$ satisfied by e.

An Abstract View of Propagation Data Structure



Propagation (Fabret, Jacobsen, Llirbat, Pereira, Ross, and Shasha, SIGMOD'01)

1. Distribute subscriptions in disjoint clusters to achieve high degree of parallelism
2. Store subscriptions as contiguous blocks of memory, which enables fast sequential access to improve memory locality

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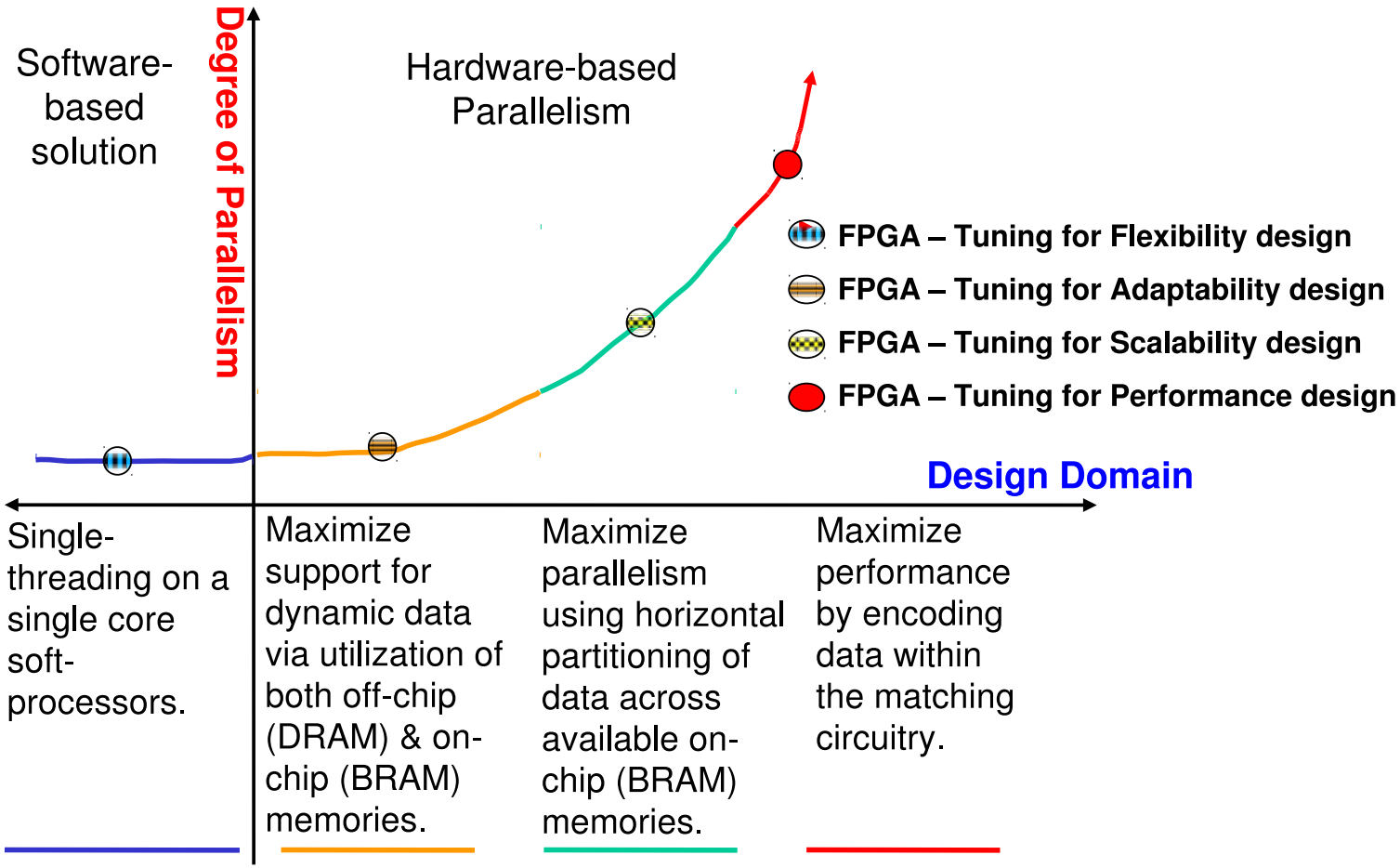
An Overview of Our Design Space

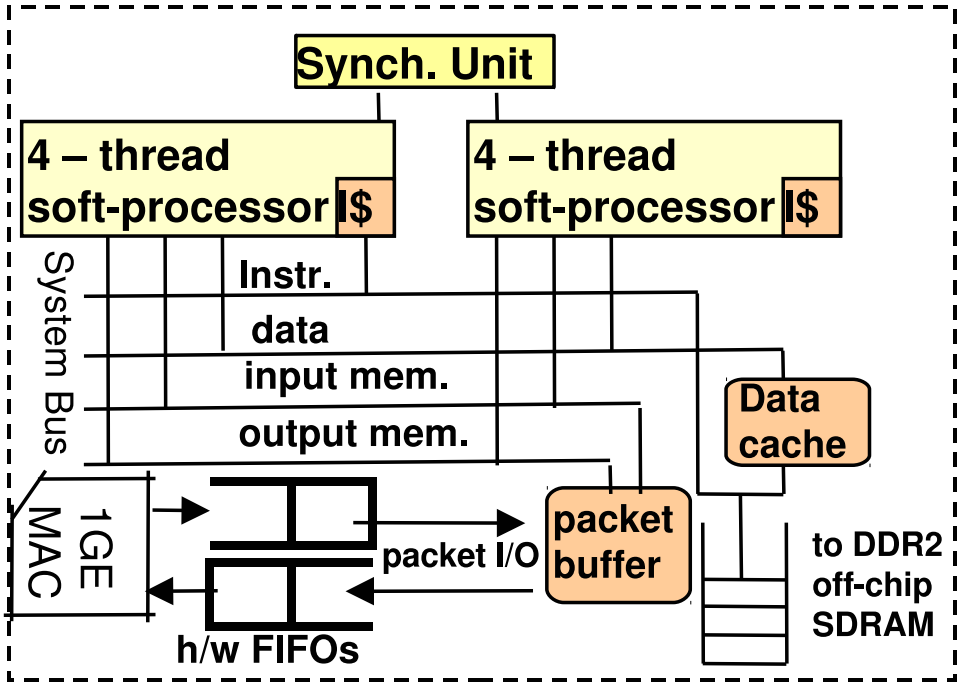
Four key designs

1. **Flexibility:** providing ease of the development and deployment cycle
2. **Adaptability:** supporting subscription updates
3. **Scalability:** relying on horizontal data partitioning
4. **Performance:** achieving the highest level of parallelism

Degrees of Offered Parallelism

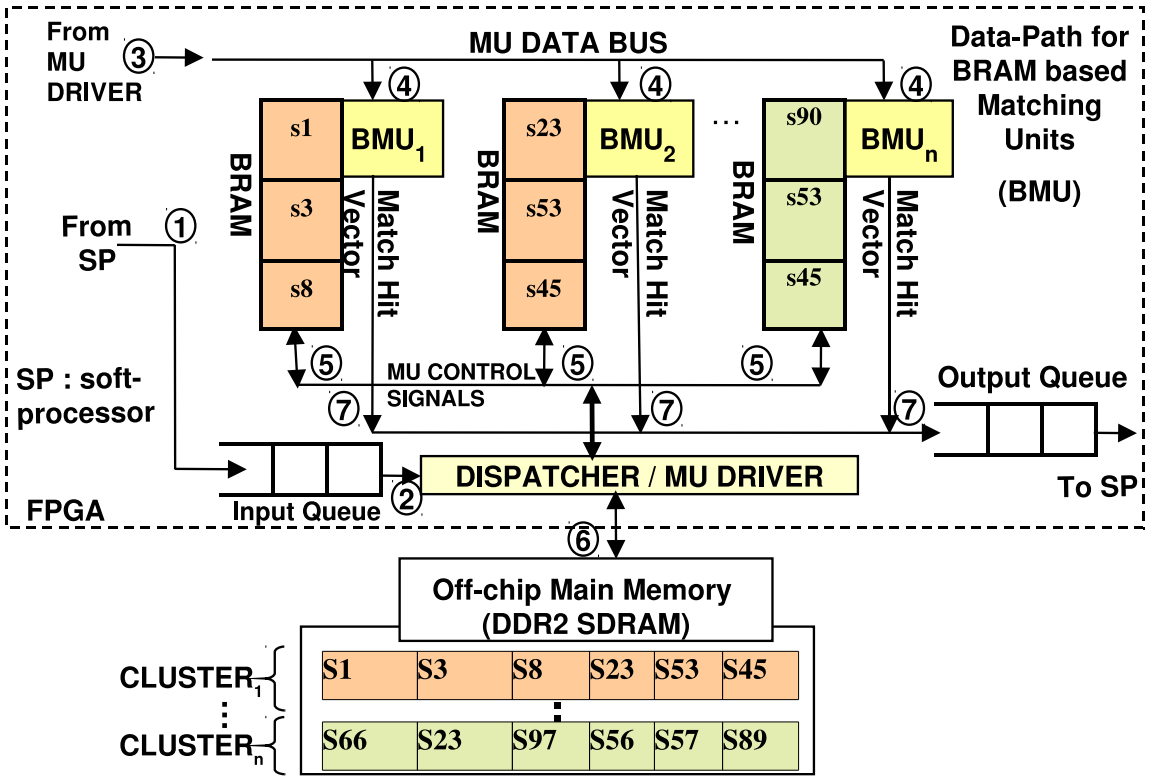


Tuning for Flexibility



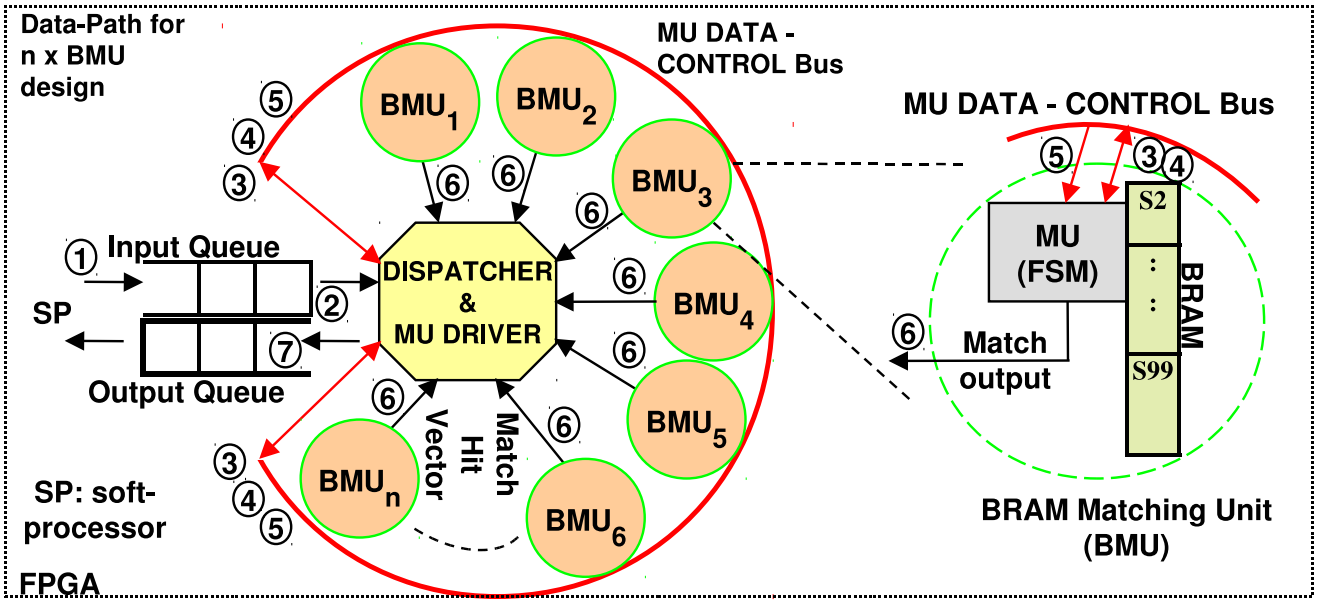
1. Eliminate software-to-hardware porting effort or the need for specialized hardware knowledge
2. Compile and execute the original PC source code on FPGA soft-core processors

Tuning for Adaptability



1. Employ a shared memory model to store propagation data structure
2. Support up to four matching units (custom processors) in parallel (parallelism limited by the off-chip memory-to-processor bandwidth)
3. Scale up to hundreds of thousands of subscriptions and support subscription updates

Tuning for Scalability



1. Inherit most of the benefits of *tuning for adaptability design*
2. Obtain an unprecedented level parallelism through horizontal data partitioning
3. Assign each matching unit a dedicated on-chip memory to minimize processor idleness
4. Realize full memory-to-processor bandwidth match via direct interconnect to dedicated memory units

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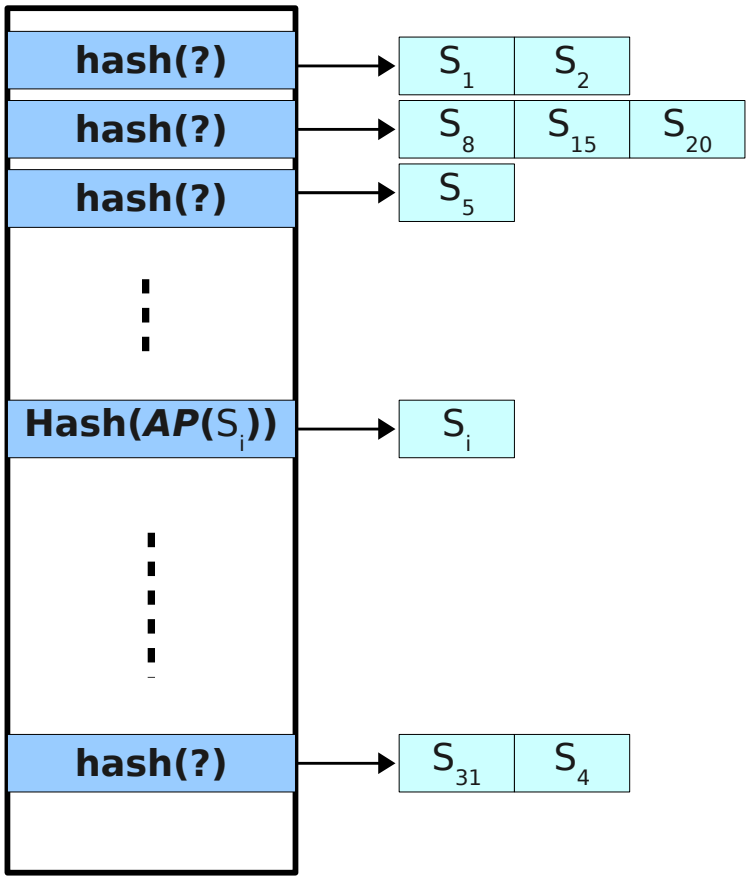
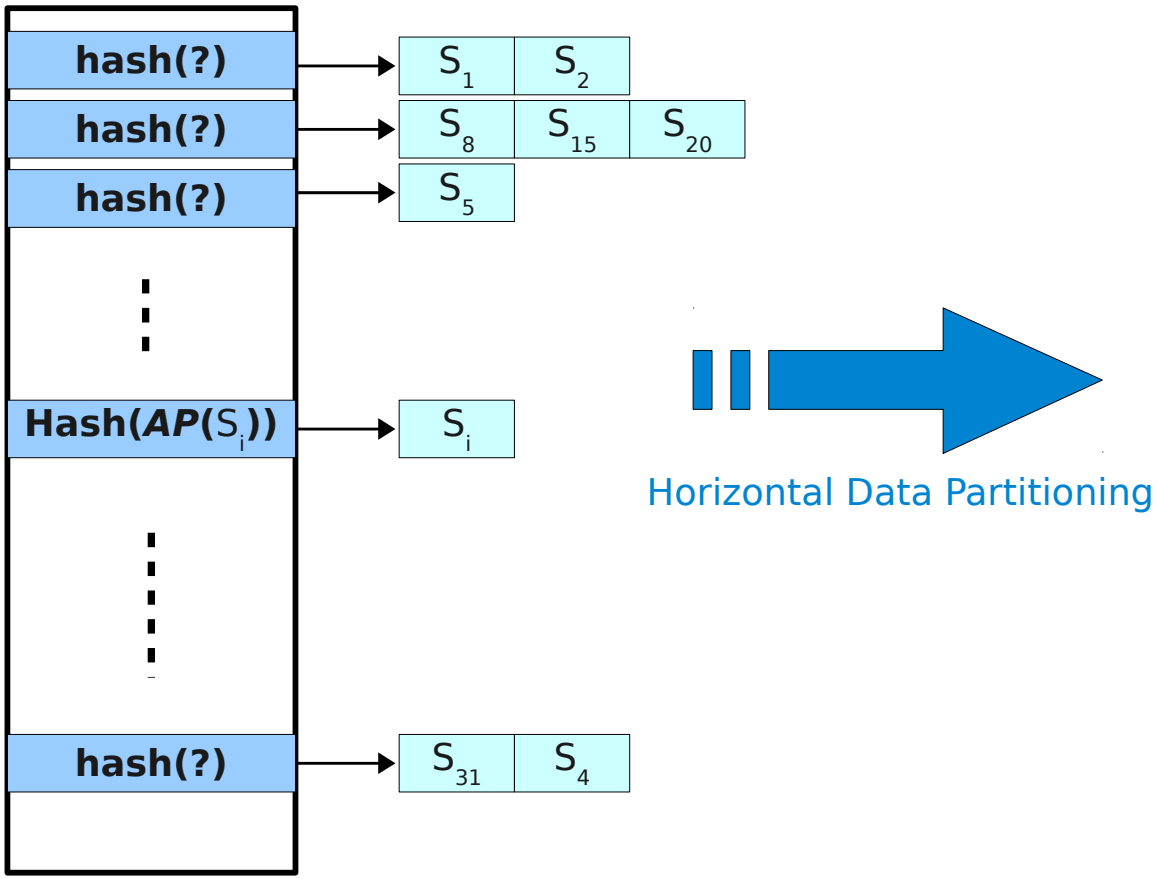
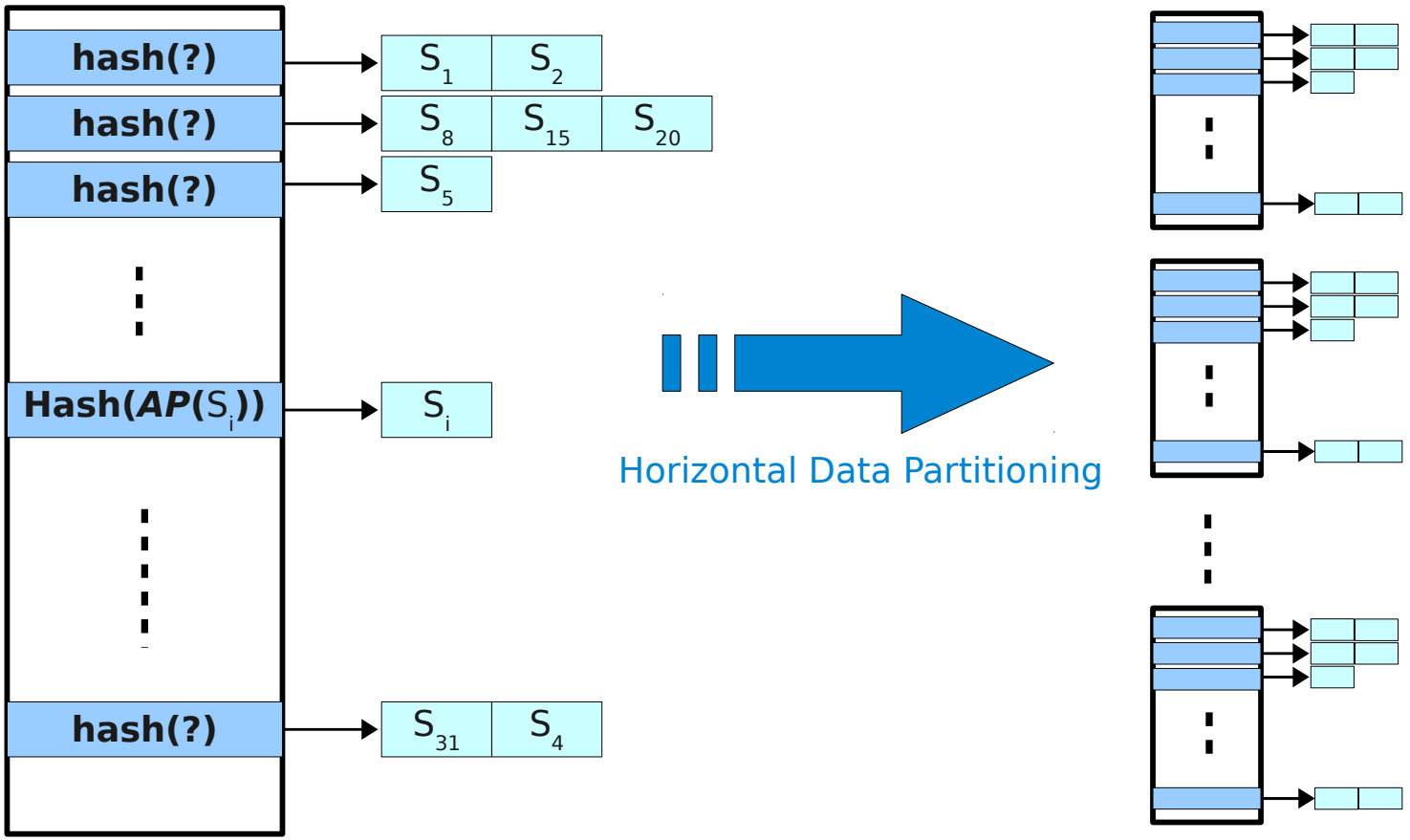
Horizontal Data Partitioning



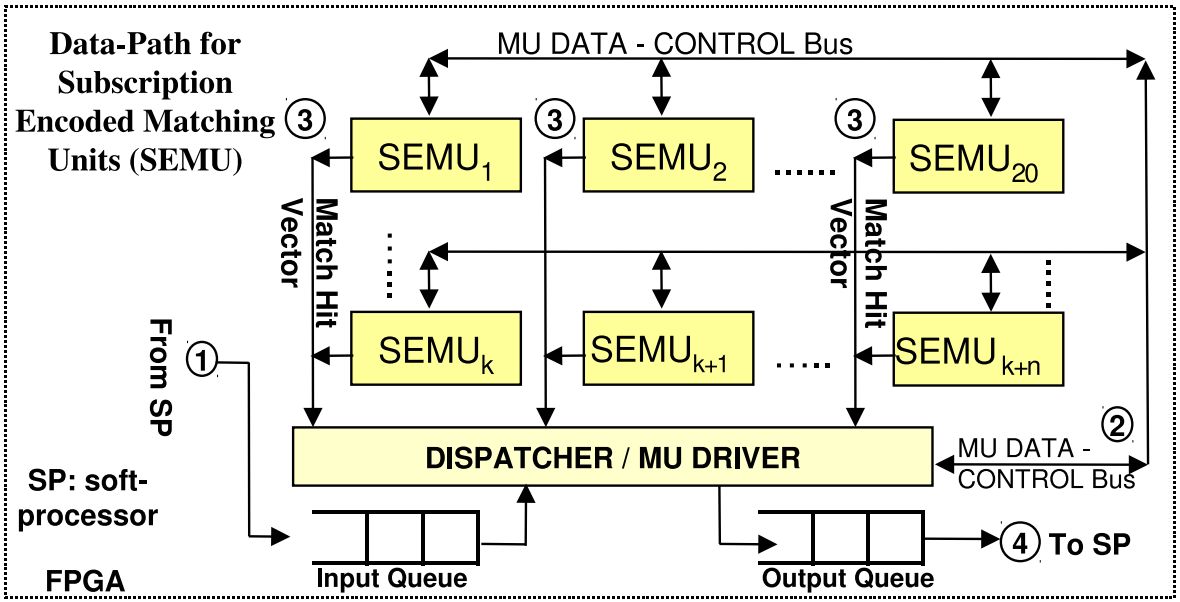
Horizontal Data Partitioning



Horizontal Data Partitioning



Tuning for Performance



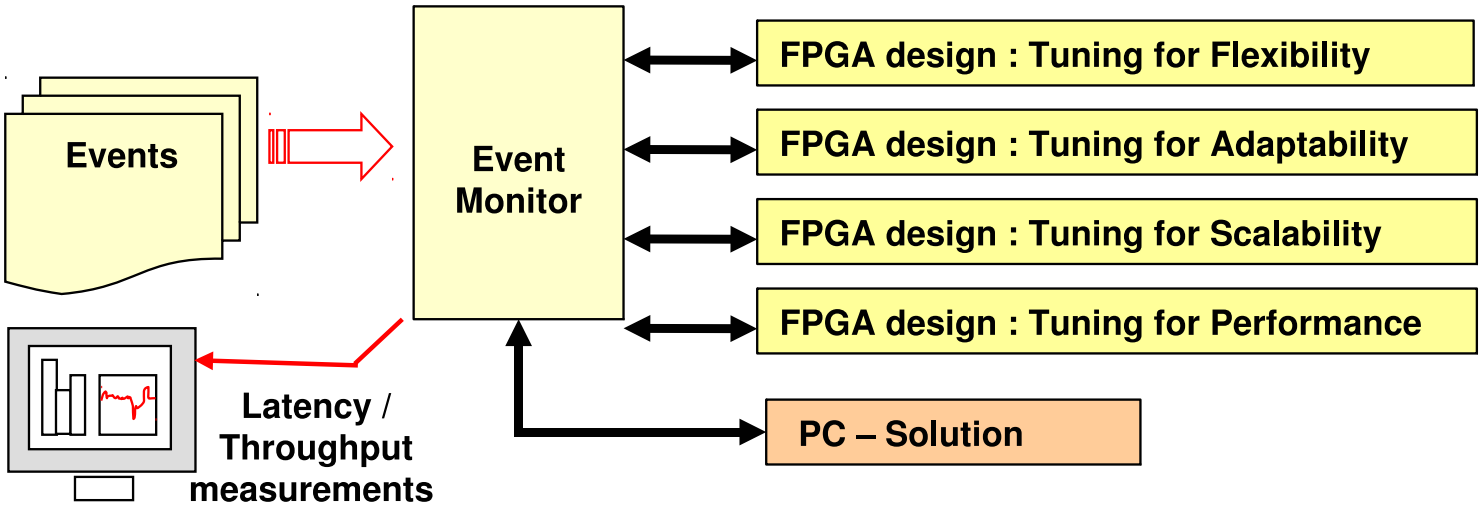
1. Encode each subscription as a matching unit (a custom processor)
2. Sustain a high rate of matching due to lack of memory access
3. Achieve a highest degree of parallelism, since all subscriptions are executed in parallel
4. Scale up to hundreds of subscriptions

Evaluation Design Space

Different Approaches

1. **PC:** PC Solution
2. **Flexibility:** FPGA embedded system (soft-core)
3. **Adaptability:** FPGA matching units (processors) + off-chip main memory
4. **Scalability:** FPGA matching units (processors) + on-chip main memory + horizontal data partitioning
5. **Performance:** Hardware encoded data + no on-/off-chip memory

Evaluation Testbed



1. **Throughput** is the maximum sustainable input packet rate, determined through a bisection search, when no packets is dropped.
2. **Latency** is the interval between the time an event packet leaves the Event Monitor output queue to the time the action is received.

Effect of the # of Matching Units (MUs) vs. Latency (μs)

Scalability Design Results

Workload	1x MU	4x MUs	32x MUs	128x MUs
250	7.5	5.5	5.0	**3.6**
1K	9.3	6.1	4.3	**4.3**
10K	64.0	19.0	6.8	**5.4**
50K	223.5	59.9	12.3	**7.3**

Effect of Workload Size vs. End-to-end Latency (μs)

Workload	PC	Flexibility	Adaptability	Scalability	Performance
250	**53.9**	71.0	6.4	**3.6**	**3.2**
1K	**60.7**	199.4	7.5	**4.3**	N/A
10K	**150.0**	1,617.8	87.8	**5.4**	N/A
100K	2,001.2	16,422.8	1,307.3	N/A	N/A

System Throughput (events/sec)

Workload	PC	Flexibility	Adaptability	Scalability	Performance
250	**122,654**	14,671	282,142	**740,740**	**1,024,590**
1K	**66760**	5,089	202,500	**487,804**	N/A
10K	**9594**	619	11,779	**317,460**	N/A
100K	511	60	766	N/A	N/A

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Percentage (%) of Line-rate Utilization

Workload	PC	Flexibility	Adaptability	Scalability	Performance
250	**7.45**	0.89	17.15	**45.04**	**62.29**
1K	**4.01**	3.09	12.31	**29.66**	N/A
10K	**0.58**	0.04	0.72	**19.30**	N/A
100K	0.031	0.01	0.05	N/A	N/A

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   - leverage on-board packet processing
3. Effective data placement of subscriptions
   - horizontally partition the data (propagation data structure)
   - increase the memory bandwidth
   - maximize the level of parallelism
4. Other FPGAs benefits
   - cost-effective
   - energy-efficient

Thank You,