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INVITED PAPER

Towards large scale CMOS single-photon detector arrays for lab-on-chip applications

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Abstract

Single-photon detection is useful in many domains requiring time-resolved imaging, high sensitivity and high dynamic range. In this paper the miniaturization and performance potential of solid-state single-photon detectors are discussed in the context of lab-on-chip applications where high accuracy and/or high levels of parallelism are suited. Technological and design trade-offs are discussed in view of recent advances in integrated LED matrix technology and the emergence of new multiplication based architectures.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

With the emergence of ultra-fast, time-correlated optical sensing techniques, there has been an increasing need for multi-pixel imagers capable of resolving single photons at picosecond accuracy with high signal-to-noise ratios and high dynamic ranges. Recent research in imaging has especially benefited biology, medicine and environmental monitoring, yielding a number of new instruments and tools.

The new developments range from multiphoton microscopy [1], to voltage sensitive dye (VSD) based imaging [2, 3], particle image velocimetry (PIV) [4], instantaneous gas imaging, [5, 6], etc. Fluorescence-based imaging (both single and multiphoton) is perhaps the research direction that has most influenced the development of fast and sensitive optical detectors [7–9]. Examples of techniques in this class include Förster resonance energy transfer (FRET) [10], fluorescence lifetime imaging microscopy (FLIM) [7, 11], and fluorescence correlation spectroscopy (FCS) [12–14]. The success of these techniques, particularly FLIM, derives from the ability to characterize an environment based on the time-domain behaviour of certain fluorophores with high resolution in space domain. This characterization can be done today with high levels of accuracy in 3D with minimal interference from the surroundings and almost no dependence on fluorophore concentration.

Thus far, in many time-resolved and/or high-sensitivity applications the detectors of choice have been photomultiplier tubes (PMTs) and multichannel plates (MCPs) [1, 15]. While these devices can reach time uncertainties of a few tens of picoseconds, usually multi-pixel images are not possible without bulky setups and expensive equipment. Thus, high sensitivity and/or time-resolved imaging has been relegated to applications requiring important investments for optical and detector equipment.

As an alternative to PMTs and MCPs, researchers have turned to solid-state photon counters based on avalanche photodiodes (APDs). Implementations of such devices have existed since the 1960s. However, only recently have APDs operating in linear and Geiger mode been demonstrated in a CMOS process [16]. In the last four decades, solid-state multiplication based photodetectors have gradually evolved from relatively crude devices to the sophistication of today. Almost every imaging technology has one such device and the range of implementations is quite wide [17]. In this context, silicon APDs have recently attracted significant interest thanks to their relative simplicity and ease of fabrication.

There are two main lines of research in silicon APDs: one that advocates the use of highly optimized processes

to boost performance and one that proposes to adapt APD design to existing processes to reduce cost and to maximize miniaturization. Both approaches have advantages and drawbacks; however, the latter is perhaps the one that can potentially enable shorter time-to-market and a higher adaptability to miniaturized analysis systems.

In this paper we focus on this approach and we discuss how the latest advances in imaging CMOS processes may be used to maximize performance and boost miniaturization at the same time. We also discuss how advanced processes can ensure in-pixel and on-chip processing of ultra-high-speed signals that are typical of single-photon detectors. This is of particular importance in the design of systems based on the concept of lab-on-chip (LoC) or micro-total analysis system (μTAS). In such systems, the remaining obstacle appears to be the illumination device that is currently the object of intensive research.

Recent work aimed at the miniaturization of LED matrices and the integration of ultra-fast drivers is pointing towards the feasibility of a complete LoC and μTAS with performance comparable to that of conventional systems [18–21]. Significant advances in packaging and microfluidics seem to suggest that the convergence of biocompatibility, sample input and handling, excitation and detection could be commercially feasible in the near future.

2. Replacing PMTs

A number of solid-state solutions have been proposed as a replacement of MCPs and PMTs using conventional imaging processes. The challenge, though, has been to meet single-photon sensitivity and low timing uncertainty. To address the sensitivity problem, cooled and/or intensified CCDs [22] and ultra-low-noise CMOS APS architectures [23] have been proposed. Multiplication of photogenerated charges by impact ionization has also been used in CCDs [24].

Meeting PMT's picosecond timing uncertainty, however, to the best of our knowledge, has not been possible in non-streak CCD/CMOS imagers, even though uncertainties as low as 1 μs in CCD [25] and a few nanoseconds in CMOS active pixel sensor (APS) architectures [26] have been demonstrated. While CCD streak cameras can achieve a resolution of a few picoseconds, they require a 2D pixel array to resolve a string of photon arrivals. Moreover, long acquisition latency and the added complexity to form and deflect the photoelectron beam make this device unsuitable for miniaturization and low-cost operation. Special CMOS sensors that can reach timing uncertainties of a hundred or more picoseconds are possible today, but only when an optical peak power of a few tens of kilowatts is used as illumination source [27]. In addition, the complexity, size and power dissipation of the ancillary circuitry required by these imagers makes scaling a difficult proposition.

As an alternative PMT replacement, APD technology was also proposed some time ago [28]. In APDs, carriers generated by the absorption of a photon in the p–n junction, are multiplied by impact ionization thus producing an avalanche. APDs can reach timing uncertainties as low as a few tens of picoseconds thanks to the speed at which an avalanche evolves from the initial carrier pair forming in the multiplication region. An APD is implemented as photodiode reverse biased near or above breakdown, where it exhibits optical gains greater than one. When an APD is biased below breakdown it is known as *proportional or linear* APD. It can be used to detect clusters of photons and to determine their energy.

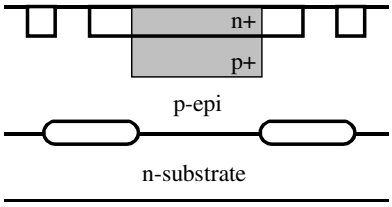

Figure 1. Cross-section of a typical APD (linear or Geiger mode). This device can in principle be fabricated in any conventional planar processes.

When biased above breakdown, the optical gain becomes virtually infinite. Thus, with relatively simple ancillary electronics, the APD becomes capable of detecting single photons. The APD operating in this regime, known as Geiger mode of operation, is called *single-photon avalanche diode* (SPAD). Individual detectors and detector arrays based on the SPAD technology have received renewed interest in recent years due to the versatility of their applications. Besides the aforementioned applications, SPADs have also been used in chemistry, physics, photonics and quantum communications. Of particular interest for SPAD technology, are currently quantum key distribution systems, where time-correlated measurements of single photons are necessary [29].

3. Single-photon detectors in standard processes

3.1. Basic structure design

There exist several implementation styles for APDs, of which two are the most used. In the first style, known as reach-through APD (RAPD), one builds a p+–π–p–n structure [30]. When reverse biased, the depletion region extends from the cathode to the anode. Thus, the multiplication region is deep in the p/n+ junction. Due to the depth of the multiplication region, this device is indicated for absorption of red and NIR photons up 1.1 μm (for silicon). Since the photoelectrons drift until the multiplication region, a larger timing uncertainty is generally observed.

The second implementation style is compatible with planar CMOS processes and it involves a shallow or medium depth p or n layer to form high-voltage pn junctions. Cova and others have investigated devices designed in this style since the 1970s, yielding a number of structures [31]. All these structures have in common a pn junction and a zone designed to prevent premature edge breakdown (PEB). An example of the early structures is shown in figure 1. In [32] n+/p+ enrichment in p-substrate was used, while PEB was prevented by confining p+ enrichment in the centre of the APD.

More recently, many authors have developed APDs, both in linear and Geiger mode, using dedicated planar and non-planar processes, achieving superior performance in terms

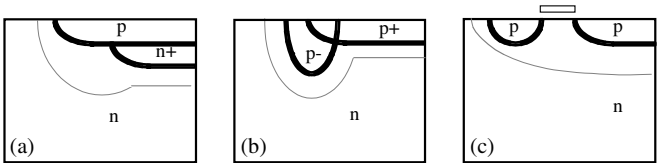

Figure 2. Techniques for prevention of PEB in a planar process.

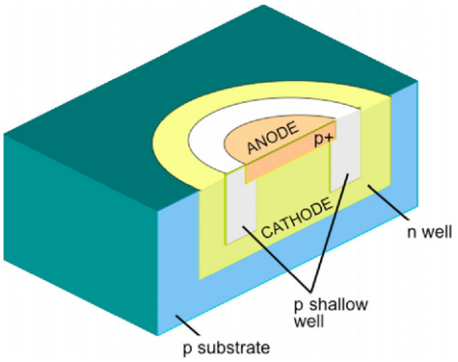

Figure 3. Cross-section of a SPAD. A guard ring structure preventing premature discharge may be implemented using a shallow well.

of sensitivity and noise. A good example is the work of Kindt [33]. As mentioned earlier, the main disadvantage of using dedicated processes is generally the lack of libraries that can support complex functionalities and deep-submicrometre feature sizes, thus limiting array sizes.

An interesting alternative is the use of a hybrid approach whereby the APD array and ancillary electronics are implemented in two different processes, each optimized for APD performance and speed, respectively [34]. If the ancillary electronics is implemented in CMOS, high degrees of miniaturization are possible. The price to pay is increased fabrication complexity.

In 2003 the integration of linear and Geiger mode APDs in a low-cost CMOS process became feasible [16,35]. One of the main challenges is the PEB prevention. This is done by design forcing the electric field everywhere to be lower than that on the planar multiplication region, where it should be uniform. Figure 2 shows some of the most used structures. In (*a*) the n+ layer maximizes the electric field in the middle of the diode. In (*b*) the lightly doped p implant reduces the electric field at the edge of the p+ implant. In (*c*) a floating p implant locally increases the breakdown voltage. With a polysilicon gate one can further extend the depletion region (grey line in the figure).

Figure 3 shows a 3D cross-section of the structure depicted in figure 2(*b*). This implementation assumes a p-substrate and an n-well isolation. There are several advantages in using an n-well. First, photocharges generated in a given pixel cannot cause avalanches in neighbouring pixels, thus minimizing electrical crosstalk. Second, only photocharges relatively near the multiplication region can trigger an avalanche, thus minimizing timing uncertainty. The main disadvantage is a set of tighter separation rules, thus reducing pixel packing potential of a given technology, fill factor and, ultimately, pixel pitch.

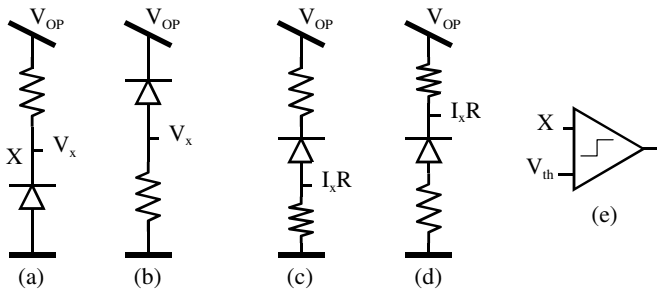

Figure 4. Passive quenching variants. Voltage detection mode (*a*), (*b*); current detection mode (*c*), (*d*); pulse shaping (*e*).

Modern imaging processes provide several lightly doped implants at three or more depths. Thus, an optimal layer combination (p+/p−/n-well) generally exists that can yield a good trade-off between timing uncertainty and noise. However, care must be used to avoid full depletion of the well and punch-throughs between shallow wells and substrate. Buried layers should also be used with care to prevent punch-through across the n-well.

3.2. Quenching and recharge

Linear APDs are multiphoton detectors, when used as charge accumulators. In this case, the charges generated at each avalanche are integrated and subsequent amplification may not be needed. In single-photon detection mode, fast amplifiers should be used, adding to jitter and dark noise.

SPADs in contrast can only operate in single-photon mode. This is achieved operating the diode *above* breakdown by a voltage known as *excess bias voltage*. In this bias state the photodiode exhibits a virtually infinite optical gain. Thus upon photon absorption, an avalanche may be triggered involving a sufficient number of charges to be easily detected and thus requiring no further amplification. However the avalanche needs be quenched.

There exist two main quenching mechanisms: *passive* and *active*. In passive quenching the avalanche current itself is used to drop the voltage across the diode. This is generally accomplished via a ballast resistor placed on the anode or the cathode of the diode as shown in figure 4. The detection of the avalanche can be accomplished by measuring the voltage across the ballast resistance (figures 4(*a*) and (*b*)) or the current across a low- or zero-resistivity path (figures 4(*c*) and (*d*)). Pulse shaping may be performed using a comparator (figure 4(*e*)). In these cases, excess bias voltage V_e satisfies the following equation:

$$V_e = |V_{OP}| - V_{bd}, \tag{1}$$

where V_{bd} is the true breakdown voltage. The resistances can be implemented in polysilicon [35,36] or using the non-linear characteristics of a biased PMOS or NMOS [37,38].

In active quenching mode, the avalanche current is used to actively stop the avalanche. The literature on active quenching is extensive. In [39] some of the existing schemes can be found. Other authors in the imaging community have recently revisited the issue [40]. After quenching, the device enters

another phase known as recharge. During this phase the photodiode bias voltage must return to the pre-avalanche state as quickly as possible. Again, there are passive and active schemes to achieve recharge. The simplest approach is shown in figure 4. The diode will automatically recharge to V_{OP} via the ballast resistance. The recharge, in this case, follows the *RC* exponential, where R is the equivalent quenching resistance and C the total parasitic capacitance at node X.

In active recharge schemes, the photodiode is forced to the initial state generally via a fast switch controlled by a current sense amplifier. Even though these schemes are attractive, they usually require extra complexity to a pixel, thus potentially hindering miniaturization. The quenching and recharge times are collectively known as *dead time*. Dead time in passive quenching/recharge methods is potentially longer than in their active counterparts. However, the advantage of a reduced dead time in large array may be reduced by limited speeds of pixel readout schemes.

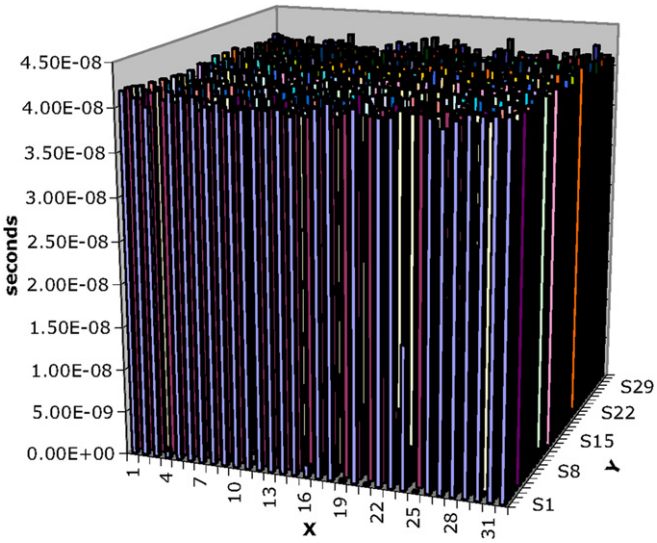

Figure 5. Typical dead time non-uniformity across the chip at room temperature.

4. Performance issues

CMOS APDs are characterized by the same parameters as conventional photodiodes, except for an optical gain higher than one. APDs operating in Geiger mode, in contrast, require a new set of parameters. In addition, due to the geometry of guard rings for PEB prevention, in SPADs the fill factor may be as low as 1%. Using modern readout techniques, fill factors of up to about 9% have been demonstrated [41]. We have also demonstrated a fill factor reclaim factor of 15 using commercial microlense arrays [42]. However, other means such as digital Fresnel and surface plasmon concentrators may be used in the future.

Dead time. In passive quenching/recharge devices dead time is generally dominated by the recharge time and it varies a few percentage points across the array as a function of temperature and process variability. This results in mild saturation non-uniformity and time variability. Figure 5 shows dead time over a sample of 1000 pixels in an area of $2 \times 2\,\text{mm}^2$.

Time uncertainty or jitter. In integrated SPADs jitter is limited from below by geometry and process technology considerations. In arrays of significant size, jitter generally degrades due to added electrical path to output and electrical supply ripple caused by surrounding pixels. Techniques derived from memory design, such as non-rail-to-rail readout and shielding should be exploited. Figure 6 shows typical timing behaviour of a SPAD upon pulsed laser exposure when surrounded by active neighbours exposed to the same illumination. Note that this behaviour is consistent with a count rate that is significantly below saturation.

With increasing count rates, the effective jitter tends to degrade. Such degradation is due to the increase in the probability that photons are detected at the last instants of the dead time. The detection of such photons, known as *twilight photons*, may require ten to several tens of nanoseconds, thus the increase in the overall time uncertainty.

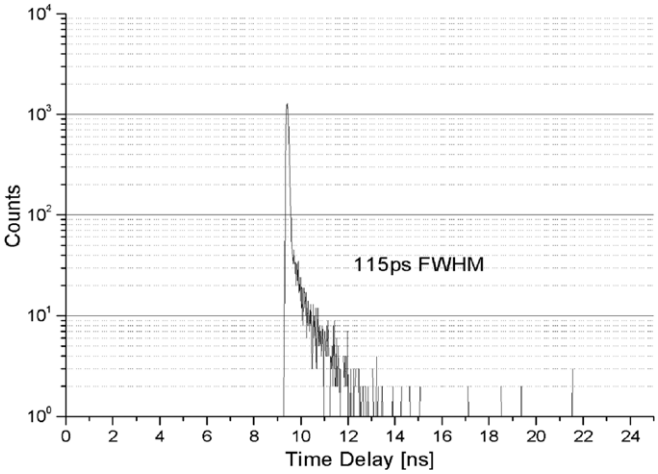

Figure 6. Time uncertainty in integrated SPADs fabricated in CMOS technology. In this case a full width at half maximum (FWHM) of 115 ps was measured.

Photon detection probability. The sensitivity is characterized in SPADs as photon detection probability (PDP) and it is the overall probability that an impinging photon triggers a digital pulse. Detailed physical models for PDP and its mechanisms can be found in [35]. PDP is dependent on temperature and excess bias voltage. A good pixel-to-pixel uniformity is generally observed, while column-wise PDP variability is usually absent [38]. Based on on-going research, we expect that deep-submicrometre SPADs will achieve up to 40–50% PDP [43]. With use of more advanced deep-submicrometre processes, the multiplication region will tend to move towards the surface and get thinner. As a result, the trend towards shorter wavelengths will be reinforced. Figure 7 plots PDP as a function of wavelength for two CMOS technologies.

Dark count rate. Dark counts, characterized in terms of average dark count rate (DCR) is a function of detector area.

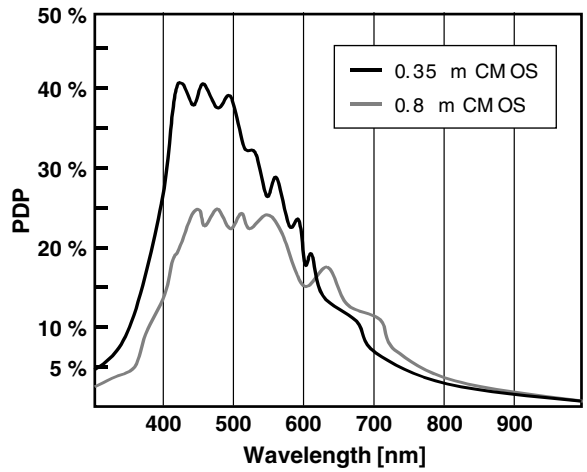

Figure 7. PDP as a function of impinging radiation wavelength for two CMOS processes.

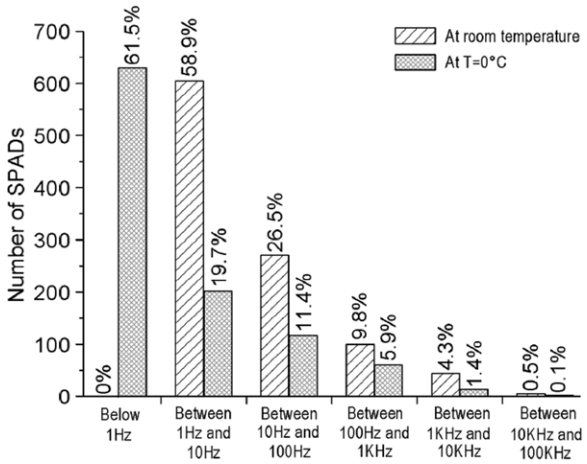

Figure 8. DCR distribution across an array as a function of temperature for a fix excess bias.

It is also a function of temperature and excess bias voltage. On a large chip, DCR may vary widely from a minimum of a few Hertz to a few kilohertz. Generally, noisy pixels are less than 1% of the array, depending upon the distribution of traps across the chip and the overall quality of the process. Hence, it is always good practice to foresee means to shut off pixels either temporarily or permanently, depending on applications. Figure 8 shows the distribution of DCR across 1000 locations as a function of temperature.

Afterpulsing. Afterpulses are generally defined as counts occurring at the end of the dead time that are caused by a previous photon detection event. Afterpulses are the result of secondary avalanches triggered by lingering carriers that were generated in the primary avalanche. Afterpulses may also be caused by a twilight photon. While ordinary afterpulses are dependent on implementation and technology, twilight counts vary with the count rate and hence can be easily isolated [44].

The mechanisms behind ordinary afterpulsing are relatively well understood and the literature on the subject is extensive. Even though active recharge schemes are attractive, a minimum recharge time is to be allocated in every technology

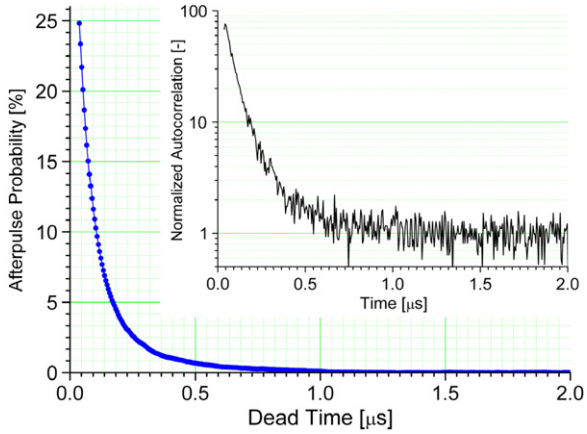

Figure 9. Afterpulsing probability in SPADs. The inset plots the raw autocorrelation function of the device fabricated in CMOS technology.

Table 1. Performance of typical CMOS single-photon avalanche diodes at room temperature.

Measurement	Min.	Typ.	Max.	Unit
Fill factor	1		10	%
Timing uncertainty or jitter	50		145	ps
DCR (pixel-wide mean at RT)	5		780	Hz
Pixel pitch	25		58	μm
V_{OP}	10		23	V
Dead time		40		ns
PDP at 550 nm		41		%
EM spectrum (PDP $>1\%$)	380		900	nm
Saturation count		25		MHz

to allow for a single-photon detector to recover from an avalanche. Fewer impact ionizations and fewer traps can reduce this time. However, since the process of afterpulsing is stochastic in nature, it is not feasible to eliminate it completely. Alternatively, one must design the recharge mechanism to ensure minimum afterpulsing probability. Figure 9 shows a plot of afterpulsing probability as a function of dead time at room temperature [45].

Crosstalk. Crosstalk is also a stochastic process, due to optical and electrical causes. In optical crosstalk the luminescence released by an avalanche elsewhere causes secondary avalanches, thus causing cross-correlated pixel firing. In electrical crosstalk, a carrier generated elsewhere may trigger an avalanche, thus again causing cross-correlated firing. The techniques proposed for pre-empting optical crosstalk include optical shields between pixels and means to prevent stray illumination [28]. Electrical crosstalk can be strongly reduced insulating the multiplication region, for example, via a well. The drawback of this approach is the reduction of fill factor or the increase in overall pitch.

Table 1 summarizes the most important parameters characterizing SPADs for high-density arrays. The data are based on our experience with three CMOS processes. Note that in our measurements inter-pixel crosstalk was always negligible; however, other authors have reported non-zero values for other processes.

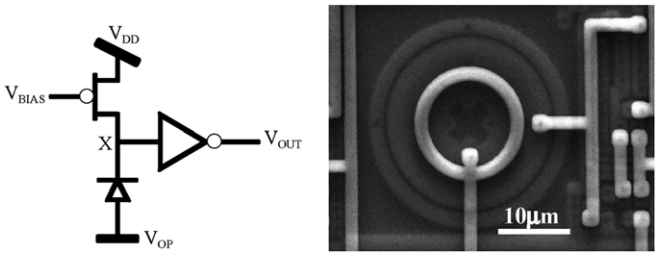

Figure 10. SPADs in CMOS: schematic (left); SEM micrograph (right). The ballast resistor can be implemented with a PMOS or NMOS, the comparator with a properly sized inverter.

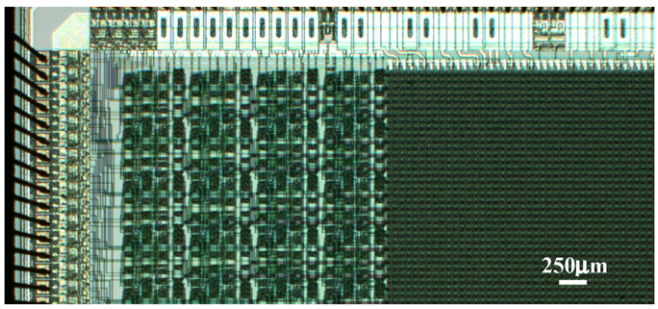

Figure 11. Example of SPAD array (right-hand side of micrograph) combined with complex digital circuitry (left-hand side of micrograph). The digital circuit was synthesized automatically with commercial tools.

5. System miniaturization for LoC and μTAS applications

5.1. Detector miniaturization

The first SPAD implementations in 0.35 μm CMOS technology [46] have demonstrated fully scalable pixels at a pitch of 25 μm. Pixel miniaturization has other benefits too. As mentioned earlier, the reduction of anode and cathode areas in SPADs generally reduces DCR [35]. It also reduces the parasitic capacitance at node X in figures 4 and 10, thus possibly reducing dead time. In addition, the number of carriers involved in an avalanche is also reduced, thus decreasing the probability of carrier trapping and, consequently, of afterpulsing. Finally, fewer carriers involved in impact ionization will cause smaller photon emission during the avalanche and thus less optical crosstalk.

Figure 10 shows a possible implementation of a SPAD that ensures compatibility with conventional CMOS processes thanks to a properly biased quenching transistor and an inverter used *in lieu* of the comparator. The inverter input voltage is made to switch between 0 V and V_{DD}. One of the advantages of simple configurations such as this is that one can incorporate a SPAD in a digital circuit whereby the remainder of it is based on standard cells and can be synthesized, placed, routed and verified using automated or semi-automated tools. A design obtained in this way was demonstrated, for example, in [47]. Figure 11 shows a detail of the design.

APD arrays can also be used for multiphoton detection if the output of each pixel (V_{OUT} in figure 10) is connected as an N-to-1 OR gate or a current summing device. This configuration can be achieved effectively, for example, with the schematic shown in figure 12.

V_{OUT} is the voltage output of this composite detector. Alternatively, a current output signal can be produced.

5.2. System miniaturization

One of the main challenges of single-photon detector based systems is the readout. In general, linear APDs can be read out using a conventional scheme, similar to CMOS APS architectures. SPADs on the contrary, may generate a digital pulse for each absorbed photon. To avoid missing photon counts, a counter can be used in each pixel [48]. However, large counters are not desirable due to the fill factor loss and/or extra time required to perform a complete readout of the contents of the chip. A partial solution to this problem is the reduction of the counter resolution (ultimately 1 bit), requiring more frequent readouts and/or lower saturation. Another solution is to access every pixel independently but sequentially using a digital random access scheme [36, 37].

In low-light-level (LLL) applications, such as in bioluminescence setups, one can use an *event-driven* readout, where the detector initiates and drives a column-wise detection process directly [46, 47]. The drawback of this approach is that multiple photons cannot be detected simultaneously on the same column. In addition, the bandwidth of the column readout mechanism limits saturation levels of the entire column. These limitations are not problematic if the expected photon flux hitting the sensor is low. An example of a setup where this kind of detector array could be used is shown in figure 13.

An alternative approach for non-LLL situations is the use of a *latchless pipeline* scheme. In this approach, the absorption of a photon causes the SPAD to inject a digital signal into a delay line that is then read externally. The timing of all injected pulses is evaluated so as to derive the time-of-arrival of the photon and the pixel of origin [41]. This method allows detection of photons simultaneously over a column even though some restrictions apply on the timing of the optical set up. Figure 14 shows the photomicrograph of an implementation of this readout style. Note that in this design an effective gating mechanism is necessary to prevent photons detected outside a certain time window being interpreted as originating in a pixel other than the one responsible for that detection.

The pixel access problem can be overcome if the photon time-of-arrival is performed *in situ*, i.e. on the pixel itself. The main problem with this approach is the physical size of circuitries capable of discriminating a few tens of picoseconds several millions times per second. While researchers have used on-pixel time-to-amplitude converters (TACs), they can be large [49, 50]. However, the research activity in this field is extensive and massively parallel TACs and their digital equivalent, time-to-digital converters (TDCs), are expected in the near future. Recently, steps towards this goal have already been accomplished [51].

Combining optical detection and other functionalities on the same substrate for LoC and μTAS applications is

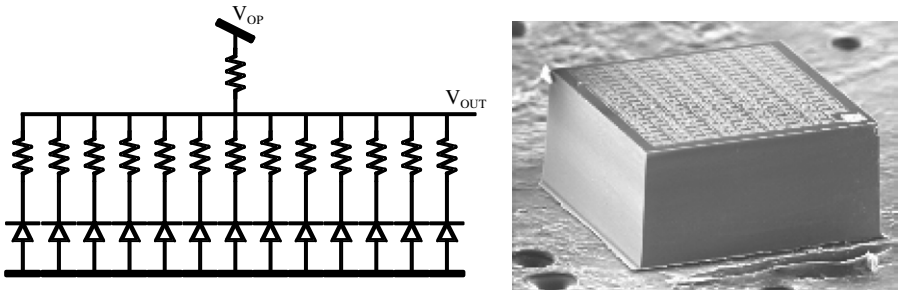

Figure 12. Integrated APD array in common anode configuration, known as *silicon photomultiplier* (courtesy of SensL): schematic (left); implementation (right).

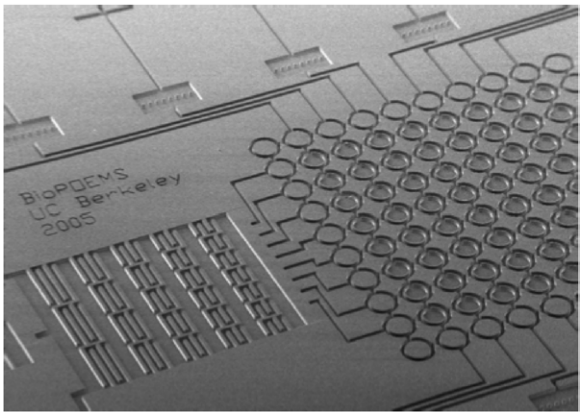

Figure 13. Example of microfluidic multi-reactor μTAS BioPOEMS (courtesy of Luke Lee, U C Berkeley).

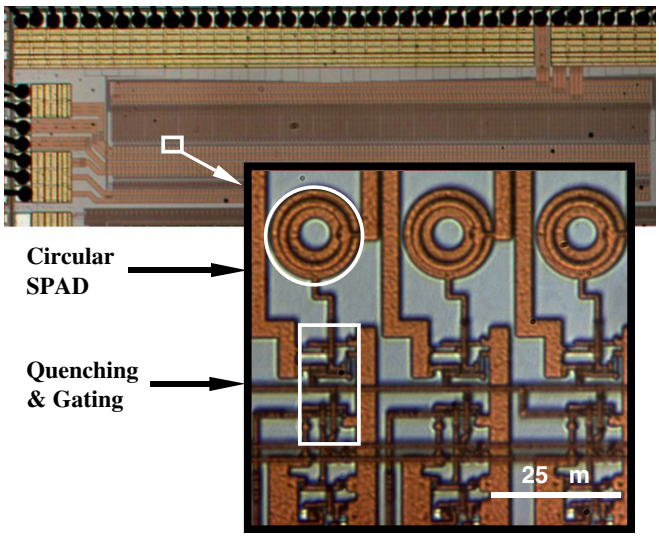

Figure 14. Photomicrograph of a single-photon detection system based on latchless pipeline readout.

also being researched quite extensively. Among the most promising developments, Lehmann *et al* have proposed the use of SPADs integrated on the same substrate with magnetic actuation devices [52]. In this work, single-photon detectors were selected due to their high dynamic range, necessary to detect small particles in a condition of high illumination. In addition, the insensitivity of *in situ* SPADs to magnetic fields and humidity made them ideal for use in wet environments with magnetically actuated bio-material. More recently, Brae *et al* have proposed a μTAS whereas a micro LED array operating in near UV is bump-bonded to a CMOS SPAD array [53]. In this work, a time-correlated single-photon counting (TCSPC) based setup is used without dichroic filters to measure the lifetime of quantum dots for uses in bioimaging applications.

6. Conclusions

The research and development of integrated APD technology has proceeded at great speed in the last years. While pixel pitch has tracked Moore's law, it still lags behind that of CCD and CMOS APS. The main challenge towards miniaturization is geometry and process optimization to yield high compactness while not excessively degrading performance. Geiger mode APDs could become even more relevant in the future especially in LoC and μTAS applications requiring low cost, high performance and short time-to-market.

Acknowledgments

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