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Towards large size substrates for III-V co-integration made by direct wafer bonding on Si

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We report the first demonstration of 200 mm InGaAs-on-insulator (InGaAs-o-I) fabricated by the direct wafer bonding technique with a donor wafer made of III-V heteroepitaxial structure grown on 200 mm silicon wafer. The measured threading dislocation density of the $In_{0.53}Ga_{0.47}As$ (InGaAs) active layer is equal to 3.5×10^9 cm^{-2}, and it does not degrade after the bonding and the layer transfer steps. The surface roughness of the InGaAs layer can be improved by chemical-mechanical-polishing step, reaching values as low as 0.4 nm root-mean-square. The electron Hall mobility in 450 nm thick InGaAs-o-I layer reaches values of up to 6000 cm^2/Vs, and working pseudo-MOS transistors are demonstrated with an extracted electron mobility in the range of 2000–3000 cm^2/Vs. Finally, the fabrication of an InGaAs-o-I substrate with the active layer as thin as 90 nm is achieved with a Buried Oxide of 50 nm. These results open the way to very large scale production of III-V-o-I advanced substrates for future CMOS technology nodes. [http://dx.doi.org/10.1063/1.4893653]

The availability of InGaAs on large scale wafers (200 mm and more) is a prerequisite for the co-integration of III-V materials (n-FETs) with silicon or SiGe (p-FETs) in future CMOS technology nodes. Contrary to other approaches, like aspect ratio trapping (ART), for example,[1–3] the direct wafer bonding (DWB) combines the possibility to cointegrate n- and p-FETs at the small pitch of 50 nm and with a minimum height difference between the III-V and the SiGe(Si) layers using the "on insulator" approach. Thanks to the presence of the buried oxide (BOX), our substrates benefit of all the advantages of the SOI technology.

DWB has been proven as a possible path to obtain InGaAs-o-I structures that are required for ultra-thin body and buried oxide (UTBB) Fully Depleted-o-I or FinFET devices. Ultra-thin InGaAs-o-I were already fabricated by DWB using InP wafer as donor substrate.[4–8] InGaAs layers directly grown on InP substrate present indeed a very low RMS surface roughness and thus can easily be transferred onto Si substrate via DWB. The use of Hydrogen implantation in a Smart Cut™ process was also proposed as a possible path to transfer the active layer of InGaAs and to recycle the donor wafers.[7] Moreover CMOS circuits were demonstrated using hybrid substrates comprising InGaAs- and SiGe-o-I,[8] allowing the fabrication of n-FET and p-FET on the respective high mobility channels. Unfortunately, the lack of 200 mm or larger InP donor wafers limits this process to research demonstration. InGaAs directly grown on Si with a thick buffer layer was reported earlier and found to have excellent metrics in blanket films and for devices such as FinFETs or heterojunction bipolar

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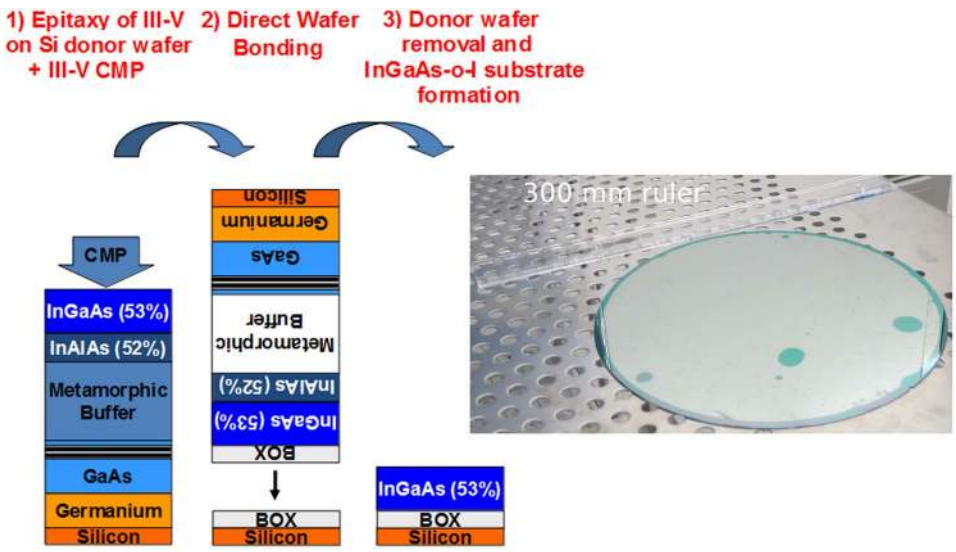

FIG. 1. The fabrication process flow consists in doing the CMP directly on InGaAs and depositing an ultrathin BOX prior to DWB and transfer. A picture of a 200 mm InGaAs-o-I is shown.

transistors (HBTs).[9,10] However, due to the large lattice parameter mismatch between Si and InGaAs (approximately 8%), the surface roughness of the as-grown InGaAs is in the range of few nanometers RMS, and it is not compatible with the DWB process (roughness must be less than 0.6-0.7 nm RMS). We smoothed the InGaAs surface down to sub-nanometric RMS roughness by using the chemical-mechanical-polishing (CMP) technique without affecting the structural quality of the layer. Such flattened InGaAs layer, grown on Si substrates can then be transferred by DWB to a Si receiver wafer, forming InGaAs-o-I on large Si substrate (200 mm or more). The deposition of a 20–30 nm thin Al_2O_3 BOX on both InGaAs surface and Si receiver wafer ensured a high bonding energy even at low temperature (<300 °C).[11] In addition, a post-transferred CMP step can be implemented to further reduce the thickness of InGaAs-o-I layer to values compatible with device fabrication. We therefore demonstrate that advanced hybrid InGaAs-SiGe-o-I substrates can be fabricated on large diameter wafers, combining the advantages of the SOI technology (low power, back biasing) with the high performance expected from high mobility InGaAs and SiGe channels.

The fabrication process of the InGaAs-o-I substrate by DWB is reported in Fig. 1. The donor wafer consists of InGaAs grown by Molecular Beam Epitaxy (MBE) on 200 mm Si (100) substrate, with a 6° offcut towards ⟨111⟩ direction to suppress the formation of antiphase domains. Prior to the top 500 nm thick InGaAs layer, a composite buffer is grown, made of a 2.5 μm Ge layer directly on the Si substrate, followed by a 0.5 μm buffer made of GaAs (100-150 nm)/n x GaAs (5 nm)-AlAs (5 nm)/GaAs (100 nm) and finally a 1.5-2 μm $In_xAl_{1-x}As$ metamorphic buffer (MB), with $5 \leq n \leq 20$. The In-content for the MB is linearly graded between approximately 10% and 60% and ended by an inverse step with an alloy composition matched to $In_{0.53}Ga_{0.47}As$, similar to Ref. 12. Details on the growth conditions will be reported elsewhere. Since the final roughness of the donor wafer (RMS ∼6-8 nm) does not allow for DWB, the process flow consists in doing a CMP step directly on the InGaAs active layer, to reduce its surface roughness down to 0.4 nm RMS, followed by the deposition of a 30 nm Al_2O_3 BOX by Atomic Layer Deposition (ALD) (Fig. 1). To obtain a high bonding energy, a 20 nm Al_2O_3 BOX is also deposited on the 200 mm receiver Si (100) wafer. Prior to the Al_2O_3 BOX deposition, hydrofluorhydric acid (HF) treatment is performed on both, Si and InGaAs. To get clean and hydrophilic surfaces, a combination of megasonic waves rinsing (1 MHz) and Ozone rich water rinsing is used. Then, the donor and receiver wafers are immediately brought into contact and annealed between 200 °C and 300 °C for 2 h. Finally, the donor wafer is removed by a combination of wet and dry etching, resulting in a 200 mm InGaAs-o-I substrate (Fig. 1).

The crystalline quality of the InGaAs layer through the full process is controlled by high-resolution X-ray diffraction (HR-XRD) measurements (Fig. 2 left). The diffraction peak (hkl 004)

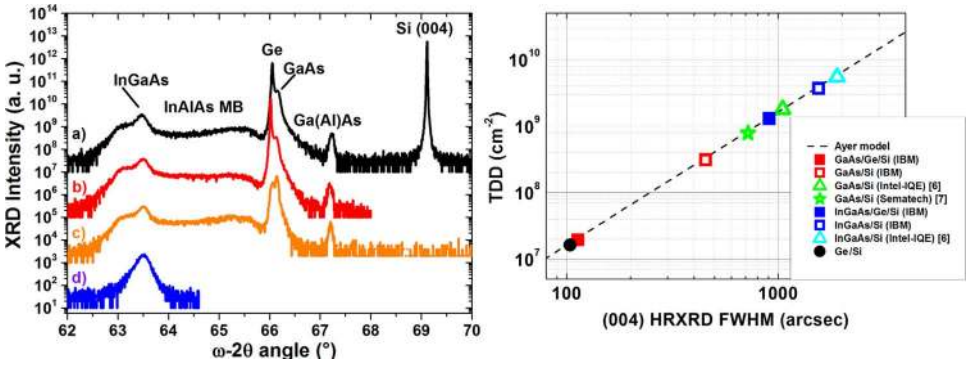

FIG. 2. (Left) HR-XRD ω-2θ scans of the InGaAs active layer after growth on Si (a, black), after DWB and etching of the Si donor wafer (b, red), after etching of the Ge layer (c, orange) and after removal of the Ga(Al)As superlattice, the InAlAs metamorphic buffer (d, blue). (Right) Threading dislocation density vs. rocking curves FWHM for different material layers grown on silicon. IBM samples, GaAs only or InGaAs with the GaAs buffer and InAlAs MB, have been grown in our MBE reactor, starting either from bare Si or from a 2.5 μm thick intermediate Ge layer grown on Si.

at approximately 63.5° corresponds to the InGaAs active layer and is the only peak remaining after DWB and removal of the donor wafer and its heterostructure. The shoulder at around 63.1° in Fig. 2 left (curves a–c) corresponds to InAlAs with In content above 52%. The absence of the Si peak after DWB and transfer is due to the 6° misalignment between the InGaAs active layer and the Si receiver wafer. The Full Width at Half Maximum (FWHM) of the rocking curves (RC) of InGaAs on the donor wafer is approximately 0.4°, and remains the same after DWB and transfer, which corresponds to a TDD of 3.5×10^9 cm^{-2}. This shows that the process does not further degrade the quality of the InGaAs active layer. The best values reported so far for InGaAs on Si virtual substrates are as low as 10^8 cm^{-2},[13] comparable to values reported for layers grown by the aspect ratio trapping (ART) method.[11–13] The density (D) of threading dislocation is calculated following the Ayers model:[14,15] $D = \beta^2/(4.36 \cdot b^2)$ with β the FWHM of the rocking curve [arcsec] and b the Burger vector [Å]. InGaAs and GaAs layers grown on Si with our MBE system, with (full square) or without (empty square) 2.5 μm thick Ge layer, compared with similar results by other groups are plotted in Fig. 2 right. The improvement in TDD thanks to the 2.5 μm thick Ge intermediate layer is clearly visible for both GaAs and InGaAs layers. Since the FWHM of the rocking curve is broaden by the number of dislocations and the presence of mosaicity in the crystal, the calculated D value is an overestimation of the real value.

The surface roughness of the InGaAs layer at different stages of the process flow was investigated by atomic force microscopy (AFM) and reported in Figures 3(a)–3(d). A tremendous improvement is observed after the InGaAs CMP step, decreasing from 8 nm down to 0.4 nm RMS. After the DWB and transfer process, the bottom interface of the as-grown InGaAs layer becomes the new top surface, whose roughness can also be reduced by a CMP step (Fig. 3(d)). The RMS for CMP on the transferred layer (Fig. 3(d)) is not as good as the value for CMP on the grown layer (Fig. 3(b)) because a different CMP tool and a not optimized process were used.

The cross-sectional scanning transmission electron microscope (STEM) micrographs at different stages of the process flow are displayed in Fig. 4. The InGaAs grown on Si is shown in Fig. 4(a). This structure can be bonded on Si doing first a CMP step of this as-grown InGaAs layer and then depositing a very thin Al_2O_3 BOX (Fig. 4(b)). After transfer, the InGaAs-o-I was flattened again by CMP. It is thus shown that a thin InGaAs-o-I substrate with a 50 nm thin BOX and a 90 nm thin InGaAs active layer can be obtained (Fig. 4(c)). Thinner InGaAs layer should be possible with this fabrication process and are currently under investigation.

Hall mobility extracted on InGaAs layers grown on InP follows the expected trend with respect to doping density. When bonded onto 200 mm Si wafers, in an InGaAs-o-I configuration, we observe however a deviation from that behavior. Experiments are ongoing to investigate the reason and increase the statistic. Even if the mobility of the bonded InGaAs layers is not as high as the bulk values (possibly due to defects with the bonded interface), it remains high enough after the DWB

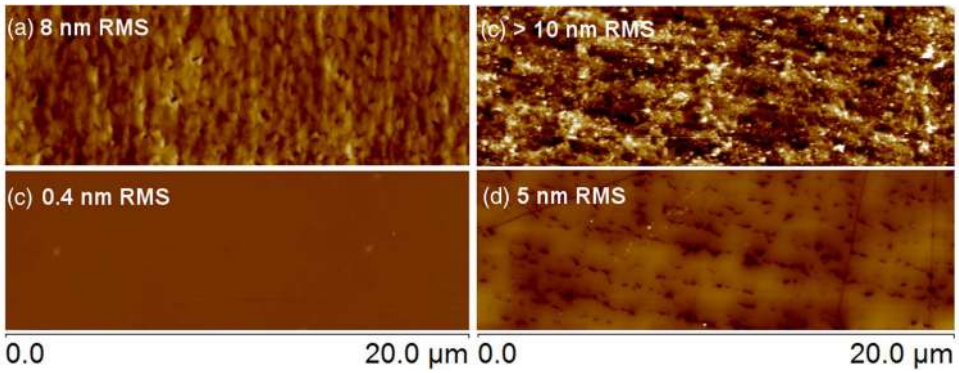

FIG. 3. AFM surface topography and corresponding roughness of the InGaAs layer after growth (a), after III-V CMP (b), after DWB and transfer (c) and after partial CMP of the transferred layer (d). Surface topography area is $20 \times 7\ \mu m^2$.

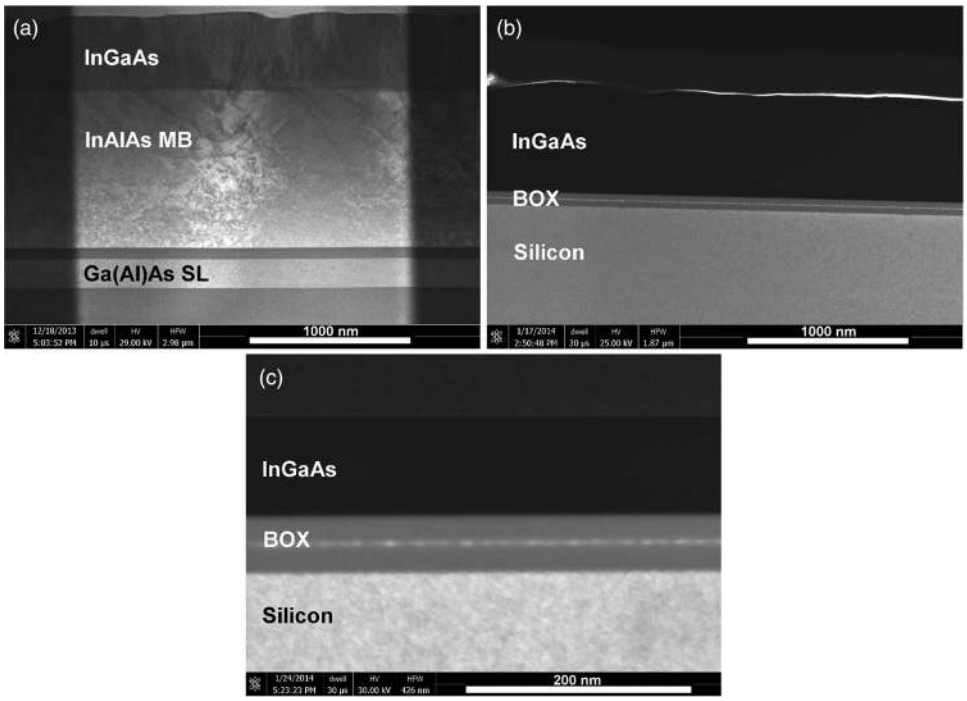

FIG. 4. Cross-sectional STEM micrographs of as-grown III-V layers on silicon (a), InGaAs-o-I with CMP of InGaAs at the bonding interface (b), and InGaAs-o-I after the second CMP step (c).

to process competitive devices. Finally, the InGaAs layers grown on miscut Si donor wafers and bonded behave like those grown on InP and also transferred. Namely, the mobility of the layer grown on the offcut Si wafer remains very high (Fig. 5) with values up to $\sim$6000 cm^2/Vs for a residual doping density $\leq 10^{17}\ cm^{-3}$. This preliminary data points to the fact that the transport characteristics of InGaAs layers grown on silicon are comparable with those of InGaAs grown on lattice matched InP substrates. The current-voltage (I-V) characteristics of our InGaAs-o-I structures were measured on pseudo (Ψ)-MOSFET having etched mesa of variable width and length with patterned tungsten source and drain top electrodes. The electrical contact to the backside gate is made with a Ga-In eutectic. The transfer and output characteristics (Figs. 6(a) and 6(b)) confirm the good structural quality of our devices. The large I_{off} current is due to the rather thick InGaAs layer ($t = 450$ nm) and the difficulty to turn off the channel due to non-optimal electrostatic control. Thinner InGaAs body ($t < 100$ nm) would solve this problem but additional work is still required to achieve good electrical

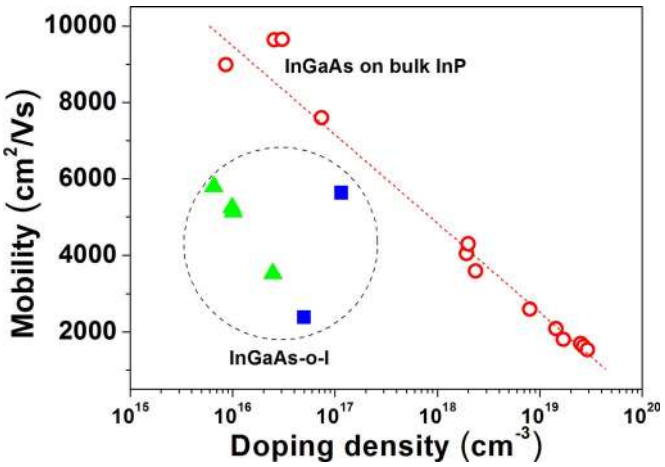

FIG. 5. Hall mobility vs. doping density of 450 nm thick InGaAs-o-I layers grown on InP starting material (triangle) and on 200 mm offcut Si wafers (square). For comparison, reference data of InGaAs layers grown on bulk InP (not InGaAs-o-I substrate) with different doping levels are shown (circle).

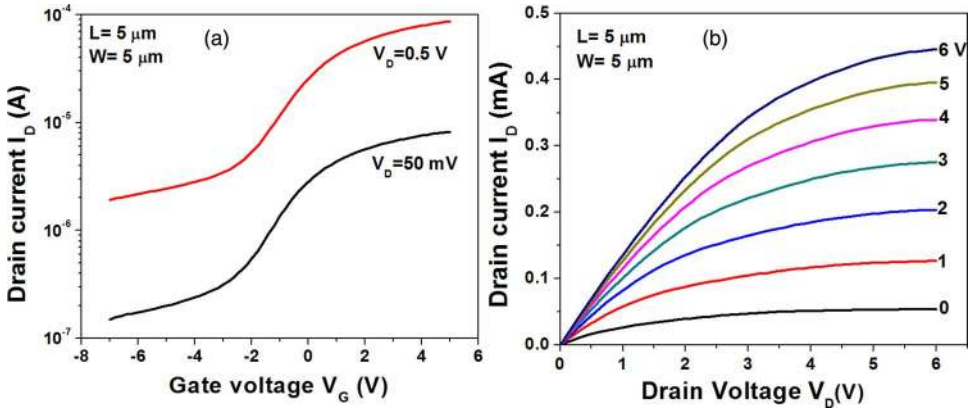

FIG. 6. Transfer (a) and output (b) characteristics of a pseudo-MOSFET based on the InGaAs-o-I substrates (450 nm thick InGaAs).

results. The extraction of the low field mobility μ_0 can be done using the ratio of the drain current I_D over the square root of the transconductance g_m as given by $I_D/(g_m)^{1/2} = (WC_{ox}\mu_0 V_D/L)^{1/2}\,(V_G\text{-}V_T)$,[16] where W and L are the effective channel width and length, C_{ox} is the gate oxide capacitance (here 50 nm Al_2O_3), V_T is the threshold voltage, and V_G is the back side gate voltage. In strong inversion the quantity $I_D/(g_m)^{1/2}$ is linear in gate voltage and μ_0 is derived from the corresponding slope. For the sample of Fig. 6 with L = W = 5 μm, μ_0 = 2380 cm^2/Vs while this value can even increase up 3100 cm^2/Vs for wider width W = 20 μm. These μ_0 values are in fair agreement with the lower Hall mobility found for InGaAs-o-I (Fig. 5).

We demonstrated the successful fabrication of 200 mm InGaAs-o-I substrates where a III-V layer directly grown on Si wafers is transferred using the direct wafer bonding process. Thin InGaAs active layers (90 nm thick) were achieved. High electron mobility in the range of 2000–3000 cm^2/Vs for the 450 nm thick InGaAs-o-I were also measured. Ultra-thin InGaAs layers (<50 nm thick) could be obtained with improved CMP steps of the active layer. This process can easily be implemented to wafers with 300 mm diameter or more, opening the way to very large scale production of such advanced substrates for the future technology nodes.

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