Towards power centric analog design

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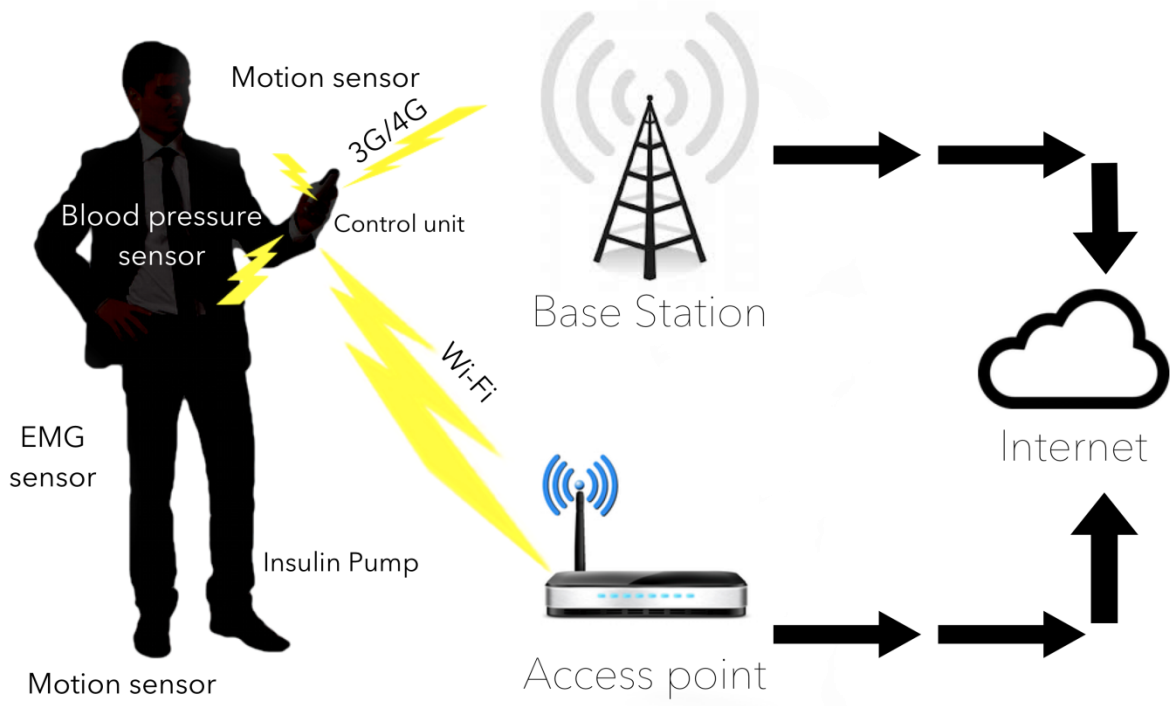

Abstract. Power consumption of analog systems is poorly understood today, in contrast to the very well developed analysis of digital power consumption. We show that there is good opportunity to develop also the analog power understanding to a similar level as the digital. Such an understanding will have a large impact in the design of future electronic systems, where low power consumption will be crucial. Eventually we may reach a power centric analog design methodology.

Introduction.

Power consumption is a central issue today. More and more devices and systems are operated on battery, making the battery lifetime one of the key performance measures. This goes for laptops, mobile phones and many other devices. And this is even more important for smaller systems as body networks, Internet of Things, smart cards, etc., where we strive for battery-less systems which may be active for long time without any form of maintenance [1]. Some power could be made available through energy scavenging, but very small amounts. Also for larger systems power consumption is central. Active cooling is expensive, bulky and noisy. Power itself is an issue in an energy-conscious world, in the same time as we see very large demands for server-farms and supercomputers. So, all electronic design today really needs to make low power consumption top priority. As any electronic system is built from both analog and digital parts, we need to understand the power issues of both analog and digital designs. However, it appears that we do have a very good picture of digital power consumption, but much less so regarding analog.

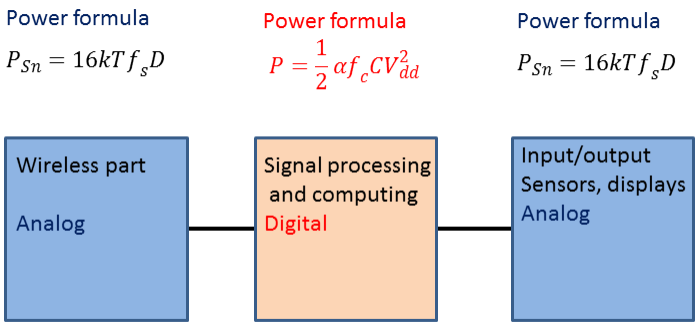

Fig. 1. Any system is built from both analog and digital parts.

For digital systems power-aware design is very well established today. It started already in the beginning of the 1990ies by the work of Chandrakasan [2] and Liu [3]. The key issue was to create a basic understanding of the power consumption in digital systems (based on CMOS technology). The power consumption of a digital system can be described as:

$$P = \frac{1}{2}\alpha f_c C V_{dd}^2 \qquad (1)$$

Where α is the activity (the probability for a logic output to change value during one clock cycle), f_c is the clock frequency, C is the switched capacitance and V_{dd} is the supply voltage. In spite of its simplicity, this formula has proven extremely powerful and did create a whole new research community. An interesting observation is that C is proportional to the number of logical circuits, so $\alpha f_c C$ is in fact proportional to the total amount of computation performed. What can be learned from the formula is for example the importance of low supply voltage for digital systems, which eventually lead to supply voltages of the order of 0.4-0.9V (which limits were already predicted in [3]). Low supply voltage leads to less speed capability, so we have also learned how to trade parallelism (reducing speed demands) for power consumption at a given speed requirement, already noted in [2]. Since the 1990ies we have seen a vast amount of papers, numerous books and yearly conferences dedicated to digital power consumption (see for example [4]).

So, why have we not seen anything like this in the analog world? Even modern textbooks, as for example Razavi's Design of analog CMOS integrated circuits [5] or Sedra/Smith's Microelectronic circuits [6], lack a chapter or a section on analog power consumption. Would it be possible to find a formula corresponding to Eq. (1) for analog systems? Is it realistic to think about power centric analog design?

Of course we have seen some work on low power analog previously, but not in the same systematic way as seen in the digital world. Eric Vittoz pioneered low power techniques already1980 [7] and presented the first analysis of power consumption in analog circuits some 10 years later [8,9]. In 1985 Castello and Gray presented an analysis of the power consumption of switched capacitor circuits [10]. These analyses of power consumption in analog circuits were further developed by Enz and Vittoz[11]. Later, Bult [12] and Annema et al. [13] looked into the effect of scaling on analog power consumption, an analysis which Bult then developed into a more comprehensive analysis of analog power consumption [14]. More recently, Sundström et al., presented a quantitative analysis of the lower bounds of the power consumption of analog-to-digital converters [15]. That work was then generalized by Svensson and Wikner [16], to a large extent based on Bults analysis, to a first attempt to realize the goal of an analog correspondence to eq. (1). Abidi discussed power-conscious design of wireless circuits in [17], and Nilsson [18] later attempted to extend the analog power concept in [16] to such circuits. Homayoun and Razavi [19] recently presented some innovative ideas for power saving in a wireless receiver.

So, why have we not seen anything like the digital power models in the analog world? Even modern textbooks lack a chapter or a section on analog power consumption. Would it be possible to find a master formula corresponding to the digital one for analog systems? Is it realistic to think about power centric analog design?

Elements of a theory of analog power consumption.

A good starting point in the discussion of analog power consumption is the ideal sampler (the sample-and-hold circuit) [8, 16]. An ideal sampler will follow an analog signal and then sample and hold its value for a period of time. The main performance measures are sampling rate (number of sampling instances per unit time) and dynamic range (the signal-to-noise ratio at maximum input signal). Other performance measures are accuracy and signal bandwidth. See figure 2.

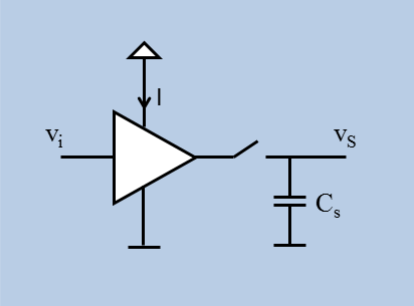

Fig. 2. Sample and hold circuit.

When the switch is conducting, the noise voltage at the output can be estimated to ("classical kT/C-noise", assuming the only noise source being the amplifier output resistance and the switch series resistance):

$$v_{nS}^2 = \frac{kT}{C_{Sn}} \tag{2}$$

where k is Boltzmann's constant and T the absolute temperature. Assuming a full scale voltage (peak-to-peak voltage) at the input equal to V_{FS} will allow a maximum rms sine voltage of

$$v_s = \frac{V_{FS}}{2\sqrt{2}} \tag{3}$$

This gives a dynamic range of the circuit of D:

$$D = \frac{v_s^2}{v_{nS}^2} = \frac{V_{FS}^2 C_{Sn}}{8kT} \tag{4}$$

In order to meet a certain dynamic range requirement, we thus need a capacitor larger or equal to C_{Sn}

$$C_{Sn} = \frac{8kTD}{V_{FS}^2} \tag{5}$$

In order to charge this capacitor in time T to the full scale voltage V_{FS} we need a charging current of $I=C_{Sn}V_{FS}/T$. With a sampling frequency of f_s, we may assume that we use half a sampling period for capacitor charging, $T = 1/2f_s$. Finally, assuming that we have an ideal amplifier, with maximum output current equal to the supply current and maximum output voltage equal to supply voltage, we may calculate the power consumption of the sampler:

$$P_{Sn} = IV_{FS} = 16kTf_sD \tag{6}$$

The consequence is that analog power consumption does not depend on the supply voltage. This means that most attempts to save analog power by reducing the supply voltage will fail. Also, striving for later technology nodes with very small geometries will not help analog power consumption.

This formula gives a good insight in analog power consumption, and may be seen as the analog version of eq. (1). We note that it is proportional to the dynamic range of the signal and the sampling rate (or signal bandwidth). The fact that it is proportional to kT indicates that it is bounded by thermal noise. Furthermore, we note that this expression is independent of both technology and supply voltage, in contrast to the digital case (eq. (1)), as also noted in [17].

So, what happens at very low dynamic ranges? Then the capacitance may become very small. What can happen is that C_{Sn} in eq. (5) becomes less than the minimum capacitance which can be implemented in the actual technology used. We thus need to replace C_{Sn} in the above expressions with C_{min}, the smallest capacitance which can be implemented. So, for low dynamic ranges the power consumption will become dependent on both technology and supply voltage through C_{min} and V_{FS}:

$$P_{ST} = 2 f_s C_{min} V_{FS}^2 \qquad (7)$$

We note that this expression is very similar to eq. (1), which can be interpreted as that the digital case is limited by C_{min} because its dynamic range requirement is very low. See also figure 3. We also included the digital case in the figure, in order to demonstrate the different behavior of the two. The actual data is taken from [16] and corresponds to a simple filter designed in analog or digital technique.

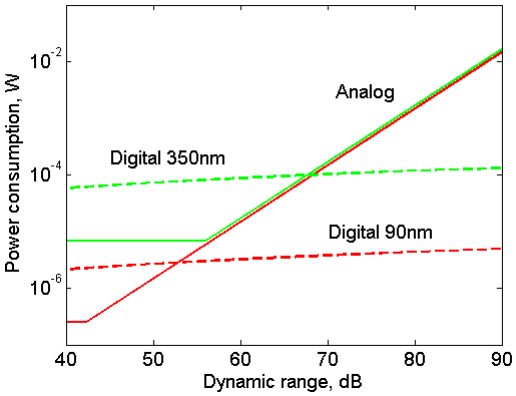

Fig. 3. Power versus dynamic range, demonstrating the difference between analog and digital and the effect of technology [16].

In most practical cases the dynamic range requirements are large enough to make eq. (6) valid. The consequence is that analog power consumption does not depend on the supply voltage. This means that most attempts to save analog power by reducing the supply voltage will fail. Also, striving for later technology nodes with very small geometries will not help analog power consumption. Instead, what we can learn from eq. (6) is that power can be saved by limiting the dynamic range to the actual needs, and by striving for circuits utilizing the full supply voltage range.

Transistors and amplification.

Let us take a look on a simple transistor circuit, figure 4. As in the above example, we start to look at the thermal noise.

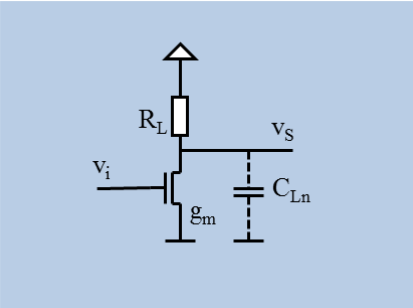

Fig. 4. Simple transistor amplifier.

For an MOS transistor we normally express the drain noise current in terms of transistor transconductance, g_m as:

$$i_{dn}^2 = 4kT\gamma g_m B_n \quad (8)$$

where γ is a noise factor and B_n is the system noise bandwidth [16]. In the following we neglect noise contributions from other sources than the transistor drain current (as the drain current noise normally dominates). The output noise voltage, $v_{dn} = Ri_{dn}$. Again, assuming that the output full scale voltage is V_{FS}, corresponding to a maximum output as eq. (3), we may express the dynamic range, D, as:

$$D = \frac{v_S^2}{v_{dn}^2} = \frac{V_{FS}^2 g_m}{32kT\gamma A_v^2 B_n} \quad (9)$$

where we introduced the DC gain of this stage, $A_v = g_m R$. From eq. (9) we may now calculate the g_m needed to reach the dynamic range, D:

$$g_m = \frac{32kT\gamma A_v^2 B_n}{V_{FS}^2} D \quad (10)$$

To achieve a certain transconductance, g_m, we need to supply the transistor with a bias current $I_D = g_m V_{eff}$, where we have introduced the parameter V_{eff} (of the order of 25 to 500 mV, see below). Using I_D together with the supply voltage, again assumed to be V_{FS}, we can calculate the power consumption as:

$$P_{Tn} = 32kT\gamma A_v^2 B_n \frac{V_{eff}}{V_{FS}} D \quad (11)$$

We may note large similarities to eq. (6), particularly considering the close relation between sampling frequency, f_s, and bandwidth, B_n. Noting that $f_s \approx 2B_n$ (for Nyquist sampling) makes $32B_n$ equal to $16f_s$, and eq. (11) differ from eq. (6) only through A_v^2 and V_{eff}/V_{FS}. The first of these factors indicates that voltage gain comes at a power cost and the second factor indicates that part of this cost is mitigated if we can choose a small value of V_{eff}.

Just as eq. (6), also eq. (11) is independent of the technology used. However, again this is not entirely true. In order to understand this we need to include the capacitive load of the transistor, C_{Ln}, assumed parallel to R. C_{Ln} will control the noise bandwidth through $B_n = 1/4RC_{Ln}$ (noise bandwidth of a single pole low-pass filter). Inserting this expression into eq. (9) and solving for C_{Ln} gives:

$$C_{Ln} = \frac{8kT\gamma A_v}{V_{FS}^2} D \quad (12)$$

which is similar to eq. (5). So, if C_{Ln} is less than the smallest capacitance that can be implemented, we need to replace C_{Ln} with C_{min} as before. To keep the same bandwidth and gain we need $g_m=4A_vC_{min}B_n$ which leads to a power consumption of:

$$P_{TT} = 4B_nC_{min}V_{eff}V_{FS}A_v \quad (13)$$

which is similar to eq. (7). So for low dynamic range also the transistor circuit has a power consumption which depends on technology (C_{min}) and supply voltage (V_{FS}).

Let us now discuss the V_{eff} parameter used above. V_{eff}, is defined as [15]:

$$V_{eff} = \frac{I_D}{g_m} \quad (14)$$

For a classical long channel MOST in strong inversion $V_{eff}=(V_G-V_T)/2$, where V_G and V_T are the gate voltage and threshold voltage respectively. For weak inversion, that is for $V_G<V_T$, $V_{eff}=mkT/q$, with m slightly larger than 1. For a modern submicron MOST V_{eff} tends to fall above these values, see figure 7 in [15]. We could also note that bipolar transistors exhibits $V_{eff}=kT/q$.

Returning to the MOS transistor and the formula above, we can conclude that small V_{eff} is preferred to save power. But there are some constraints to how we can choose V_{eff}. First transistor speed depends on gate bias, so a low V_{eff} corresponding to a low V_G leads to reduced speed. Transistor speed can be characterized by f_T, the frequency at which the transistor current gain has fallen to one. In figure 7 in [15] we note quite a difference between two process nodes. In a 350nm node we need to keep quite a large V_{eff} to keep transistor speed, whereas in a 90nm node we do not gain much speed above V_G=100mV corresponding to V_{eff}=100mV. So, deep submicron technologies easily combine low power and high speed.

Second, high input voltage amplitude is not compatible with very low V_{eff}. If the input voltage amplitude is large compared to V_{eff}, then we can expect a highly nonlinear response of the transistor. For example, for an input voltage swing of $V_{FSin}=V_{eff}$ (where V_{FSin} is the peak-to-peak gate voltage), the transistor current will vary roughly between $I_{DC}/2$ and $3I_{DC}/2$ (I_{DC} is the DC drain bias). Thus choosing V_{eff} larger or equal to the peak-to-peak gate voltage is a reasonable first attempt to keep the circuit linear. Bult derived a more strict relationship between V_{FSin}, V_{eff} and the second order distortion, HD_2, $HD_2=V_{FSin}/2V_{eff}$, valid for MOSTs in strong inversion [20].

Including more circuit specifications.

In the above description only dynamic range given by thermal noise and speed is considered. We showed initially that the dynamic range requirement leads to a requirement on the minimum load capacitance. We then showed how this capacitance, in combination with a speed requirement leads to a lower bound of power consumption.

Bult [14] used the same scheme as this one, but extended it to include more circuit specifications. He showed that not only thermal noise, but also 1/f noise and circuit matching will put demands on the capacitance. So in practice several specifications will control the load capacitance. Then he showed that not only bandwidth or sampling time will affect the power consumption at a given load capacitance, but also slew rate, distortion and settling.

Still, however, the basic scheme above is always valid. Power consumption can be understood in terms of a minimum capacitance requirement, and the current required driving that capacitance. The capacitance is given by technology, thermal noise, 1/f –noise, and matching (in terms of offset or gain matching) [14, 15, 16]. And the current is controlled by this minimum capacitance, combined with the

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requirements on speed (in terms of bandwidth, sampling rate or slew rate), settling accuracy, and distortion (in terms of second order or third order distortion with or without feedback) [14, 15].

Radio frequency circuits.

The above discussion mainly treats low frequency or wide-band circuits. The large difference compared to radio frequency circuits is that radio frequency circuits normally utilize inductors. Therefore inductor performance will be an important additional factor for circuit performance and power consumption.

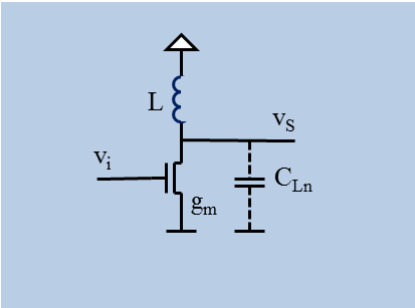

Fig. 5. Simple radio frequency amplifier.

Let us look at a simple circuit example. In figure 5 we show a simple radio frequency amplifier, utilizing an inductive load. In this case the noise bandwidth is given by

$$B_n = \frac{\pi}{2} f_{3dB} = \frac{\pi}{2}\frac{f_0}{Q} = \frac{\pi}{2}\frac{\omega_0}{R}\sqrt{\frac{L}{C}} \qquad (15)$$

where we have defined the 3dB bandwidth f_{3dB}, the center frequency f_0 and corresponding angular frequency ω_0, and the load Q-value Q. Also in this case the voltage gain is g_mR (in the center of the passband $R=\omega_0LQ$), so eqs. (8) to (11) are still valid. The problem is that the availability of inductance properties is limited, which limits our choice of load capacitance and resistance. Typical on-chip inductances are limited to about 10nH, with Q-values of about 5 [18]. At a typical radio frequency of 2.4GHz (the most common WiFi band) this means that C cannot be less than 440fF for resonance with 10nH, and R cannot be higher than 754ohm (equivalent parallel resistance of a lossy inductance is ω_0LQ). 440fF is far larger than C_{min}, leading to considerable larger power consumption than a wide-band circuit with the same bandwidth and gain (eq. (13) with C_{min} replaced by 440fF). In addition, we may not be able to choose the bandwidth, as it cannot be made smaller than f_0/Q, equal to 480MHz in our example. As a result, it may be so that we are better off from a power perspective by not utilizing an inductor at all! Just designing a wide-band amplifier with a bandwidth of f_0 may lead to lower power consumption as demonstrated in [18].

In other cases passive components may save power in radio frequency circuits. One example is a low noise amplifier (LNA) used at the input of a radio receiver. In this case we are interested in the noise figure of the LNA. Following [16] we use an OTA with feedback as prototype LNA, see figure 6a. The input impedance of this circuit is 1/G, where G is the OTA transconductance, and is set to the source impedance R_s. The noise is dominated by the noise current of the input transistor with transconductance g_m and can be modelled as an input noise voltage, v_{gn}:

$$v_{gn}^2 = \frac{i_{dn}^2}{g_m^2} = \frac{4kT\gamma B_n}{g_m} \quad (16)$$

And the noise figure can be expressed as

$$F = 1 + \frac{v_{gn}^2}{v_{sn}^2} = 1 + \frac{\gamma}{g_m R_S} \quad (17)$$

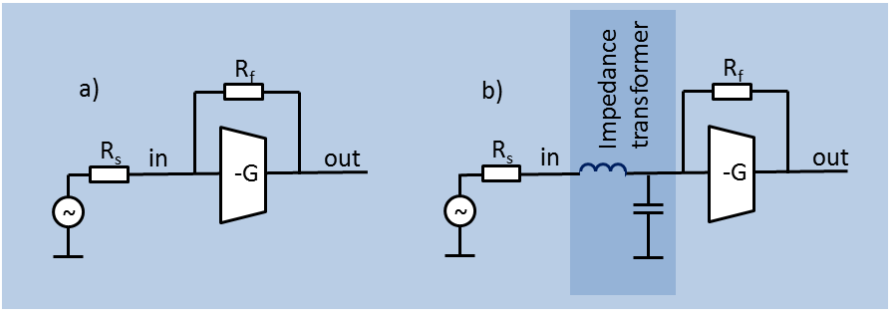

Fig. 6. a) prototype LNA, and b) prototype LNA with impedance transformer.

where v_{sn} is the noise voltage of the source resistance R_s, $v_{sn}^2=4kTR_sB_n$. So, a certain requirement on noise figure becomes a requirement on g_m, which then leads to a certain power consumption through $P=g_mV_{eff}V_{dd}$ as above.

How can we save power in this case? We note that g_mR_s appear in eq. (17), so if we can increase R_s we may decrease g_m for the same noise figure. And R_s can be increased by a passive impedance transformer at the LNA input [17, 18, 19]. In [18] it was shown that an impedance transformer based on an external inductance (figure 6b) will have an impedance transformation ratio equal to the Q-value of the external inductance, which may be about 35 at 2.4GHz. An external inductance may therefore lead to a power reduction of 35x at a given noise figure. More drastic solution is to replace the LNA by a passive transformer, directly followed by a passive mixer [19]. An extended discussion of power-conscious design of radio frequency circuits can be found in [17].

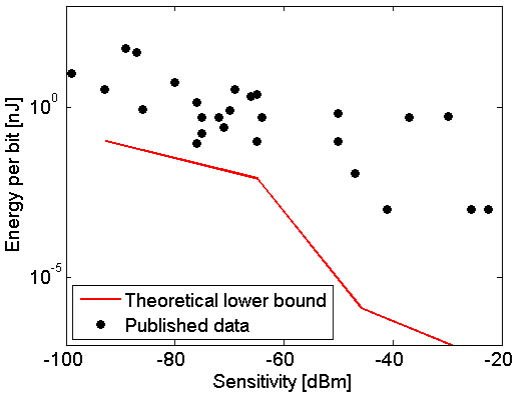

Fig. 7. Energy per bit versus sensitivity for wireless receivers. The red line is the estimated lower power bound. Dots are published data on low power receivers. The red line ends at the point where a room temperature antenna noise at 500kHz bandwidth dominates.

In order to better grasp the consequences of the above results, lower bounds to the power consumption of wireless receivers was estimated in [18]. As discussed above the number of parameters is very large, so such estimation needs to be limited in scope. We chose to estimate the energy per bit received data versus receiver sensitivity for low power receivers at 2.5GHz carrier frequency with relatively low bandwidth (500kHz) (typically so called wake-up receivers). The lower bounds from [18] are summarized in figure 7 (red line), together with published data of low power receivers (for references

As a result, it may be so that we are better off from a power perspective by not utilizing an inductor at all. In no case a superheterodyne architecture is preferred from a power perspective.

see [18]). We note three sections of the bound curve. For very low sensitivities (on the right) the power bound is given by the baseband amplifier. For the mid part the power bound is related to the detector (here an active nonlinear element), utilizing an input impedance transformer as discussed above. In these two sections the most efficient receiver utilizes just an envelope detector and a baseband amplifier. For the leftmost sector of the red curve a low noise amplifier is added to the architecture. In no case a superheterodyne architecture is preferred from a power perspective. Inductors are beneficiary only in the input impedance transformer.

Analog-to-digital converters.

Analog-to Digital converters (ADCs) are good examples of where the above power approaches can be applied. For an ADC it is reasonable to use the number of bits, n, as a measure of dynamic range. This is accomplished by equalizing thermal noise and quantization noise [15], leading to a sampling power (corresponding to eq. (6)) of

$$P_{ST} = 24kTf_s 2^{2n} \qquad (18)$$

By applying the principles above to flash and pipelined ADCs [15] and successive approximation ADCs [21] we were able to estimate lower bounds to the ADC power consumption. Just as in the above sampling case, power will be proportional to the sampling frequency, f_s. It will also depend strongly on the dynamic range, or the number of bits, for high dynamic range, and less so for low dynamic range. In figure 8 we show the power consumption divided by the sampling frequency, P/f_s (equivalent to energy per sample), versus the number of bits, n, for these three classes of ADCs.

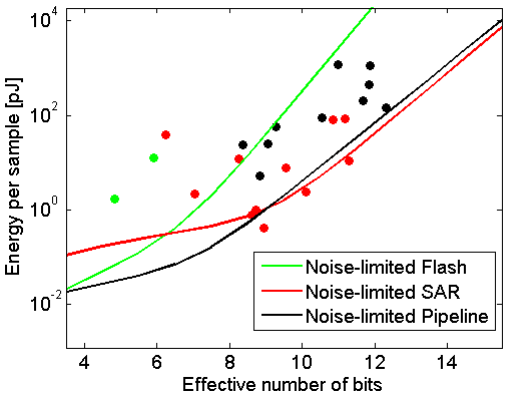

Fig. 8. Energy per sample versus effective number of bits for three classes of ADCs, flash, SAR and Pipeline. Lines are theoretical bounds (from [15] and [21]), dots are data from ISSCC and VLSI Symposium 2013-2014 (from [22]).

We note the typical behaviour versus dynamic range (in this case effective number of bits), relatively flat for low dynamic range and steep for large dynamic range. We also note that flash ADCs use much higher power for bitnumbers above about 4b, and that SAR and pipeline are comparable above 8b (Below 8b SAR power is dominated by the digital operations). Further we see that some experimental converters approach the bounds. This is particularly obvious regarding SAR converters, where some published converters even appear to have power consumption below the limits, indicating that the theoretical bounds could be improved.

The parameters used in calculating the bounds in figure 8 corresponds to a 90nm technology [15, 21], whereas the experimental data refers to 28nm to 180nm technologies. The experimental data covers sampling frequencies between 4kHz and 5GHz, and are taken from [22].

How to utilize this knowledge?

So, if we eventually understand the relation between power consumption and circuit performance, how to utilize this knowledge? One way to utilize it is to use the understanding to estimate the lower bounds of power consumption of a particular class of circuits. Comparing these lower bounds to actual power consumption, we may discover areas with large prospect for improvements, and therefore promising areas of research or product development. For example, figure 7 suggests that improvements can be expected for low sensitivity wireless receivers.

Another way to utilize this knowledge is by starting a new circuit design project by estimating the power consumption of the circuit, based on its specifications. By using this estimate as a design target, there will be a good chance to arrive to a power-optimal solution. An example of this thinking is found in [23]. Similarly, if specifications of a product are changed (new technology available, changed requirements, etc.) it is possible to estimate the power consumption of an upgraded design and thus to judge if an upgrade is worth the effort.

A third application is to compare different solutions to a given problem from a power consumption perspective, including comparison between digital and analog solutions, or comparison between different architectures.

Future work.

Analog circuits are far more diverse that digital circuits. Therefore it is very difficult to formulate a general description of the power consumption of analog circuits. Still, we believe that the descriptions above, together with the ideas formulated in [14], could be the first elements of such a general description, although many aspects of analog circuits are left to be investigated.

Examples of important topics to be investigated are linearity, matching, and RF passives. Regarding linearity we need to relate power consumption to various linearity requirements, as HD2/HD3, THD, IP2/IP3, SFDR etc. We also need to understand the power cost for linearity improvement through feedback or other circuit tricks. Matching requirements are sometimes quite expensive in power, particularly regarding offset [14]. Therefore we need compensating techniques, as offset compensation, offset and gain calibration, etc., and we need to understand the power cost for such techniques. Contemporary AD-converters often use various digital calibration or error correction techniques to mitigate matching errors. In these cases also the power consumption of the digital functions must be considered. As discussed above RF passives may have a large impact on power, but the use of passives is not governed by power alone. Other aspects, as radio receiver selectivity, or suppression of unwanted signals, are also essential. Again, all requirements must be included when optimizing for power, which calls for a very good understanding of the whole problem. So, there is a lot to do!

Conclusion.

It is possible to develop a generic theory of power consumption in analog circuits, similarly to what is available for digital circuits. We demonstrated the usefulness for such a theory in terms of the development and utilization of lower bounds to power consumption or in terms of comparisons between different system architectures. Still, what we have is just the first steps towards a complete

theory, indicating a fruitful future research area. Based on these and future results we may approach a power centric analog design methodology, similarly to what we have in the digital domain.

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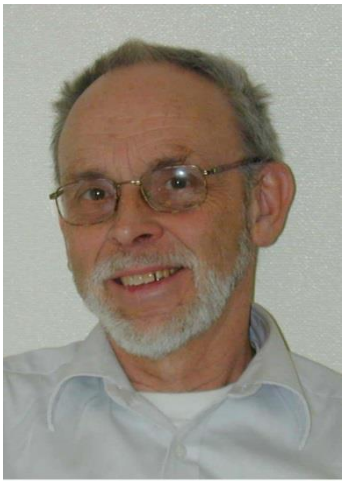

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