Trans-Z-Source Inverters

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***Abstract*—This paper extends the impedance-source (Z-source) inverters concept to the transformer-based Z-source (trans-Z-source) inverters. The original Z-source inverter (ZSI) employs an impedance network of two inductors and two capacitors connected in a special arrangement to interface the dc source and the inverter bridge. It has buck and boost function that cannot be achieved by traditional voltage-source inverters and current-source inverters. In the proposed four trans-Z-source inverters, all the impedance networks consist of a transformer and one capacitor. While maintaining the main features of the previously presented Z-source network, the new networks exhibit some unique advantages, such as the increased voltage gain and reduced voltage stress in the voltage-fed trans-ZSIs and the expanded motoring operation range in the current-fed trans-ZSIs, when the turns ratio of the transformer windings is over 1. Simulation and experimental results of the voltage-fed and the current-fed trans-ZSIs are provided to verify the analysis.**

***Index Terms*—Current-source inverter, dc–ac conversion, voltage-source inverter, Z-source inverter.**

I. Introduction

TRADITIONAL voltage-source inverters (VSIs) and current-source inverters (CSIs) have similar limitations and problems. For VSIs: 1) the obtainable ac output voltage cannot exceed the dc source voltage. So a dc–dc boost converter is needed in the applications, for instance, with limited available dc voltage or with the demand of higher output voltage. 2) Dead time is required to prevent the shoot-through of the upper and lower switching devices of each phase leg. However, it induces waveform distortion. For CSIs: 1) their output voltage cannot be lower than the dc input voltage; and. 2) overlap time between phase legs is required to avoid the open circuit of all the upper switching devices or all the lower devices. The Z-source inverter (ZSI) [1], as well as the derived quasi-Z-source inverters (qZSI) [2], [3], can overcome the aforementioned problems. They advantageously utilize the shoot-through of the inverter bridge to boost voltage in the VSIs (or open circuit in the CSIs to buck voltage). Thus, buck–boost functionality is achieved with a single-stage power conversion. They also increase the immunity of the inverters to the EMI noise [4], which may cause misgating and shoot-through (or open circuit) to destroy the conventional VSIs and CSIs.

The voltage-fed Z-source inverter can have theoretically infinite voltage boost gain. However, the higher the voltage boost gain, the smaller the modulation index has to be used. In applications such as grid-connected photovoltaic (PV) generation and fuel cell power conversion, a low-voltage dc source has to be boosted to a desirable ac output voltage. A small modulation index results in a high voltage stress imposed on the inverter bridge. Several pulse width modulation (PWM) methods [5], [6] have been developed with the attempt of obtaining as much voltage gain as possible and thus limiting the voltage stress across the switching devices. The maximum boost control [5] achieves the maximum voltage gain through turning all the zero states in the traditional VSIs to shoot-through zero states. Nevertheless, it brings in low-frequency ripples associated with the ac-side fundamental frequency. So, the constant boost control [6] has been proposed to eliminate those ripples and thus reduce the L and C requirement in the Z-source network, with slightly less voltage gain, compared to the maximum boost control. These PWM methods still have limits to further extend the voltage gain without sacrificing the device cost. Recently, some modified impedance source networks were proposed in [7]–[10] for the sake of increasing the output voltage gain. Among them, a T-source inverter [7] has the possibility of increasing voltage gain with the minimum component count. As will be discussed in the next section, it can be grouped into a general class of transformer-based Z-source inverters (trans-ZSIs) presented in this paper, which employ two transformer windings in the impedance network.

The voltage-fed Z-source/quasi-Z-source inverters cannot have bidirectional operation unless replacing the diode with a bidirectional conducting, unidirectional blocking switch [11]. Neither can the traditional current-fed inverters [12]–[14] do unless they are fed by a phase-controlled rectifier in front that can change the dc-link voltage polarity. Interestingly, the current-fed Z-source/quasi-Z-source inverters [2], [15], [16] can have voltage buck–boost and bidirectional power flow only with a diode in the impedance network. With the newly developed reverse-blocking IGBTs [17], this single-stage power converter becomes a promising topology. Yet, their dc–ac voltage gain cannot exceed 2 in the boost mode operation. In other words, the dc input voltage cannot be lower than half of the peak output line-to-line voltage. Hence, this paper further proposes two current-fed trans-Z-source inverters that are capable of reaching wider voltage boost range and bidirectional power flow with a single diode. As a result, a wider output voltage range can be obtained, which is essential to some applications such as HEV/EV motor drives.

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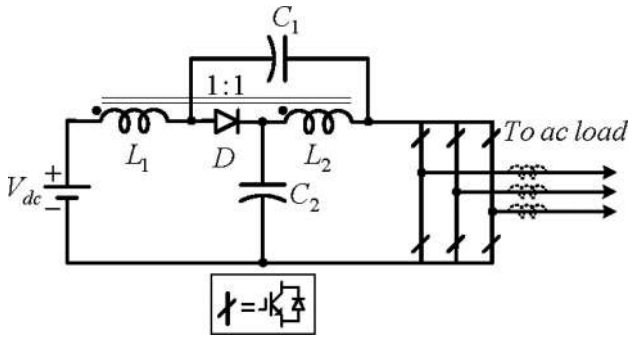


Fig. 1. Voltage-fed quasi-Z-source inverter with coupled inductors.

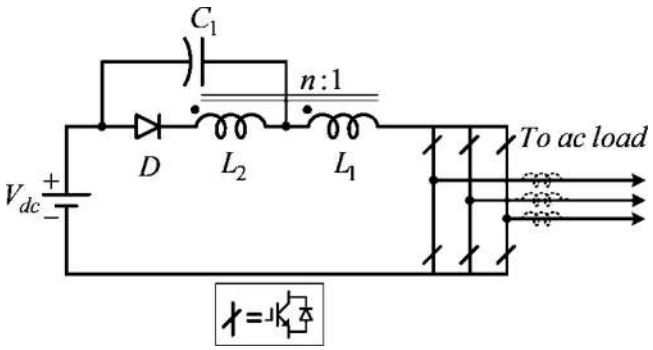


Fig. 2. Voltage-fed trans-quasi-Z-source inverter.

The trans-Z-source inverters can be derived from the voltage-/current-fed quasi-Z-source inverters or the voltage-/current-fed Z-source inverters. The trans-Z-source inverters inherit their unique features, and they can be controlled using the PWM methods applicable to the Z-source inverters. This paper will begin with the derivation of two voltage-fed trans-Z-source inverters from one of the quasi-Z-source inverters. Next, the same idea is extended to the development of two current-fed trans-Z-source inverters. Then, the followed comparative analysis, simulation, and experimental results will demonstrate their new properties different from the Z-source/quasi-Z-source inverters.

II. Voltage-Fed Trans-Z-Source Inverters

In the voltage-fed quasi-Z-source inverter with continuous input current, two dc inductors can be separated or coupled. When the two inductors are coupled as shown in Fig. 1, the voltage across the inductor L_1 is reflected to the inductor L_2 through magnetic coupling. Then, one of the two capacitors, for instance C_2, can be removed from the circuit. The rearrangement of the circuit yields the structure as shown in Fig. 2. Furthermore, the voltage across L_2 can be made proportional to the voltage across L_1 by changing the turns ratio n_2/n_1. As the voltage constraint associated with one of the capacitors is released, the two windings, to some extent, behave more like a flyback transformer rather than the original coupled inductors [18], except that the currents flow simultaneously through both windings in some of the operation states. Therefore, it is named as the voltage-fed trans-quasi-Z-source inverter (trans-qZSI).

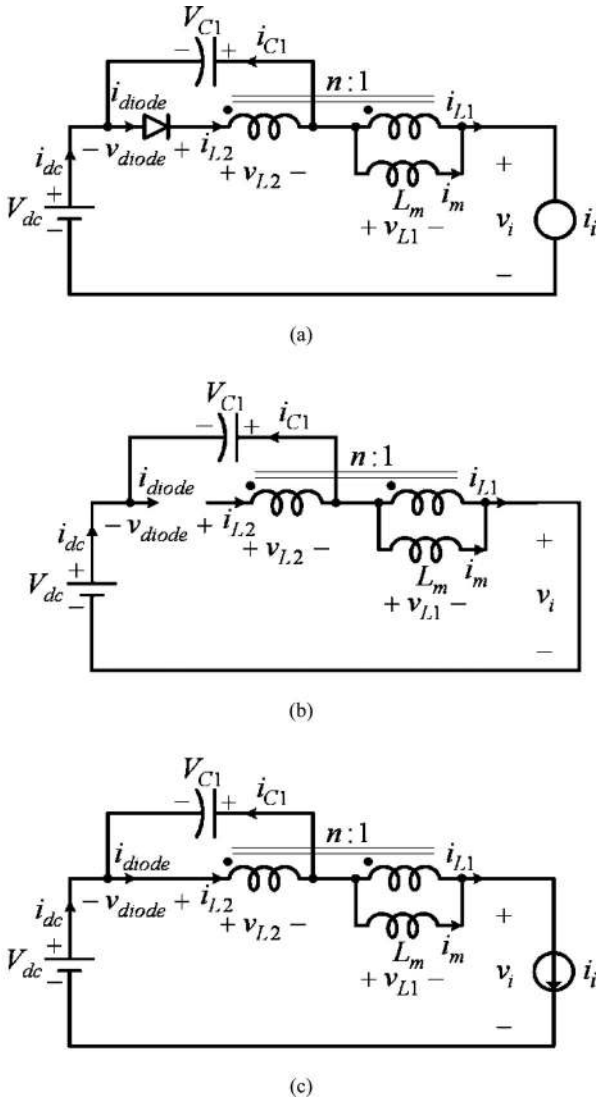


Fig. 3. Equivalent circuits of the voltage-fed trans-qZSI viewed from the dc link. (a) With the transformer equivalent circuit. (b) Shoot-through zero states. (c) Non-shoot-through states.

Like the Z-source inverter, the trans-quasi-Z-source inverter has an extra shoot-through zero state besides the six active states and two traditional zero states. The shoot-through zero state can be realized by short-circuiting both the upper and lower switching devices of any one phase leg, any two phase legs, or all three phase legs. The shoot-through zero state contributes to the unique buck–boost feature of the inverter. Otherwise, when the dc voltage is sufficient to produce the desirable ac output voltage, a traditional PWM without shoot-through zero state is used. For analyzing the characteristics of the trans-Z-source inverters, this paper will focus on the two general continuous current modes as in the Z-source inverter: the shoot-through zero state and the non-shoot-through states [1], [19]. By replacing the two windings with an ideal transformer and a mutual inductance L_m (a model used in [20]), the overall equivalent circuit viewed from the inverter dc side can be obtained as shown in Fig. 3(a).

In the shoot-through zero state, the inverter is equivalent to a short circuit as shown in Fig. 3(b). Given that the inverter is in the shoot-through zero state for an interval of $D_{\rm sh}T$ during a switching cycle T, the voltages across L_1 and L_2 are

$$v_{L1} = V_{\rm dc} + V_{C1} \tag{1}$$

$$v_{L2} = \frac{n_2}{n_1} v_{L1}. \tag{2}$$

Thus, the diode is reversed biased. Note that the symbol $D_{\rm sh}$ is used here for the shoot-through duty ratio in voltage-fed Z-source inverters.

In any of the non-shoot-through states for an interval of $(1 - D_{\rm sh})T$, the inverter bridge can be modeled as an equivalent current source as shown in Fig. 3(c). The non-shoot-through states include the six active states and two traditional zero states. For the traditional zero states, the current source has a zero value (i.e., an open circuit). During one of the non-shoot-through states, one can get

$$v_{L2} = -V_{C1} \tag{3}$$

$$v_{L1} = \frac{n_1}{n_2} v_{L2} = -\frac{n_1}{n_2} V_{C1}. \tag{4}$$

The average voltage of both inductors should be zero over one switching period in the steady state. Thus, from (1) to (4), we have

$$\langle v_{L1} \rangle = \frac{(V_{\rm dc} + V_{C1}) D_{\rm sh} T + (-\frac{n_1}{n_2} V_{C1})(1 - D_{\rm sh}) T}{T} = 0. \tag{5}$$

From the previous equation, the capacitor voltage can be calculated as

$$V_{C1} = \frac{n \cdot D_{\rm sh}}{1 - (1 + n) D_{\rm sh}} V_{\rm dc} \tag{6}$$

where $n = n_2/n_1 \geq 1$.

From (4) to (6), the dc-link voltage across the bridge in the non-shoot-through states can be boosted to

$$\hat{v}_i = \frac{1}{1 - (1 + n) D_{\rm sh}} V_{\rm dc} = B V_{\rm dc} \tag{7}$$

where the boost factor is

$$B = \frac{1}{1 - (1 + n) D_{\rm sh}}. \tag{8}$$

The peak value of the phase voltage from the inverter output is

$$\hat{V}_{\rm ph} = M \cdot \hat{V}_i / 2 = M \cdot B \cdot V_{\rm dc} / 2 \tag{9}$$

where M is the modulation index.

When the constant boost control [6] is used, the voltage gain MB as defined in [5] is

$$G = {\rm MB} = \frac{M}{1 - (1 + n)(1 - \frac{\sqrt{3}}{2} M)}. \tag{10}$$

It can be seen that if the turns ratio is 1, the inverter dc-link voltage boost gain is the same with that of the original Z-source/quasi-Z-source inverters, but one capacitor is saved in the new trans-Z-source network. If the turns ratio is over 1, the inverter dc-link voltage boost gain can be higher given the same modulation index M. In other words, it needs a smaller shoot-through duty ratio $D_{\rm sh}$ (accordingly, a larger modulation index M) to produce the same ac output voltage than the Z-source/quasi-Z-source inverters do. The voltage gain MB versus the modulation index for the voltage-fed trans-quasi-Z-source inverter (with a turns ratio $n = 2$) is compared in Fig. 4 with that for the Z-source/quasi-Z-source inverters, using the constant boost control.

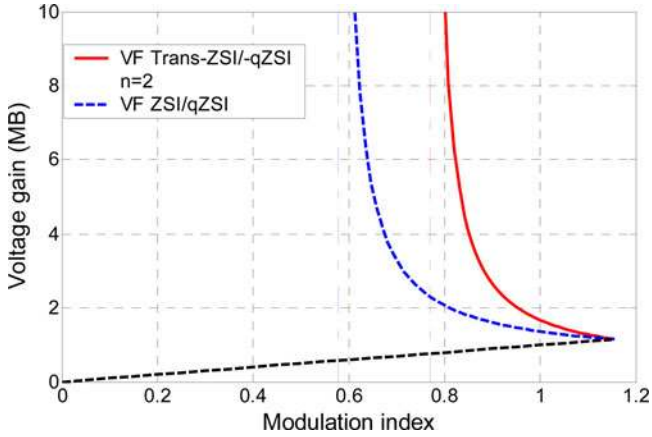


Fig. 4. Voltage gain MB versus modulation index of the voltage-fed trans-ZSI/-qZSI ($n = 2$) and ZSI/qZSI.

The voltage stress V_s across the switching devices can be assessed by comparing its peak dc-link voltage against the minimum dc voltage $GV_{\rm dc}$ [6] needed for the traditional VSI to produce the same ac output voltage at $M = 1$. The ratio represents extra cost that the voltage-fed trans-quasi-Z-source inverter and Z-source/quasi-Z-source inverters have to pay for the voltage boost in association with the higher voltage stress. The ratio of the voltage stress to the equivalent dc voltage for the trans-quasi-Z-source inverter is

$$\frac{V_s}{GV_{\rm dc}} = \frac{BV_{\rm dc}}{GV_{\rm dc}} = \frac{\sqrt{3}}{2}\left(1 + \frac{1}{n}\right) - \frac{1}{n \cdot G}. \tag{11}$$

When $n = 1$, it is the same with the relative voltage stress in the Z-source inverter. When $n > 1$, as can be seen in Fig. 5, the voltage-fed trans-Z-source inverter has less voltage stress across the inverter bridge for the same dc–ac output voltage gain. Hence, this circuit is beneficial to applications, in which a high voltage gain is required.

Similarly, another trans-Z-source inverter can be reconfigured as shown in Fig. 6, if C_1 is removed in Fig. 1 instead of C_2. This trans-Z-source inverter is the same as the T-source inverter proposed in [7]. It is obvious that it essentially has the same operation principle, voltage gain, and voltage stress as the previously developed voltage-fed trans-quasi-Z-source inverter, except for different capacitor voltage stress and different input current drawn from the dc source. Therefore, Figs. 1, 2, and 6 can be classified as a class of voltage-fed trans-Z-source inverters. In Fig. 6, the capacitor voltage is

$$V_{C1} = \frac{1 - D_{\rm sh}}{1 - (1 + n) D_{\rm sh}} V_{\rm dc}. \tag{12}$$

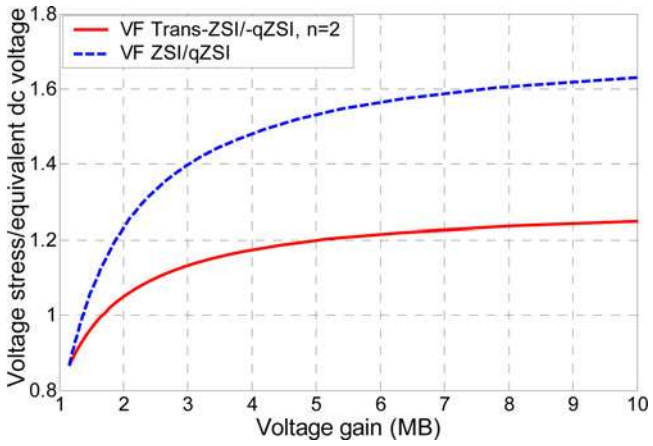


Fig. 5. Active switch voltage stress of voltage-fed trans-ZSI/-qZSI ($n = 2$) and ZSI/qZSI.

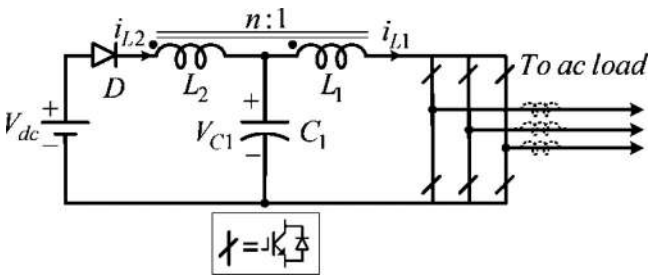


Fig. 6. Voltage-fed trans-Z-source inverter.

When the turns ratio n of the trans-Z-source inverter in Fig. 6 equals 1, (12) becomes the same equation for the capacitor voltage in the original Z-source inverter.

III. Current-Fed Trans-Z-Source Inverters

Applying the similar concept to the current-fed Z-source and quasi-Z-source inverters leads to the current-fed trans-Z-source and trans-quasi-Z-source inverters. The current-fed quasi-Z-source inverter with a continuous input current is shown in Fig. 7, with inductors L_1 and L_2 coupled. The dc current source is provided by a dc inductor $L_{\rm dc}$. Similarly, this circuit can be further modified to a current-fed trans-quasi-Z-source inverter as shown in Fig. 8, where $n = n_2/n_1 \geq 1$. The current-fed trans-quasi-Z-source inverters have two unique open zero states besides six active states and three traditional short-circuit (or shoot-through) zero states. The open zero states can be realized by turning off either all the upper switches or all the lower switches. The open zero states are forbidden in the conventional CSI. The new Z-source inverters, however, utilize the open zero state so that the inverter can step up and down the voltage.

Its equivalent circuit viewed from the inverter dc side is shown in Fig. 9(a), assuming an ideal coupling for the transformer. When in an open zero state, the inverter bridge turns to an open circuit as shown in Fig. 9(b). When in one of the nonopen states (which includes the traditional active states and short-circuit zero states), the inverter bridge can be modeled as an equivalent

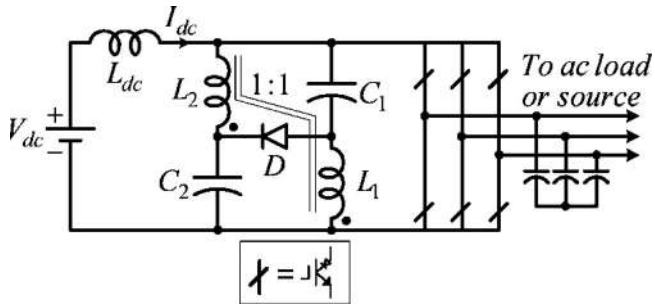


Fig. 7. Current-fed quasi-Z-source inverter with two inductors coupled.

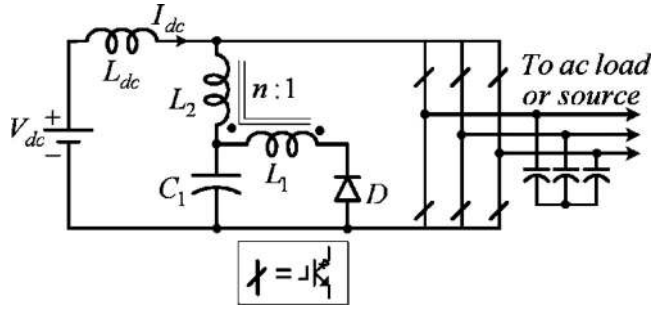


Fig. 8. Current-fed trans-quasi-Z-source inverter.

voltage source v_i as shown in Fig. 9(c). The equivalent voltage source v_i is the line-to-line voltage when in one of the six active states and is zero when in one of the short-circuit zero states.

Using the similar circuit analysis with the aforementioned voltage-fed trans-Z-source inverters, the following current relation and the dc–ac voltage gain can be obtained for the current-fed trans-Z-source inverters. According to the KCL and the relationship of the winding currents, the following relations hold

$$i_{C1} = i_{L1} - i_{L2}, \quad i_{L1} = i_m + i'_{L1}, \quad i'_{L1} + n i_{L2} = 0. \tag{13}$$

In the open-zero states as shown in Fig. 9(b), for a duration of $D_{\rm op}T$, the diode is conducting to carry the current through L_1. From (13), the capacitor current can be expressed as

$$i_{C1} = (1+n) i_{\rm dc} + i_m. \tag{14}$$

In the nonopen states for a duration of $(1 - D_{\rm op})T$, the diode D is biased off; no current flows through L_1. The capacitor current is

$$i_{C1} = -i_{L2} = -\frac{i_m}{n}. \tag{15}$$

With the assumption that the inverter operates in the continuous current mode, given small magnetizing current ripple and input current ripple, both i_m and $i_{\rm dc}$ can be approximated by their dc components I_m and $I_{\rm dc}$, respectively. Application of the amp-second balance to the capacitor yields

$$I_m = \frac{n(1+n) D_{\rm op} I_{\rm dc}}{1 - (1+n) D_{\rm op}}. \tag{16}$$

Substituting I_m into the aforementioned expressions for the nonopen states, the peak value of the current flowing through

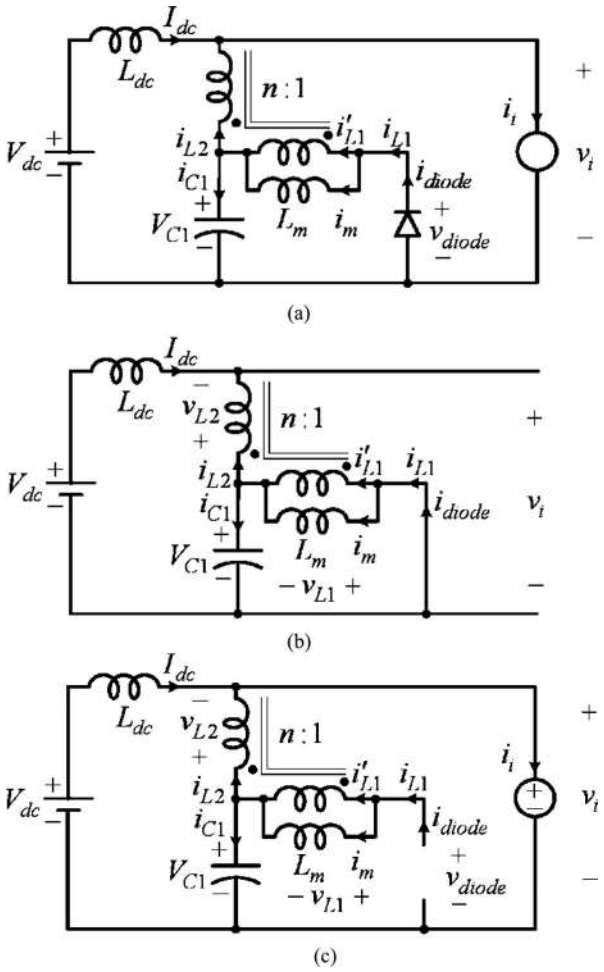


Fig. 9. Equivalent circuits of the current-fed trans-qZSI viewed from the dc link. (a) With the transformer equivalent circuit. (b) Open zero state. (c) Nonopen states.

the inverter dc link can be obtained as

$$\hat{i}_i = \frac{1}{1-(1+n)D_{\rm op}} I_{\rm dc} = B \cdot I_{\rm dc} \tag{17}$$

where *B* is the boost ratio in terms of current. Correspondingly, the ac voltage can be bucked (stepped down). Based on the operation principle of sinusoidal pulse width modulation (SPWM) for the CSI, the maximum duty ratio of two active states in one switching period for each phase can be calculated as

$$D_{A\max} = \max\left\{\frac{M\sin\omega t}{2} - \frac{M\sin(\omega t - 2\pi/3)}{2}\right\} = \frac{\sqrt{3}}{2}M \tag{18}$$

where *M* is the modulation index based on the current reference.

Therefore, the peak value of the line current can be expressed as

$$\hat{i}_l = \left(\frac{\sqrt{3}}{2}M\right)\cdot \hat{i}_i. \tag{19}$$

Assuming the energy conservation of the input and output, the peak value of the line-to-line voltage can be written as

$$\hat{v}_{ll} = \frac{V_{\rm dc}\cdot I_{\rm dc}}{\sqrt{3}\cdot(\hat{i}_l/\sqrt{2})\cdot\cos\varphi}\cdot\sqrt{2} = \frac{4\cdot V_{\rm dc}[1-(1+n)D_{\rm op}]}{3M\cos\varphi} \tag{20}$$

where $\cos\varphi$ is the power factor.

Similar to the voltage-fed ZSI, there are corresponding control methods: simple boost, maximum boost, and constant boost controls in terms of current (or buck in terms of voltage) for the current-fed Z-source inverters. The constant current boost is used here to compare the operation region of the current-fed trans-ZSIs and current-fed ZSIs. In order to keep the active state unchanged, the maximum available open zero duty ratio is

$$D_{\rm op\,max} = 1 - D_{A\max} = 1 - \frac{\sqrt{3}}{2}M. \tag{21}$$

Hence, (20) can be rewritten as

$$\hat{v}_{ll} = \frac{4\cdot V_{\rm dc}[(1+n)(\frac{\sqrt{3}}{2}M-1)+1]}{3M\cos\varphi}. \tag{22}$$

When $n = 1$, (20) and (22) can be proven to be the same as in the Z-source and quasi-Z-source inverters. The ratios of the peak line-to-line voltage to the input voltage as a function of the modulation index are compared in Fig. 10(a) and (b) for (quasi-) Z-source and trans-(quasi-)Z-source inverters, where *n* equals 2 for the trans-Z-source inverters. The blue dash line is the minimum voltage envelope for the buck mode and the regeneration mode, with the constant current boost control. The shaded areas are operable regions with only one additional diode, *D* in Figs. 7 and 8. When no open state is employed (that is, $D_{\rm op} = 0$), the red envelope line in Fig. 10(a) and (b) that can be obtained from (20) depicts the maximum voltage boost gain for both the current-fed (quasi-)Z-source inverters and trans-quasi-Z-source inverters. It is noticeable that, however, the trans-Z-source has a wider boost range in the motoring operation mode. In the current-fed quasi-Z-source inverter [15], the dc-link voltage v_i cannot exceed the sum of capacitor voltages, because the diode will otherwise improperly conduct in the active states and cause waveform distortion. For the same reason, in the trans-quasi-Z-source inverters, to maintain the diode-reversed-biased in the active state, the voltage across it should satisfy

$$v_{\rm diode} = \frac{1}{n}(V_{C1} - v_i) + V_{C1} = \left(1+\frac{1}{n}\right)V_{\rm dc} - \frac{1}{n}v_i \geq 0. \tag{23}$$

Hence, the peak value of the line-to-line voltage is constrained to

$$\hat{v}_i = \hat{v}_{ll} = \frac{4\cdot V_{\rm dc}}{3M\cos\varphi} \leq (1+n)V_{\rm dc}. \tag{24}$$

It implies that the minimum modulation index is related to the power factor seen from the inverter bridge. When $n > 1$, the peak line-to-line voltage can reach $(n+1)V_{\rm dc}$, as shown in Fig. 10(b). Note that the dc–ac voltage gain can also be analyzed by calculating the voltage relation and active duty ratio in the

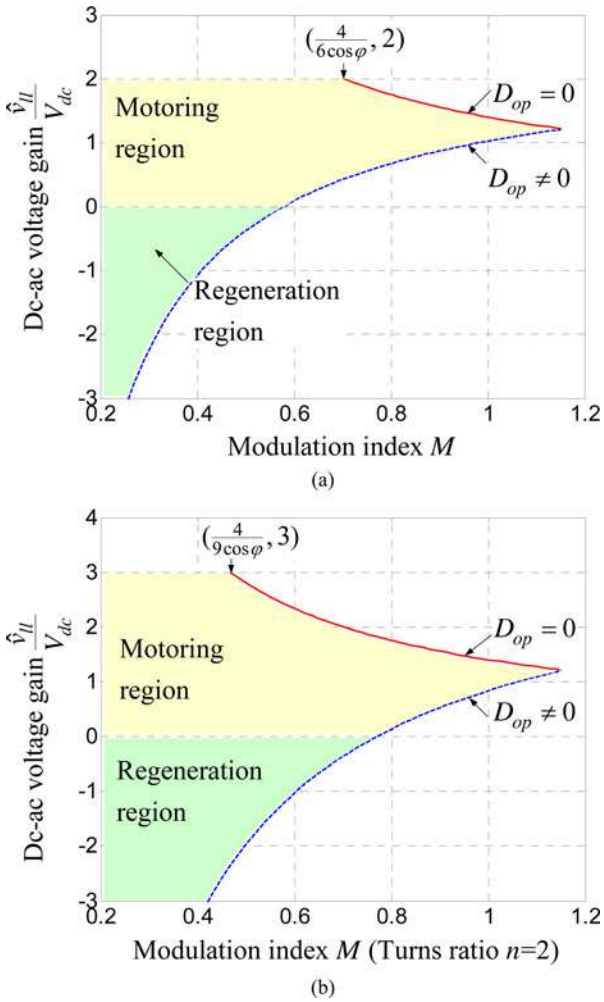


Fig. 10. DC–AC voltage gain and operation region in the current-fed ZSI/qZSI and trans-ZSI/-qZSI. (a) Current-fed ZSI/qZSI. (b) Current-fed trans-ZSI/-qZSI.

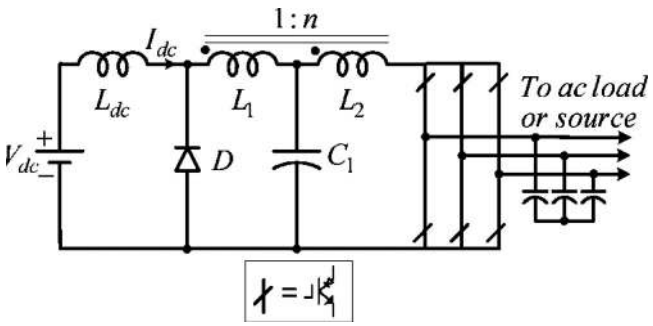


Fig. 11. Current-fed trans-Z-source inverter.

same way as in [15], where the active and short-circuit zero states are depicted separately.

Similarly, a current-fed trans-Z-source inverter can be derived as shown in Fig. 11. It has the same operation principle, voltage gain, and operation regions as the trans-quasi-Z-source inverter, but with different current stress, which will be discussed in the next section.

IV. Comparison With the Z-Source and Quasi-Z-Source Inverters

Table I compares the governing equations for the voltage-fed trans-Z-source, trans-quasi-Z-source, Z-source, and quasi-Z-source inverters. Table II compares the class of current-fed Z-source inverters. Two tables also provide a guideline for determining the ratings of the components such as the active switch, the diode, the capacitor, and the transformer. The voltage and current directions in the Z-source and quasi-Z-source inverters follow the same definition as that shown in the equivalent circuits of the trans-Z-source and trans-quasi-Z-source inverters. All the magnetizing current is reflected to the primary winding. While S_D is the shoot-through switching function in the voltage-fed inverters, it is the open-circuit switching function in the current-fed inverters due to the duality between the voltage-fed and current-fed inverters. S_D is defined as 1 when the inverter is in the shoot-through zero states and 0 when it is in the non-shoot-through states in the voltage-fed inverters. It is 1 for the open zero states and 0 for the nonopen states in the current-fed inverters.

In Table I, when the turns ratio is over 1, the voltage-fed trans-Z-source and trans-quasi-Z-source inverters, with reduced component count, have higher dc-link voltage gain than the voltage-fed Z-source and quasi-Z-source inverters. When the turns ratio is 1, some of the governing equations can be unified, including the relation for the magnetizing current of the two coupled windings. Comparing the voltage-fed trans-Z-source and trans-quasi-Z-source inverters, less capacitance is needed for an input filter capacitor in parallel with the low-voltage dc source in the voltage-fed trans-Z-source inverter, whereas the capacitor voltage stress is reduced in the voltage-fed trans-quasi-Z-source inverter.

In Table II, when the turns ratio is over 1, besides a wider motoring operating range, the current-fed trans-Z-source and trans-quasi-Z-source inverters feature more voltage buck ratio. This feature can also be found in Fig. 10. When the turns ratio is 1, some of the governing equations in the Z-source inverter and quasi-Z-source inverter are consistent with those for the trans-Z-source inverter and trans-quasi-Z-source inverter, respectively. Similar to the Z-source and quasi-Z-source inverters, as shown in Fig. 12, the trans-quasi-Z-source inverter has less magnetizing current than the trans-Z-source inverter in the motoring operation ($I_m > 0$) when the open zero duty ratio $D_{\rm op}$ is $0 < D_{\rm op} < 1/(n+1)$. However, the trans-Z-source inverter has less magnetizing current (absolute value) than the trans-quasi-Z-source inverter does in the regeneration operation ($I_m < 0$) when the open zero duty ratio $D_{\rm op}$ is $1/(n+1) < D_{\rm op} < 1$.

Admittedly, as can be seen from Table I, the new voltage-fed trans-Z-source inverters mitigate the switch stress while transferring the stress to the less costly passive device, the diode. Therefore, the boost ratio also cannot avoid its practical limit, although it is an improvement on the boost ratio to some extent from the voltage-fed Z-source inverters. Besides, from the inductor currents in Tables I and II, very high power transformer is difficult to implement. Since the transformer has some characteristics like the transformer in the flyback dc–dc converter, the transformer should be designed with low leakage inductance.

TABLE I
COMPARISON OF THE VOLTAGE-FED TRANS-ZSI/-qZSI AND ZSI/qZSI

	Voltage-fed trans-ZSI	Voltage-fed trans-qZSI	Voltage-fed ZSI with coupled inductors (CL)	Voltage-fed qZSI with continuous input current and CL
Dc-link voltage v_i	$\bar{S}_D \cdot \frac{1}{1-(1+n)D_{sh}} V_{dc}$	$\bar{S}_D \cdot \frac{1}{1-(1+n)D_{sh}} V_{dc}$	$\bar{S}_D \cdot \frac{1}{1-2D_{sh}} V_{dc}$	$\bar{S}_D \cdot \frac{1}{1-2D_{sh}} V_{dc}$
Diode voltage v_{diode}	$S_D \cdot \frac{n}{1-(1+n)D_{sh}} V_{dc}$	$S_D \cdot \frac{n}{1-(1+n)D_{sh}} V_{dc}$	$S_D \cdot \frac{1}{1-2D_{sh}} V_{dc}$	$S_D \cdot \frac{1}{1-2D_{sh}} V_{dc}$
Capacitor voltage V_{C1}	$\frac{1-D_{sh}}{1-(1+n)D_{sh}} V_{dc}$	$\frac{n \cdot D_{sh}}{1-(1+n)D_{sh}} V_{dc}$	$\frac{1-D_{sh}}{1-2D_{sh}} V_{dc}$	$\frac{D_{sh}}{1-2D_{sh}} V_{dc}$
Capacitor voltage V_{C2}	Not applicable	Not applicable	$\frac{1-D_{sh}}{1-2D_{sh}} V_{dc}$	$\frac{1-D_{sh}}{1-2D_{sh}} V_{dc}$
Magnetizing current i_m	$(1+n)\frac{P}{V_{dc}}$ with ripple	$(1+n)\frac{P}{V_{dc}}$ with ripple	$\frac{2P}{V_{dc}}$ with ripple	$\frac{2P}{V_{dc}}$ with ripple
Inductor current i_{L1}	$\bar{S}_D \cdot i_i + S_D \cdot i_m$	$\bar{S}_D \cdot i_i + S_D \cdot i_m$	$\frac{P}{V_{dc}}$ with ripple	$\frac{P}{V_{dc}}$ with ripple
Inductor current i_{L2}	$\bar{S}_D \cdot (i_m - i_i)/n$	$\bar{S}_D \cdot (i_m - i_i)/n$	$\frac{P}{V_{dc}}$ with ripple	$\frac{P}{V_{dc}}$ with ripple
Input current i_{dc}	The same as i_{L2}	The same as i_{L1}	$\bar{S}_D \cdot (2i_{L1} - i_i)$	The same as i_{L1}
Diode current i_{diode}	The same as i_{L2}	The same as i_{L2}	$\bar{S}_D \cdot (2i_{L1} - i_i)$	$\bar{S}_D \cdot (2i_{L1} - i_i)$
Capacitor current i_{C1} (and i_{C2} for ZSI/qZSI)	$i_{L2} - i_{L1}$	$i_{L2} - i_{L1}$	$\bar{S}_D \cdot (\frac{P}{V_{dc}} - i_i) + S_D \cdot (-\frac{P}{V_{dc}})$	$\bar{S}_D \cdot (\frac{P}{V_{dc}} - i_i) + S_D \cdot (-\frac{P}{V_{dc}})$

TABLE II
COMPARISON OF THE CURRENT-FED TRANS-ZSI/-qZSI AND ZSI/qZSI

	Current-fed trans-ZSI	Current-fed trans-qZSI	Current-fed ZSI with L_1 and L_2 coupled	Current-fed qZSI with continuous input current and L_1 and L_2 coupled
Peak line-to line voltage $\hat{v}_{ll}$	$\frac{4 \cdot V_{dc}[1-(1+n)D_{op}]}{3M\cos\varphi}$	$\frac{4 \cdot V_{dc}[1-(1+n)D_{op}]}{3M\cos\varphi}$	$\frac{4 \cdot V_{dc}[1-2D_{op}]}{3M\cos\varphi}$	$\frac{4 \cdot V_{dc}[1-2D_{op}]}{3M\cos\varphi}$
Diode voltage v_{diode}	$(1+\frac{1}{n})V_{dc} - \frac{1}{n}v_i \geq 0$	$(1+\frac{1}{n})V_{dc} - \frac{1}{n}v_i \geq 0$	$2V_{dc} - v_i \geq 0$	$2V_d - v_i \geq 0$
Capacitor voltage V_{C1} (and V_{C2} for ZSI/qZSI)	V_{dc}	V_{dc}	V_{dc}	V_{dc}
Input current I_{dc}	$\frac{P}{V_{dc}}$	$\frac{P}{V_{dc}}$	$\frac{P}{V_{dc}}$	$\frac{P}{V_{dc}}$
Magnetizing current i_m	$\frac{(1+n)(1-D_{op})}{1-(1+n)D_{op}} I_{dc}$ with ripple	$\frac{n(1+n)D_{op}}{1-(1+n)D_{op}} I_{dc}$ with ripple	$\frac{2(1-D_{op})}{1-2D_{op}} I_{dc}$ with ripple	$\frac{2D_{op}}{1-2D_{op}} I_{dc}$ with ripple
Inductor current i_{L1}	$\bar{S}_D \cdot I_{dc} + S_D \cdot i_m$	$S_D \cdot \frac{n}{1-(1+n)D_{op}} I_{dc}$	$\frac{1-D_{op}}{1-2D_{op}} I_{dc}$ with ripple	$\frac{D_{op}}{1-2D_{op}} I_{dc}$ with ripple
Inductor current i_{L2}	$\bar{S}_D \cdot \frac{I_{dc}}{1-(1+n)D_{op}}$	$\bar{S}_D \cdot i_m / n + S_D \cdot (-I_{dc})$	$\frac{1-D_{op}}{1-2D_{op}} I_{dc}$ with ripple	$\frac{D_{op}}{1-2D_{op}} I_{dc}$ with ripple
Diode current i_{diode}	$S_D \cdot \frac{n}{1-(1+n)D_{op}} I_{dc}$	$S_D \cdot \frac{n}{1-(1+n)D_{op}} I_{dc}$	$S_D \cdot \frac{1}{1-2D_{op}} I_{dc}$	$S_D \cdot \frac{1}{1-2D_{op}} I_{dc}$
Capacitor current i_{C1}, i_{C2}	$i_{L1} - i_{L2}$	$i_{L1} - i_{L2}$	$\bar{S}_D \cdot (I_{dc} - i_{L1}) + S_D \cdot i_{L1}$	$\bar{S}_D \cdot (-i_{L1}) + S_D \cdot (I_{dc} + i_{L1})$

Similar to the flyback dc–dc converter, the low component count is an attractive figure of merit that makes the trans-Z-source inverters suitable for low to medium power applications.

V. SIMULATION AND EXPERIMENTAL RESULTS

Two prototypes for the voltage-fed trans-quasi-Z-source and current-fed trans-quasi-Z-source inverters were built to validate the analysis. The system configuration for the simulation and experiments of the voltage-fed trans-quasi-Z-source inverter is shown in Fig. 13. The switching frequency for the SPWM is 10 kHz. The capacitance of C_1 is 400 μF. The transformer consists of two bifilar windings. The turns ratio n_2/n_1 is 2:1. The magnetic inductance measured from the primary side is 207 μH. There is no snubber circuit for the inverter bridge, thanks to the very low leakage inductance (around 100 nH mainly from the outside connection) and the parasitic capacitance in the tightly

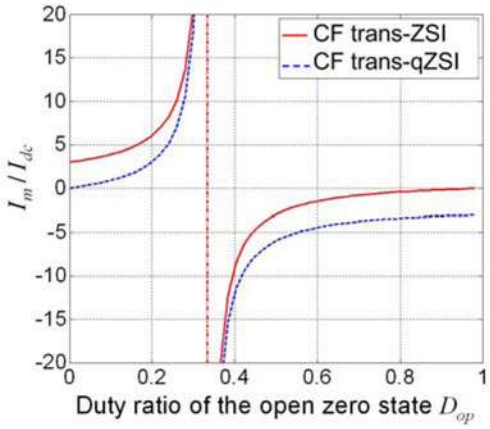


Fig. 12 Comparison of normalized magnetizing currents in trans-ZSI and trans-qZSI

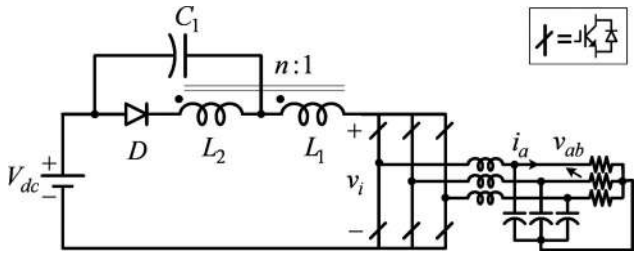
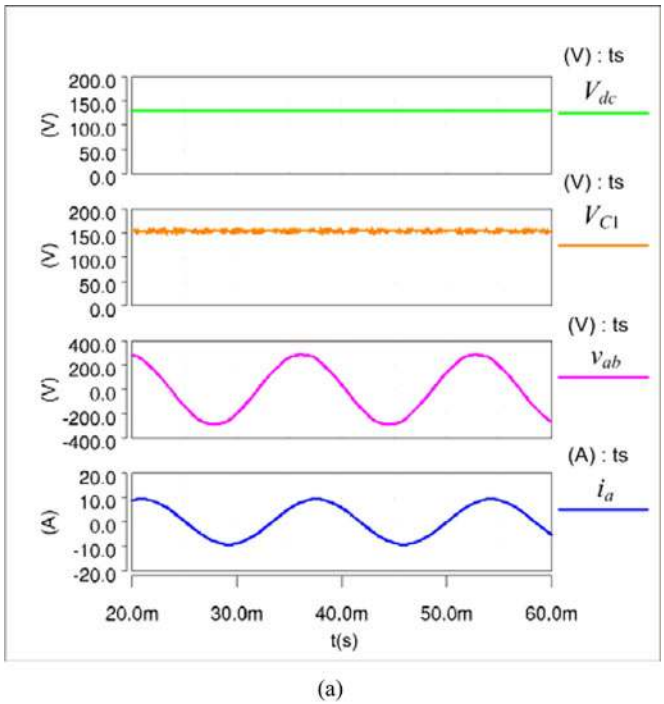
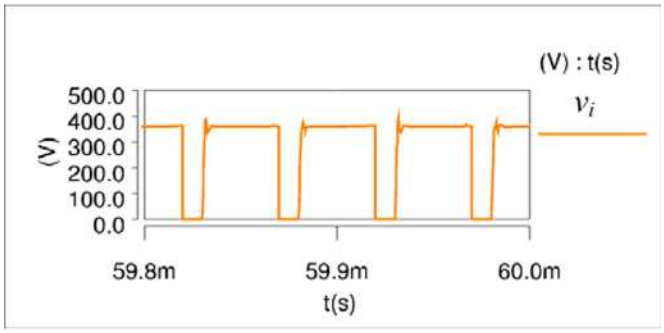


Fig. 13. Simulation and experimental system configuration of the voltage-fed trans-qZSI.



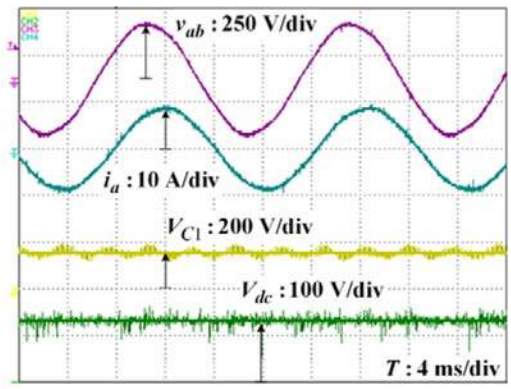
(a)



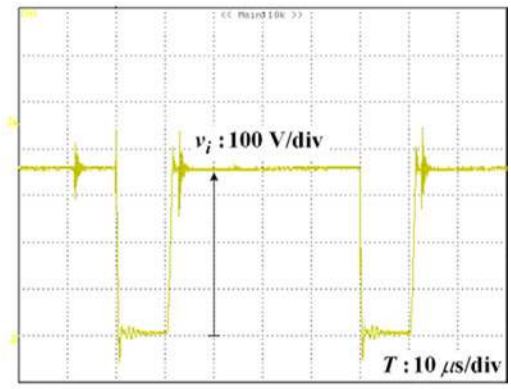
(b)

Fig. 14. Simulation results of the voltage-fed trans-qZSI considering the parasitic capacitance of the bifilar winding (constant boost control, $M = 0.93$, $D_{\rm sh} = 0.2$). (a) Input and capacitor voltages and output voltage/current. (b) Inverter dc-link voltage.

coupled bifilar windings. The parasitic capacitance lowers the dv/dt and more interestingly increases the effective boost ratio. That is because the inductor L_1 is still charged during the IGBT turn-off transition until the dc-link voltage increases and the diode then becomes forward biased. However, it is still able to achieve the desired dc voltage boost ratio by controlling



(a)



(b)

Fig. 15. Experimental waveforms of the voltage-fed trans-qZSI (constant boost control, $M = 0.93$, $D_{\rm sh} = 0.2$). (a) Input and capacitor voltages and output voltage/current. (b) Inverter dc-link voltage.

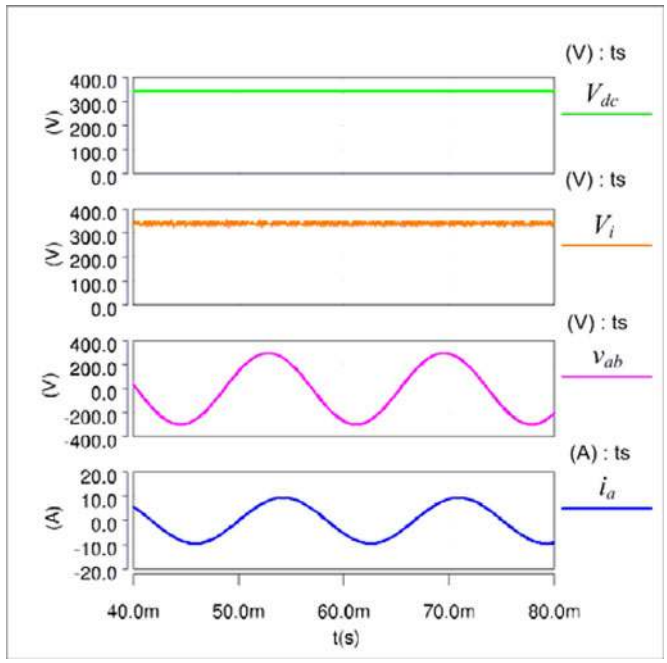


Fig. 16. Simulation results of the voltage-fed trans-qZSI without boost ($M = 1$).

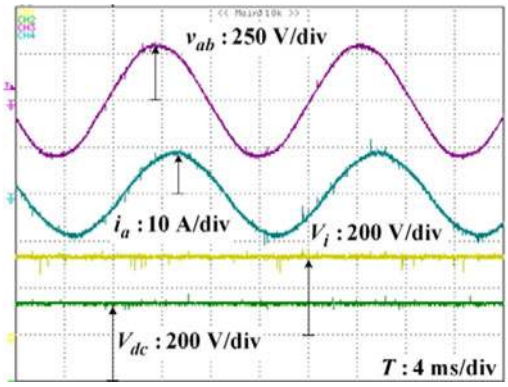


Fig. 17. Experimental waveforms of the voltage-fed trans-qZSI without boost ($M = 1$).

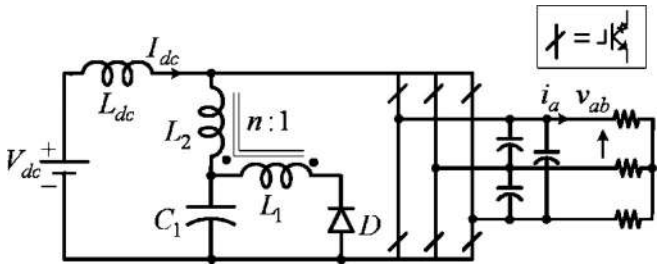


Fig. 18. Simulation and experimental system configuration of the current-fed trans-qZSI.

the shoot-though duty ratio. The simulation and experimental results of the boost mode operation are shown in Figs. 14 and 15, respectively. The output line-to-line voltage is boosted to 208 V RMS (or 294 V peak) with an input voltage of 130 V. The constant boost control is used, with the shoot-through duty ratio 0.2 and the modulation index 0.93. Both the input voltage and the voltage stress are lower than the reported results of Z-source inverter in [6] to produce the same output voltage. Besides, no significant voltage overshoot (less than 20%) was observed in the dc-link voltage, due to tight coupling between the primary and secondary. The capacitor voltage of 152 V demonstrates the low capacitor voltage requirement in the voltage-fed trans-quasi-Z-source inverter. The simulation and experimental results are shown in Figs. 16 and 17 for the operation without boost, like the traditional voltage source inverters. It needs a dc input voltage of 339 V to output the same ac output voltage.

The new feature of the current-fed trans-Z-source inverters is demonstrated by the simulation and experiments of a trans-quasi-Z-source inverter. The configuration is shown in Fig. 18. The inverter bridge is built with an RB-IGBT package from Fuji. The dc input inductor $L_{\rm dc}$ is 1 mH. The magnetic inductance of the transformer is 207 μH from the primary side. The capacitance of C_1 in the impedance-source network is 100 μF. The three-phase ac outputs are loaded with three 10-Ω resistive loads in a Y-connection. Each ac filter capacitor is just 40 μF in a Δ-connection. The resultant power factor is 0.911. The switching frequency is 10 kHz. Figs. 19 and 20 compare the simulation and experimental results for a modulation index of 0.6, without open zero states. Figs. 19(a) and 20(a) show the

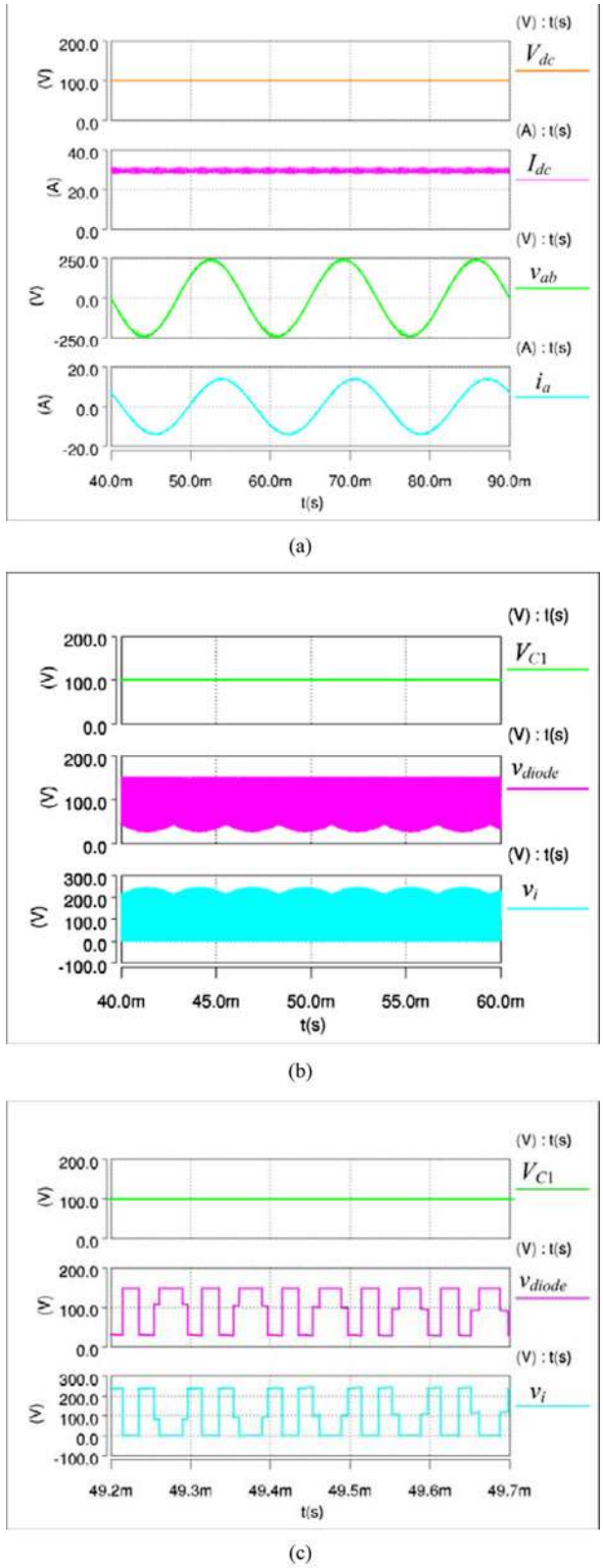


Fig. 19 Simulation results of the current-fed trans-qZSI ($M = 0.6$). (a) Input and output voltage/current. (b) Capacitor, diode, and inverter bridge voltages. (c) Zoom-in of capacitor, diode, and inverter bridge voltages.

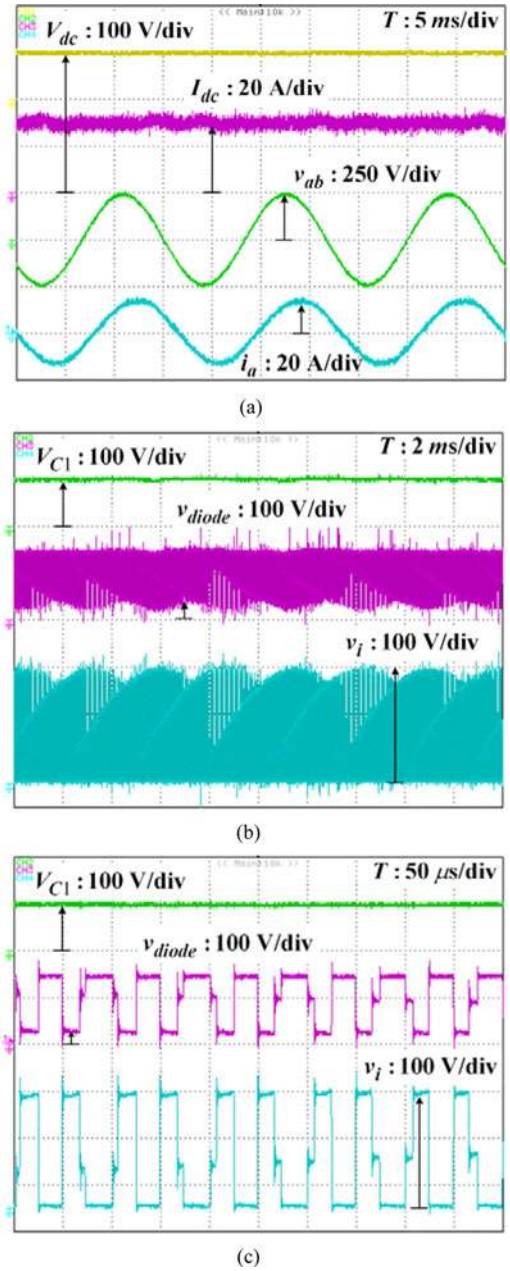


Fig. 20. Experimental waveforms of the current-fed trans-qZSI ($M = 0.6$). (a) Input and output voltage/current. (b) Capacitor, diode, and inverter bridge voltages. (c) Zoom-in of capacitor, diode, and inverter bridge voltage.

input and output voltages/currents, the output line-to-line voltages are 172 V RMS (243 V peak) with an input voltage of 100 V, and thus the ratio $\hat{v}_{ll}/V_{\rm dc}$ is 2.43 times, which agree with the theoretical calculation. With this power factor, the original current-fed quasi-Z-source inverter [15] cannot exceed a voltage ratio of 2. Figs. 19(b) and 20(b) show the capacitor voltage V_{C1}, and voltages for the diode and the inverter bridge. Thus the average winding current can be inferred as being equal to zero from the capacitor voltage under this condition. The minimum diode voltage is more clearly zoomed in as shown in Figs. 19(c) and 20(c). As can be seen, the diode is reversed biased over the entire fundamental cycle. In sum, both the simulation and experimental results verify the extended motoring operating range of the current-fed trans-quasi-Z-source inverter.

VI. Conclusion

A class of trans-Z-source inverters has been presented for voltage-fed and current-fed dc–ac inversion systems. When the turns ratio of the two windings is over 1, the voltage-fed trans-Z-source inverter can obtain a higher boost gain with the same shoot-through duty ratio and modulation index, compared with the original Z-source inverter; the current-fed trans-Z-source-inverter can extend the motoring operation range to more than that can be achieved in the original Z-source and quasi-Z-source inverters. With new unique features, they can broaden applications of the Z-source inverters. For instance, the voltage-fed trans-Z-source inverters provide a promising potential in the applications with very low input voltage, such as the microinverter for the photovoltaic systems. Simulation and experimental results of the voltage-fed trans-quasi-Z-source and the current-fed trans-quasi-Z-source inverters have verified the analysis and feature.

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