Transformerless DC-to-DC Converters with Large Conversion Ratios

R. D. MIDDLEBROOK, FELLOW, IEEE

Abstract—A new switching dc-to-dc converter is introduced in which large voltage step-down ratios can be achieved without a very small duty ratio and without a transformer. The circuit is an extension of the Ćuk converter to incorporate a multistage capacitor divider. A particularly suitable application would be a 50-V to 5-V converter in which dc isolation is not required. The absence of a transformer and a larger duty ratio permits operation at a high switching frequency and makes the circuit amenable to partial integration and hybrid construction techniques. An experimental 50-W three-stage voltage divider Ćuk converter converts 50 V to 5 V at 500 kHz, with efficiency higher than for a basic Ćuk converter operated at the same conditions. A corresponding voltage-multiplier Ćuk converter is described, and also dual buck–boost-derived step-down and step-up converters.

I. INTRODUCTION

THE NEED is growing for a converter/regulator to provide +5-V output from a nominal −48-V input and with a low profile capable of assembly on a plug-in card. An obvious motivation exists to use a switching frequency at least in the hundreds of kHz to reduce magnetics sizes and to take advantage of hybrid construction techniques. With the advent of power MOSFETs, the switching frequency is limited by the magnetics rather than by the switch.

More specifically, it is a transformer that limits the frequency, rather than an inductor, because the ratio of leakage to magnetizing inductance increases as the physical size decreases. A transformer commonly provides two functions in a dc-to-dc switching converter: it provides dc isolation, and it provides an additional voltage conversion ratio over and above that available from the switch duty ratio.

In applications where dc isolation is not needed, a transformer (or an autotransformer) would normally still be required if the necessary voltage conversion ratio is large. For example, in a 50-to-5-V converter, the switch duty ratio would have to be about 0.1 if a transformer were not used, which severely limits the switching frequency and the dynamic range, and also has undesirable implications with respect to peak currents, loss of efficiency, and noise. On the other hand, if a transformer were used, the switching frequency would also be severely limited by the transformer itself. This paper sug- gests a way to avoid both these undesirable solutions by introducing a voltage-divider property that does not require a transformer.

II. THE VOLTAGE-DIVIDER ĆUK CONVERTER

The new circuit is another extension of the basic Ćuk converter [1, vol II, sec. 18], introduced in 1976 as a solution to the problem of achieving nonpulsating current at both input and output with a minimum number of components. In the Ćuk converter, shown in Fig. 1, the capacitor is charged by the input inductor current when the transistor is off and the diode is on and is discharged through the output inductor when the transistor is on and the diode is off.

As far as the basic conversion property is concerned, the converter may be considered a coalesced boost followed by a buck converter, in which the capacitor average voltage V_c corresponds to the output of the boost stage, given by $V_g/(1 - D)$ and also to the input of the buck stage whose output V is DV_c. Hence the overall input-to-output conversion ratio is $M \equiv V/V_g = D/(1 - D)$ where D is the fractional on-time of the transistor and V_g is the input voltage. This is the same functional relationship as in the flyback converter and permits either up or down conversion.

Polarity inversion between input and output occurs because during charge the positive capacitance terminal is grounded through the diode, and during discharge the negative end is grounded through the transistor. The circuit is normally designed to operate in the "continuous capacitance voltage mode" in which the polarity of the capacitance voltage does not reverse [1, vol. II, sec. 27].

The Ćuk converter is unique compared with the conventional buck, flyback, and other converters in that it utilizes capacitive rather than magnetic energy transfer. It is this property that permits the capacitance voltage-divider feature to be incorporated. The new circuit, shown in its simplest form in Fig. 2, is a "voltage-divider Ćuk converter," in which two energy transfer capacitors are charged in series when the transistors are off and discharged in parallel when the transistors are on. Thus, effectively, a two-to-one voltage division is introduced, and the overall conversion ratio is $M = D/2(1 - D)$ where D is the duty ratio of the two transistors driven on and off simultaneously.

This concept can be generalized to where N capacitors
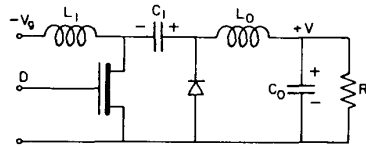
Fig. 1. Basic Ćuk converter.
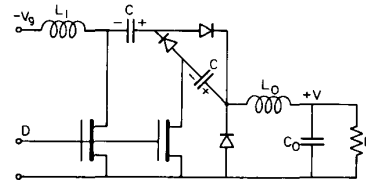
Fig. 2. New voltage-divider Ćuk converter with two stages.

Fig. 3. Generalized N-stage voltage-divider Ćuk converter.

(a)

(b)

Fig. 4. N-stage converter. (a) During driving transistor off-time, N capacitors are charged in series. (b) During transistor on-time, N capacitors are discharged in parallel.

are charged in series and discharged in parallel, as shown in Fig. 3, so that the overall conversion ratio is $D/N(1 - D)$. The circuit configuration is shown in Fig. 4 for the two intervals that comprise the switching cycle. The transistors and diodes are assumed to be ideal switches. During the fractional off-time $(1 - D)$ of the transistors, shown in Fig. 4(a), the N energy transfer capacitors are charged in series by the input current I_g. During the transistor fractional on-time D, shown in Fig. 4(b), each capacitor supplies one Nth of the output current I. By volt-second balance across the input inductor L_1, the voltage across all N capacitors in series is $V_c = V_g/(1 - D)$ (the same expression as for the basic Ćuk converter), and this voltage is shared equally by the N capacitors as a result of automatic self-adjustment when the capacitors are paralleled during the transistor fractional on-time D.

In comparison with the basic Ćuk converter, the new converter operates at a higher duty ratio for the same overall conversion ratio $M = V/V_g$. The relation between the respective duty ratios D_N and D_1 is obtained from

$$\frac{D_N}{N(1 - D_N)} = M = \frac{D_1}{1 - D_1} \tag{1}$$

which leads to

$$D_N = \frac{ND_1}{1 + D_1(N - 1)} \tag{2}$$

and

$$D_N = \frac{NM}{1 + NM} \qquad D_1 = \frac{M}{1 + M}. \tag{3}$$

Thus D_N is larger than D_1 and permits a higher switching frequency to be used with transistors having given switching times.

Stress levels are also lower on some of the components, partly as a result of sharing between the extra elements where N is greater than unity. In particular, transistor Q_1 carries only the input current plus one Nth of the output current, and the extra transistors carry only one Nth of the output current. On the other hand, the voltage stress on Q_1, which is $V_g/(1 - D)$, is higher because of the higher
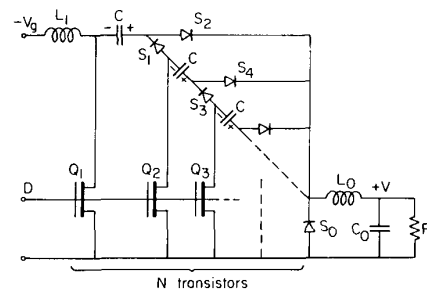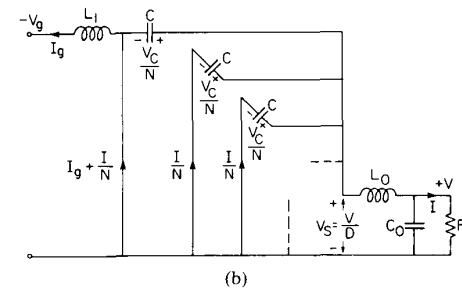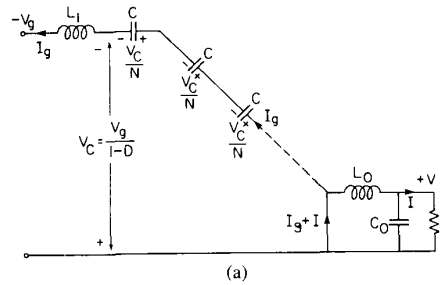
D. The output diode still carries the sum of the input and output currents, but for a shorter fractional time $(1 - D)$; its voltage stress level V/D is also lower.

Previously described extensions of the basic Ćuk converter can also be incorporated into the new circuit. For example, the input and output inductors may be coupled, with the attendant ripple steering properties [1, vol. II, secs. 19, 20]. Transformer isolation may be introduced between the two capacitors that result from splitting the first energy transfer capacitor into two in series [1, vol. II, secs. 22, 26; vol. III, secs. 12, 18], in which case all the magnetics may be integrated [1, vol. II, sec. 28; vol. III, secs, 2, 15, 21].

Of course, introduction of an isolation transformer may obviate the advantage obtained by the voltage divider circuitry, but it may be beneficial in some applications since the required transformer turns ratio would be smaller by the voltage division ratio. Also, in multiple outputs the relative volts-per-turn constraints would be eased. On the other hand, the dc isolation transformer would require
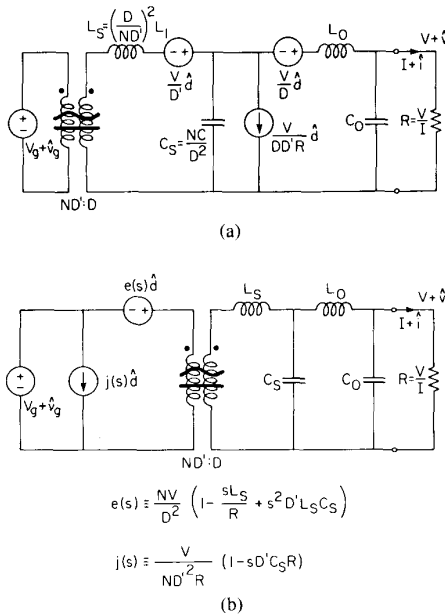
(a)

$$e(s) = \frac{NV}{D^2} \left(1 - \frac{sL_S}{R} + s^2 D'L_S C_S \right)$$

$$j(s) = \frac{V}{ND'^2 R} (1 - sD'C_S R)$$

(b)

Fig. 5. Small-signal model of N-stage voltage-divider Ćuk converter. (a) In form resembling buck converter preceded by input filter. (b) In canonical form.

Fig. 6. Experimental three-stage voltage-divider Ćuk converter operated at 500 kHz.

C_1, C_2, C_3	TRW-35 1-μF 100-V polypropylene, paralleled by two 0.1-μF ceramics,
L_1	124-μH 56-mΩ (25T #22 on Ferroxcube 1811 PA 250 387 pot core),
L_0	5-μH 3-mΩ (6T 1.4 mm $\times$ 5.0 mm rectangular wire on Magnetics Inc. F material 1811 pot core),
C_0	100-μF 35-V, paralleled by a 1-μF ceramic,
C_1	1-μF ceramic.

The circuit operates as expected at a switching frequency of 500 kHz. The drain voltage V_{DS} and current I_D waveforms for each transistor are shown in Fig. 7. The calculated (ideal) duty ratio for $M = 0.1$ and $N = 3$ is

$$D_3 = \frac{NM}{1 + NM} = 0.23$$

compared with the value 0.28 observed in Fig. 7.

The waveforms shown in Fig. 7 are direct plots taken from a Tektronix 7854 digital sampling oscilloscope. The waveforms are quite clean, although ringing is very sensitive to the wire loop added for insertion of the current probe. All the voltage waveforms were taken without any such loops, and the current waveforms were taken with a loop only for the current being measured.

Efficiency measurements on the $N = 3$ converter were made over a range of input voltage with the output maintained constant at 5 V. The input current was measured with a Triplett 630-NA. The results, shown in Fig. 8, indicate a broad maximum in the range 72–74 percent from about $V_g = 40$–100 V.

Of more interest than the actual efficiency value, however, is whether, for a given conversion ratio M, the multistage converter has higher efficiency than the original single-stage converter. To effect as close a comparison as possible, the same components in the three-stage converter (and in the same layout) were reconnected in parallel, and the energy transfer capacitor consisted of C_1 and C_3 in parallel; C_2 and S_1 through S_4 were omitted. The

separate drives for the first transistor on the primary side and for the others on the secondary side.

The small-signal model of the new voltage-divider Ćuk converter can be obtained by straightforward application of the state-space averaging analysis method [1, vol. I, sec. 6]. The result is shown in Fig. 5 in two forms: in Fig. 5(a) the model is presented in the form that exposes the similarity to the model of the buck converter with input filter; in Fig. 5(b) the model is in the canonical form in which the modulation generators are in front of the two-section filter. As would be anticipated, both these forms are the same as for the original Ćuk converter except that certain element values are modified by the voltage-divider ratio N. Interpretation and utilization of both models have been extensively discussed elsewhere [1, vol. II, sec. 25].

III. EXPERIMENTAL RESULTS

A three-stage voltage-divider Ćuk converter ($N = 3$) has been constructed to demonstrate feasibility. The circuit, shown in Fig. 6, is constructed on a printed circuit board with short length, large area connections. The circuit is designed for a nominal conversion ratio $M = V/V_g = 5$ V/50 V = 0.1. Because only N-channel MOSFET transistors were conveniently available, the polarities are positive in, negative out. All the diodes are Schottkys.

The component list is as follows:

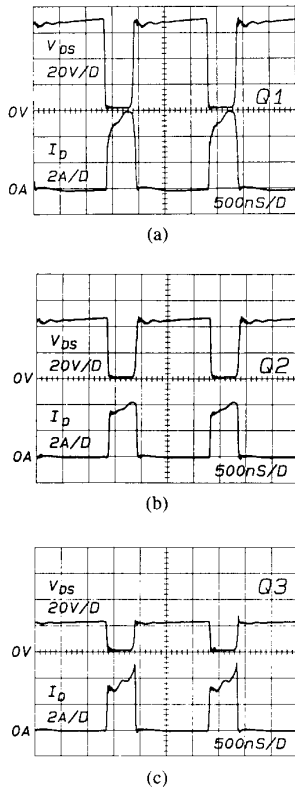|	
Q_1, Q_2, Q_3	RFP10N15 RCA N-channel MOSFET (150 V, 10 A, 0.3 Ω),
S_1, S_3, S_4	1N5822 (40 V, 3 A),
S_2	Fuji ERC88-099 (90 V, 5 A),
S_0	Unitrode USD945 (45 V, 16 A),

(a)

(b)

(c)

Fig. 7. Drain voltage V_{DS} and drain current I_D waveforms for circuit of Fig. 6 operated at 500 kHz. (a) For Q_1. (b) For Q_2. (c) For Q_3.
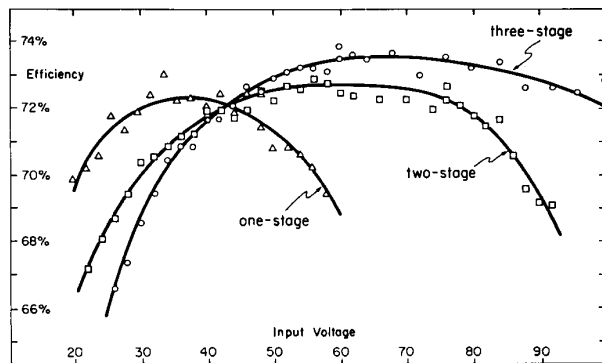

Fig. 8. Efficiency as function of input voltage for three-stage Ćuk converter of Fig. 6, and for same components reconnected as two-stage and single-stage converters. Output maintained at 5 V, 50 W in all cases.

drain voltage and drain current waveforms are shown in Fig. 9. The duty ratio necessary to realize the conversion ratio 50 to 5 V is reduced to 0.11.

The efficiency measurements for the single-stage converter are also shown in Fig. 8, as well as those for the intermediate two-stage converter. The broad maximum in efficiency does indeed move to higher input voltages for a greater number of stages, confirming the expectation that the multistage converter can deliver higher efficiencies for large step-down ratios.
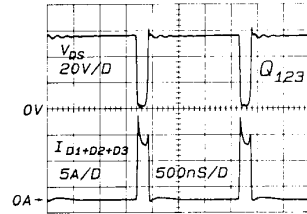

Fig. 9. Drain voltage and current waveforms for three parallelled transistors when circuit of Fig. 6 is reduced to basic (single-stage) Ćuk converter.
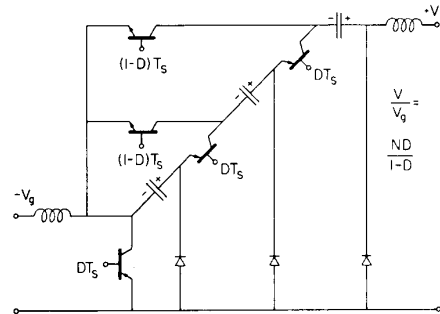

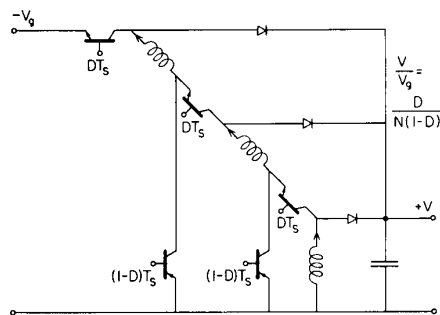Fig. 10. Principle of three-stage voltage-multiplier Ćuk converter.

Fig. 11. Principle of three-stage voltage step-down buck–boost converter.

IV. OTHER LARGE-RATIO STEP-UP AND STEP-DOWN CONVERTERS

The previously described voltage step-down Ćuk converter is based on the energy transfer capacitor being divided into N capacitors which are charged in series and discharged in parallel. Each extra energy transfer capacitor requires one extra transistor and two extra diodes.

An analogous extension leads to a voltage step-up Ćuk converter, in which N capacitors are charged in parallel and discharged in series (Fig. 10, for $N = 3$). Each extra capacitor requires two extra transistors and one extra diode.

A dual procedure leads to voltage step-down and voltage step-up extensions of the buck–boost converter. In the voltage step-down buck–boost converter (Fig. 11 for $N = 3$), the energy-transfer inductor is divided into N inductors which are charged in series and discharged in parallel. Each extra inductor requires two extra transistors and one extra diode.
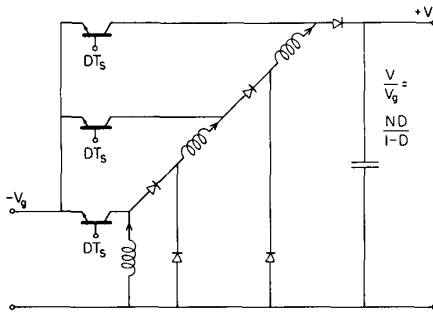
Fig. 12. Principle of three-stage voltage step-up buck–boost converter.

In the voltage step-up buck–boost converter (Fig. 12 for $N = 3$), the N inductors are charged in parallel and discharged in series. Each extra inductor requires one extra transistor and two extra diodes.

In either the voltage step-up or the step-down buck–boost converter, one or more of the inductors may be coupled to give the additional ripple-steering feature. The buck–boost-based multiple-inductor converters compare less favorably with the conventional transformer-coupled versions because they require additional magnetics, contrary to the original motivation to reduce the magnetics.

V. CONCLUSIONS

The voltage-divider Ćuk converter permits large overall step-down conversion ratios to be achieved without a transformer and yet with switch duty ratios that are not crunched at the low end, permitting higher switching frequencies to be used that take full advantage of power MOSFET fast switching speeds. Other advantages are that all the transistors have a common ground and can be driven in parallel from a single drive source, each additional transistor and shunt diode carries only one Nth of the output current, and each series diode carries only the input current. The circuit is particularly suitable for partial integration and hybrid construction techniques.

Experimental results confirm the basic operation of a 50–5 V 50 W three-stage voltage-divider Ćuk converter.

Reconnection as a single-stage and as a two-stage converter, still delivering 50 W at 5 V, verifies that the efficiency maximizes at larger conversion ratios for a greater number of stages.
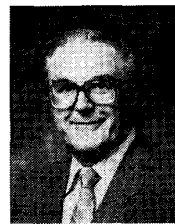
A corresponding voltage-multiplier Ćuk converter is described in Section IV, and also dual step-down and step-up converters based on the buck–boost circuit. A U.S. patent (4 654 769) has been issued for the voltage-divider Ćuk converter.

REFERENCES

[1] R. D. Middlebrook and S. Ćuk, *Advances in Switched-Mode Power Conversion*, vols. I–III. Pasadena, CA: TESLAco, 1983.

R. David Middlebrook (S'55–M'56–SM'58–F'78) was born in England on May 16, 1929. He received the B.A. and M.A. degrees from Cambridge University, England, and the M.S. and Ph.D. degrees from Stanford University, Stanford, CA, in 1952, 1954, 1953, and 1955, respectively.

He is a Professor of Electrical Engineering at the California Institute of Technology, Pasadena. His interests include solid-state device modeling, circuits and systems, and power processing electronics in which he is both Lecturer and Consultant. He is especially interested in design-oriented circuit analysis and measurement techniques which he teaches at Caltech and through short courses in both Europe and the U.S.

Dr. Middlebrook is the recipient of the 1982 IEEE William E. Newell Power Electronics Award for Outstanding Achievement in Power Electronics and a 1982 Award for Excellence in Teaching, presented by the Board of Directors of the Associated Students of Caltech. He is the author of numerous papers, a book on solid-state device theory, and one on differential amplifiers.