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Transmission Line Modeling of Vias in Differential Signals

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Abstract

Signal layer transitions in differential lines are modeled using both FDTD and equivalent circuit methods. The equivalent circuit is developed based on transmission-line reasoning regarding via behavior. Parameters of each transmission-line segment are obtained based on its corresponding physical geometry. The mixed-mode S-parameters from the equivalent circuit and the FDTD modeling are compared. Good agreement is demonstrated in the frequency range from 1 GHz to 20 GHz. The results indicate that vias in differential lines can be modeled as a transmission line for a quick and easy engineering estimation of the differential signal behavior in an environment of signal layer transitions.

Keywords

FDTD, equivalent circuit and differential transmission line

INTRODUCTION

With the increase of operating frequency and edge rates in high-speed digital systems, signal propagation can be affected by the vias used for signal layer transitions. Because of the complex three-dimensional geometry, full-wave analysis was applied in the past and network parameters were calculated [1-5]. Because full-wave methods are computationally intense and time consuming, it is desirable to extract equivalent circuits for engineering modeling. Equivalent circuits were extracted in the past using curve-fitting approaches based on the network parameters obtained from full wave analysis [2-4]. In [6] and [7], the equivalent network for both single via and weakly coupled vias was developed by dividing the via structure into cascaded sub-networks, and the parameters of each sub-network were obtained based on the geometrical layout of each part. Vias in differential signaling have also been analyzed using a cascade of lumped capacitances and inductances [8].

In this study, vias in differential transmission lines are modeled as transmission line segments in order to provide a quick and easy engineering method for analyzing differential signal integrity issues. Two common printed circuit board stackups were examined, one with a 3-layers transition and the other with a 4-layers transition. The boards were modeled using the Finite Difference Time Domain (FDTD) method, then by an equivalent circuit based on transmission line reasoning.

FDTD MODELING

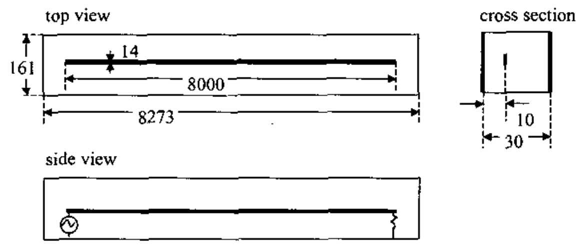

Figure 1. Geometry of a single-ended stripline. Units are in mils.

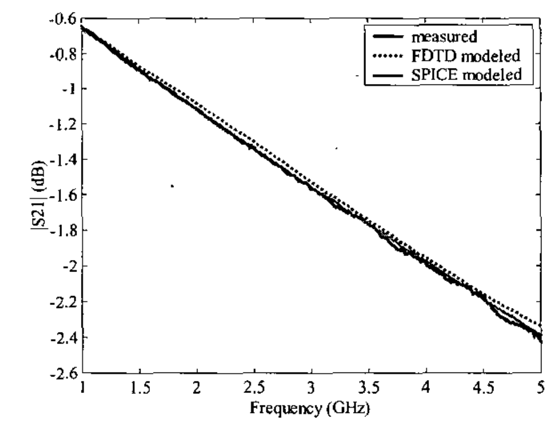

Figure 2. Comparison of FDTD, HSPICE and measurement for a single-ended stripline.

First, a single-ended stripline was modeled using FDTD to demonstrate the suitability of applying FDTD to signal integrity issues. This stripline was also modeled using HSPICE, and the corresponding measurements were performed. Figure 1 shows the geometry. The stripline was 8" long, 14 mils wide, and was located at 1/3 of the thickness of a three-layer board. The board was 30 mils thick, with the top and bottom layers being solid copper planes. The dielectric constant was approximately 3.45, yielding a 50 Ω characteristic impedance of the stripline. In the FDTD modeling, both dielectric loss and skin-effect

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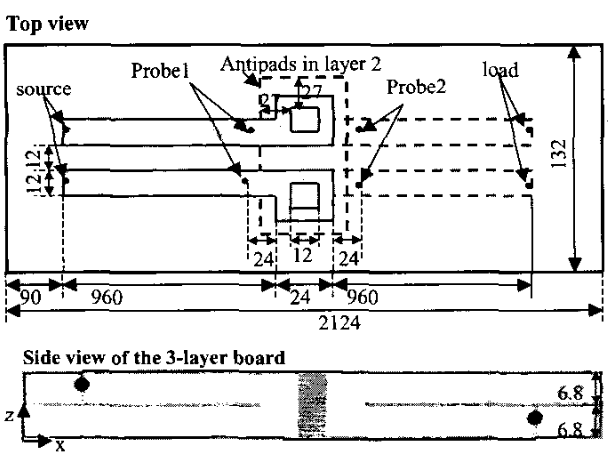
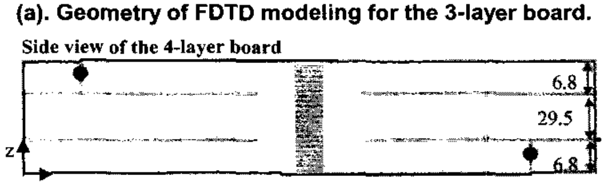
loss were taken into account. Figure 2 shows the measured, the FDTD modeled and the HSPICE modeled scattering parameters $|S_{21}|$ over a frequency range 1 ~ 5 GHz. The three curves nearly coincide, indicating the FDTD method is suitable to analyze signal integrity issues.

Next, via transitions in differential lines were studied using FDTD and equivalent circuit modeling. In order to focus on the behavior of the via transition, both the dielectric loss and the skin-effect loss were neglected in the modeling. Figure 3 (a) shows the geometry of the FDTD modeling for a 3-layer board with dimensions of 2124 mils × 1320 mils × 13.6 mils. Layers 1 and 3 are signal layers and layer 2 is a reference layer. A pair of microstrip differential lines of length of 960 mils was routed on layer 1, then transitioned to layer 3 through a pair of identical vias for another 960 mils, as shown in Figure 3 (a). The width of each line was 12 mils and the spacing between the lines from edge to edge was also 12 mils. The differential lines were 6.8 mils from the reference layer. For a substrate with a dielectric constant of 4.3, this design resulted in approximately 100 Ω differential impedance. Vias in real boards are produced by drills, resulting in circular cross sections. In this FDTD model, however, the cross section was approximated as a square for convenience. Each via hole was 12 mils × 12 mils and each via pad on layers 1 and 3 was 24 mils × 24 mils. The edge of the anti-pad on the reference layer was 27 mils from the closest wall of the via hole. All the dimensions were chosen to approximate those that could be found in a real board.

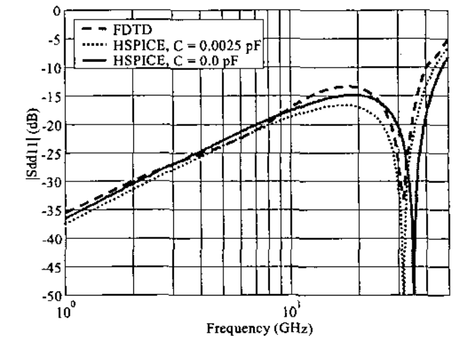


(a). Geometry of FDTD modeling for the 3-layer board.

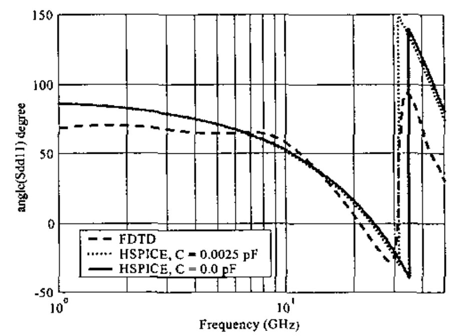


(b). Geometry of FDTD modeling for the 4-layer board.

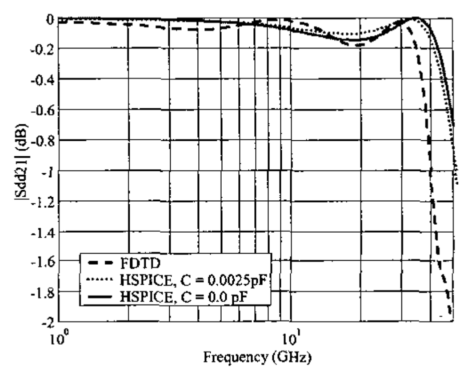
Figure 3. Geometry of FDTD modeling for the 3- and 4-layer cores. Units are in mils.



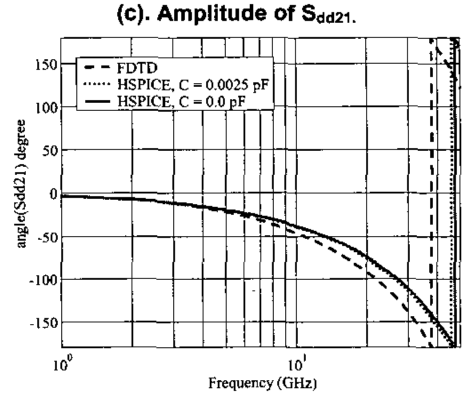
(a). Amplitude of S_{dd11}.



(b). Phase of S_{dd11}.



(c). Amplitude of S_{dd21}.



(d). Phase of S_{dd21}.

Figure 4. Comparison of differential-mode S-parameters for the via transition case with 3-layers.

The differential transmission lines were excited by two out-of-phase voltage sources at the source end. Each voltage source was a sinusoidally modulated Gaussian source with 50 Ω internal impedance. The load end was terminated with a π-network so that both the common-mode and the differential-mode impedances of the differential transmission line were matched. Voltage probes and current probes were placed at locations 1 and 2, and the mixed-mode S-parameters were calculated from 1 GHz to 50 GHz, as shown in Figure 4 (a) – (d).

EQUIVALENT CIRCUIT

In the differential transmission lines, the propagation velocity in the vertical part of the vias is approximately the same as the propagation velocity in the substrate [9]. This indicates that the two vias may be approximated as a transmission line buried in the substrate. Furthermore, the net current of the differential-mode should be zero for a balanced differential pair. Therefore, a transmission line model for the vertical part of the vias in a balanced differential transmission line is reasonable.

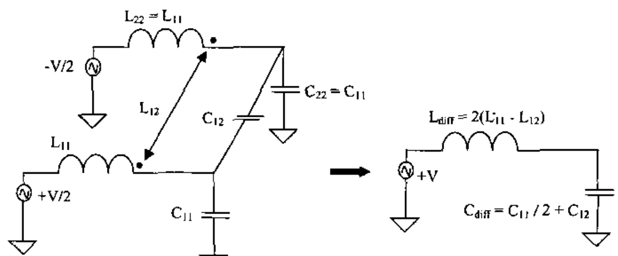
Table 1. Per-unit-length inductance and capacitance.

	T_1, T_5	T_2, T_4
L_{11} (nh/in)	15.38	11.213
L_{12} (nh/in)	6.052	3.968
C_{11} (pf/in)*	0.813	1.229
C_{12} (pf/in)	0.469	0.576
L_{diff} (nh/in)	18.65	14.5
C_{diff} (pf/in)	0.88	1.19
Z_{diff} (Ω)	146	110.4

* C_{11} is the self-capacitance to ground, not including C_{12}.

	T_3
L_0 (nh/in)	16.12
C_0 (pf/in)	1.814
Z_0 (Ω)	94.3

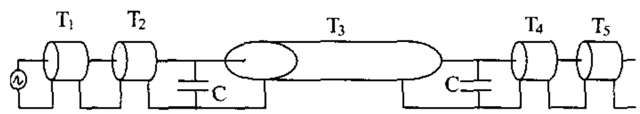
Figure 5 (a) shows a general schematic circuit of two coupled lossless transmission lines in terms of per-unit-length inductances and capacitances. For balanced differential transmission lines, the net current of the differential-mode in the ground is zero. Therefore, the circuit in Figure 5 (a) can be simplified to a circuit in Figure 5 (b), where $L_{diff} = 2(L_{11} - L_{12})$ and $C_{diff} = C_{11} / 2 + C_{12}$.



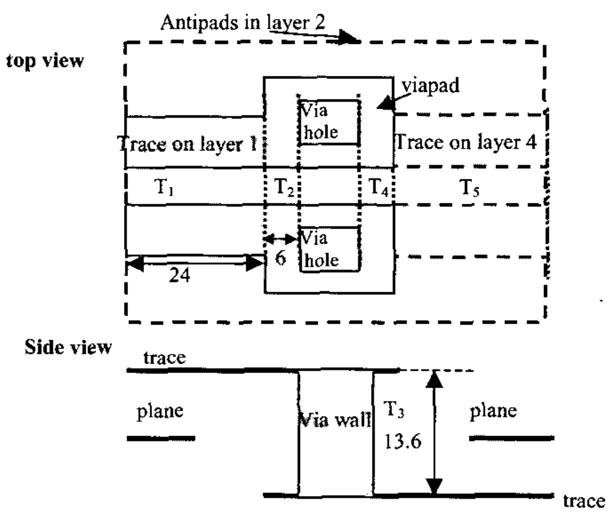
(a). Coupled transmission lines.

(b). Coupled transmission line operating in a balanced differential mode.

Figure 5. Equivalent circuit of coupled transmission lines operating in balanced differential mode. (C_{11} is the self-capacitance to ground, not including C_{12}.)



(a). Transmission line based equivalent circuit.



(b). Via geometry corresponding to transmission line segments.

Figure 6. Equivalent circuit and corresponding geometry. Units are in mils.

Figure 6 (a) shows the equivalent circuit of the via transition based on the balanced transmission line model. A close-up view of the trace, as well as the via and the pad geometry from locations 1 to 2 is shown in Figure 6 (b). The entire structure can be divided into five transmission line segments, with each segment corresponding to a different cross-section geometry. The per-unit-length inductances and capacitances were calculated using the 2 dimensional field solver, XFX, and the results are shown in Table 1. L_{diff} and C_{diff} were used for T_1, T_2, T_4, and T_5, and L_0 and C_0 were used for T_3. The lumped capacitance C in Figure 6 (a) was introduced in order to account for the parasitic capacitance between the differential pair at the via pads. The S-parameters of the equivalent circuit were calculated using HSPICE, and the results are shown in Figure 4. The gray curves correspond to C = 0 pF, and the dotted curves correspond to C = 0.0025pF. The S-parameters of the equivalent circuit model and the FDTD model agree within engineering accuracy in both amplitude and phase. The discrepancy of the $|S_{dd11}|$ curves is less than 5 dB over the frequency range of 1 GHz to 20 GHz in general, and the discrepancy of the $|S_{dd21}|$ curves is less than 0.1 dB over the frequency range of 1 GHz to 20 GHz in general.

In order to further study the equivalent circuit model for thicker boards, an FDTD simulation with a 4-layer via transition was performed. The geometry was similar to that of the 3-layer case, except that an additional reference layer was added, as shown in Figure 3 (b). A similar equivalent circuit with transmission-line segments was developed, and the resulting S-parameters are compared in Figure 7. Good agreement was obtained as well. The discrepancy of the $|S_{dd11}|$ curves is less than 3 dB over the frequency range of 1 GHz to 20 GHz, and the discrepancy of the $|S_{dd21}|$ curves is less than 0.1 dB over the frequency range of 1 GHz to 20 GHz in general.

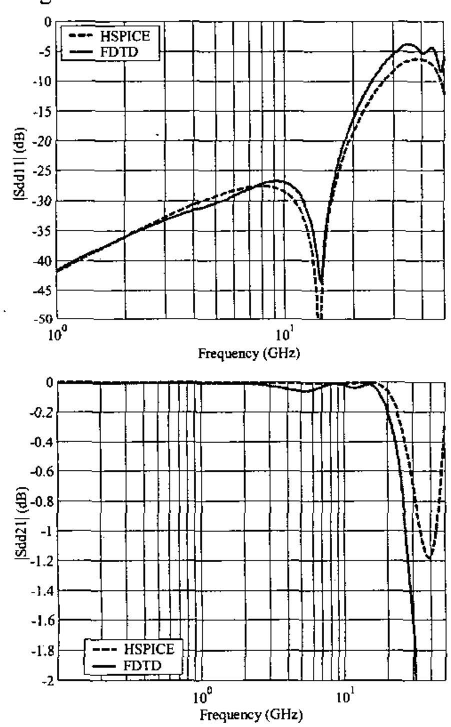


Figure 7. Comparison of differential-mode S-parameters for the 4-layer via transition case. (C = 0.008pF in HSPICE model.)

CONCLUSION

Differential S-parameters of vias in balanced differential transmission lines on PCBs have been calculated both with FDTD modeling and with HSPICE. The agreement between the HSPICE results and the FDTD results demonstrates that modeling vias in balanced differential lines as transmission line segments is promising as an engineering approach to estimating differential signal behavior. For the 100 Ω differential trace geometry examined, the discrepancy of $|S_{dd11}|$ between the HSPICE results and the full wave FDTD calculation was within 5 dB over the frequency range of 1 – 20 GHz, and $|S_{dd21}|$ was within 0.1 dB.

REFERENCES

[1] S. Meada, T. Kashiwa, and I. Fukai, "Full wave analysis of propagation characteristics of a through hole using the finite-difference time-domain method", *IEEE Transactions on Microwave Theory and Technology,* vol. 39, No. 12, December 1991.

[2] W. Becker, P. H. Harms, and R. Mittra, "Time-domain electromagnetic analysis of interconnects in a computer chip package", *IEEE Transactions on Microwave Theory and Technology,* vol. 40, No. 12, December 1992.

[3] P. Cherry and M. F. Iskander, "FDTD analysis of high frequency electronic interconnection effects", *IEEE Transactions on Microwave Theory and Technology,* vol. 43, No. 10, October 1995.

[4] H. H. M. Ghouz and E. EL-Sharawy, "An accurate equivalent circuit model of flip chip and via interconnects", *IEEE Transactions on Microwave Theory and Technology,* vol. 44, No. 12, December 1996.

[5] C. Hwang, S. Mao, R. Wu and C. Chen, "Partially prism-gridded FDTD analysis for layered structures of transversely curved boundary", *IEEE Transactions on Microwave Theory and Technology,* vol. 48, No. 3, March 2000.

[6] Q. Gu, E. Yang and M. A. Tassoudji, "Modeling and analysis of vias in multilayered integrated circuits", *IEEE Transactions on Microwave Theory and Technology,* vol. 41, No. 2, February 1993.

[7] Q. Gu, M. A. Tassoudji, S. Y. Poh, R. T. Shin and J. A. Kong, "Coupled noise analysis for adjacent vias in multilayered digital circuits ", *IEEE Transactions on Circuit and System – I: Fundamental Theory and Applications,* vol. 41, No. 12, December 1994.

[8] E. Laermans, J. D. Geest, D. D. Zutter, F. Olyslager, S. Sercu and D. Morlion, "Modeling differential via holes", *IEEE Transactions on Advanced Packaging,* vol. 24, No. 3, August 2001.

[9] C. Wang, J. Fan, J.L. Knighten, N. W. Smith, R. Alexander and J. L. Drewniak, "The effects of via transitions on differential signals", *Proc. 10th Topical Meeting Elect. Perform. Electro. Packag.,* Oct. 2001.