Transmuter: Bridging the Efficiency Gap using Memory and Dataflow Reconfiguration

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Subhankar Pal*, Siying Feng*, Dong-hyeon Park*, Sung Kim*, Aporva Amarnath*, Chi-Sheng Yang*, Xin He*, Jonathan Beaumont*, Kyle May*, Yan Xiong†, Kuba Kaszyk‡, John Magnus Morton‡, Jiawen Sun‡, Michael O'Boyle‡, Murray Cole‡, Chaitali Chakrabarti†, David Blaauw*, Hun-Seok Kim*, Trevor Mudge*, Ronald Dreslinski*

*University of Michigan, USA †Arizona State University, USA ‡University of Edinburgh, UK
Email: subh@umich.edu

ABSTRACT

With the end of Dennard scaling and Moore's law, it is becoming increasingly difficult to build hardware for emerging applications that meet power and performance targets, while remaining flexible and programmable for end users. This is particularly true for domains that have frequently changing algorithms and applications involving mixed sparse/dense data structures, such as those in machine learning and graph analytics. To overcome this, we present a flexible accelerator called `Transmuter`, in a novel effort to bridge the gap between General-Purpose Processors (GPPs) and Application-Specific Integrated Circuits (ASICs). `Transmuter` adapts to changing kernel characteristics, such as data reuse and control divergence, through the ability to reconfigure the on-chip *memory type*, *resource sharing* and *dataflow* at run-time within a short latency. This is facilitated by a fabric of light-weight cores connected to a network of reconfigurable caches and crossbars. `Transmuter` addresses a rapidly growing set of algorithms exhibiting dynamic data movement patterns, irregularity, and sparsity, while delivering GPU-like efficiencies for traditional dense applications. Finally, in order to support programmability and ease-of-adoption, we prototype a software stack composed of low-level runtime routines, and a high-level language library called `TransPy`, that cater to expert programmers and end-users, respectively.

Our evaluations with `Transmuter` demonstrate average throughput (energy-efficiency) improvements of 5.0× (18.4×) and 4.2× (4.0×) over a high-end CPU and GPU, respectively, across a diverse set of kernels predominant in graph analytics, scientific computing and machine learning. `Transmuter` achieves energy-efficiency gains averaging 3.4× and 2.0× over prior FPGA and CGRA implementations of the same kernels, while remaining on average within 9.3× of state-of-the-art ASICs.

CCS CONCEPTS

• **Computer systems organization → Reconfigurable computing**; *Data flow architectures*; Multicore architectures.

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KEYWORDS

Reconfigurable architectures, memory reconfiguration, dataflow reconfiguration, hardware acceleration, general-purpose acceleration

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1 INTRODUCTION

The past decade has seen a surge in emerging applications that are composed of multiple kernels[1] with varying data movement and reuse patterns, in domains such as machine learning (ML), and graph, image and signal processing. A growing number of such applications operate on compressed and *irregular* data structures [22, 51, 73], or on a combination of regular and irregular data [18, 21, 118]. While conventional CPU-GPU systems generally suffice for desktop computing [28], arenas such as high-performance computing (HPC) clusters and datacenters that demand higher performance for such applications require more specialized hardware; such systems are typically comprised of CPUs paired with GPUs and other domain-specific application-specific integrated circuit (ASIC) based accelerators [40, 50, 75], or field programmable gate arrays (FPGAs) [85, 96, 113]. coarse-grained reconfigurable architectures (CGRAs) have also been proposed as promising alternatives for achieving near-ASIC performance [82, 106]. These platforms have been historically bounded by three conflicting constraints: *programmability*, *algorithm-specificity*, and *performance/efficiency* [72], as is illustrated in Fig. 1. Owing to these trade-offs, there is currently no single architecture that is the most efficient across a diverse set of workloads [89].

Thus, the rising complexity of modern applications and need for efficient computing necessitate a solution that incorporates:

- **Flexibility.** Ability to cater to multiple applications, as well as emerging applications with changing algorithms, that operate on both regular and irregular data structures.

[1] This work refers to *kernels* as the building blocks of larger applications.

Platform	Programmability	Flexibility	Reconfig. Time
ASIC	Low/None	Low	N.A.
CGRA	Low-Medium	Medium	~1 µs - ~100 ns
FPGA	Medium	Medium-High	~1 ms - ~1 µs
GPU	High	High	N.A.
CPU	High	High	N.A.
Transformer	High	High	~10 ns

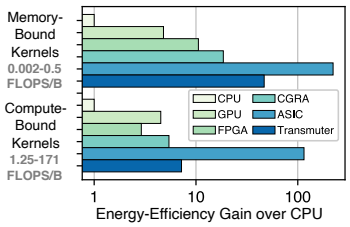

Figure 1: ***Left:*** **Transmuter compared to contemporary platforms in terms of programmability, hardware flexibility and reconfiguration overhead.** ***Right.*** **Energy-efficiency comparisons for kernels spanning a wide range of arithmetic intensities (FLOPS/B). Note that for ASICs and CGRAs, no single piece of hardware supports all kernels. Transmuter achieves 2.0× better average efficiency over state-of-the-art CGRAs, while retaining the programmability of GPPs.**

- **Reconfigurability.** Enabling near-ASIC efficiencies by morphing the hardware to specific kernel characteristics, for applications that are composed of multiple cascaded kernels.
- **Programmability.** Facilitating better adoption of non-GPP hardware by providing high-level software abstractions that are familiar to end-users and domain experts, and that mask the details of the underlying reconfigurable hardware.

To this end, we propose `Transmuter`, a reconfigurable accelerator that adapts to the nature of the kernel through a flexible fabric of light-weight cores, and reconfigurable memory and interconnect. Worker cores are grouped into tiles that are each orchestrated by a control core. All cores support a standard ISA, thus allowing the hardware to be fully *kernel-agnostic*. `Transmuter` overcomes inefficiencies in vector processors such as GPUs for irregular applications [87] by employing a multiple-instruction, multiple data (MIMD) / single-program, multiple data (SPMD) paradigm. On-chip buffers and scratchpad memories (SPMs) are used for low-cost scheduling, synchronization and fast core-to-core data transfers. The cores interface to a high-bandwidth memory (HBM) through a two-level hierarchy of reconfigurable caches and crossbars.

Our approach fundamentally differs from existing solutions that employ gate-level reconfigurability (FPGAs) and core/pipeline-level reconfigurability (most CGRAs) — we reconfigure the on-chip *memory type*, *resource sharing*, and *dataflow*, at a coarser granularity than contemporary CGRAs, while employing general-purpose cores as the compute units. Moreover, `Transmuter`'s reconfigurable hardware enables run-time reconfiguration within 10s of nanoseconds, faster than existing CGRA and FPGA solutions (Section 2.1).

We further integrate a prototype software stack to abstract the reconfigurable `Transmuter` hardware and support ease-of-adoption. The stack exposes two layers: (*i*) a `C++` intrinsics layer that compiles directly for the hardware using a commercial off-the-shelf (COTS) compiler, and (*ii*) a drop-in replacement for existing high-level language (HLL) libraries in Python, called `TransPy`, that exposes optimized `Transmuter` kernel implementations to an end-user. Libraries are written by experts using the `C++` intrinsics to access reconfigurable hardware elements. These libraries are then packaged and linked to existing HLL libraries, *e.g.* `NumPy`, `SciPy`, *etc.*

In summary, this paper makes the following contributions:

- **Proposes a general-purpose, reconfigurable accelerator design** composed of a sea of parallel cores interweaved with a flexible cache-crossbar hierarchy that supports fast run-time reconfiguration of the memory type, resource sharing and dataflow.
- **Demonstrates the flexibility of `Transmuter`** by mapping and analyzing six fundamental compute- and memory-bound kernels, that appear in multiple HPC and datacenter applications, onto three distinct `Transmuter` configurations.
- **Illustrates the significance of fast reconfiguration** by evaluating `Transmuter` on ten end-to-end applications (one in detail) spanning the domains of ML and graph/signal/image processing, that involve reconfiguration at kernel boundaries.
- **Proposes a prototyped compiler runtime and an HLL library called `TransPy`** that expose the `Transmuter` hardware to end-users through drop-in replacements for existing HLL libraries. The stack also comprises of `C++` intrinsics, which foster expert programmers to efficiently co-design new algorithms.
- **Evaluates the `Transmuter` hardware against existing platforms** with two proposed variants, namely `TransX1` and `TransX8`, that are each comparable in area to a high-end CPU and GPU.

In summary, `Transmuter` demonstrates average energy-efficiency gains of 18.4×, 4.0×, 3.4× and 2.0×, over a CPU, GPU, FPGAs and CGRAs respectively, and remains within 3.0×-32.1× of state-of-the-art ASICs. Fig. 1 (right) presents a summary of these comparisons.

2 BACKGROUND AND MOTIVATION

In this section, we provide a background on conventional computing platforms, and motivate the need for a reconfigurable design.

2.1 Contemporary Computing Platforms

ASICs have been the subject of extensive research in the dark silicon era due to their superior performance and efficiency [100]. However, ASICs compromise on generality by stripping away extraneous hardware, such as control logic, thus limiting their functionality to specific algorithms. An obvious solution is to design systems with multiple ASICs, but that leads to high under-utilization for applications with cascaded kernels. Moreover, fast-moving domains, such as ML, involve algorithms that evolve faster than the turnaround time to fabricate and test new ASICs, despite efforts on accelerating the design flow [20], thus subjecting them to near-term obsolescence [16, 43]. Finally, ASICs are generally non-programmable, barring a few that use sophisticated software frameworks [1].

FPGAs have been successful for fast prototyping and deployment by eliminating non-recurring costs through programmable blocks and routing fabric. Moreover, high-level synthesis tools have reduced the low-level programmability challenges associated with deploying efficient FPGA-based designs [7, 61, 62]. Despite that, power and cost overheads prohibit FPGAs from adaptation in scenarios that demand the acceleration of a diverse set of kernels [15, 94, 95]. Besides, reconfiguration overheads of FPGAs are in the ms-µs range, even for partial reconfiguration [111, 115, 116], thus impeding fast run-time reconfiguration across kernel boundaries. CGRAs overcome some of the energy and performance inefficiencies of FPGAs by reconfiguring at a coarser granularity. However, CGRA reconfiguration usually happens at compile-time, and the few that support run-time reconfiguration only support compute datapath reconfiguration [68], with overheads ranging from a few µs to 100s of

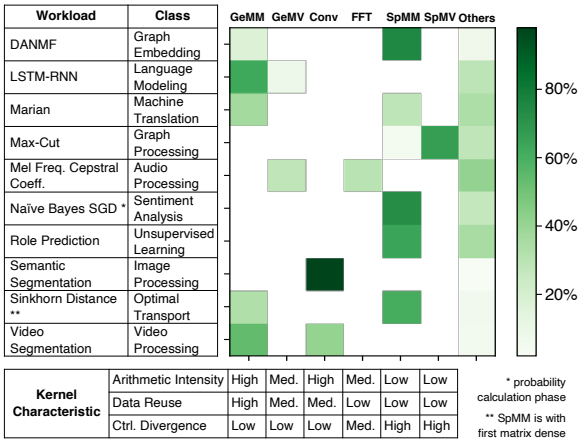

Figure 2: Fraction of execution time of kernels in applications spanning the domains of ML, signal processing, and graph analytics [14, 18, 21, 22, 51, 67, 73, 74, 78, 118] on a heterogeneous CPU-GPU platform. Some key characteristics, namely arithmetic intensity, data reuse and divergence, of each kernel are also listed.

ns [30, 33, 71]. Furthermore, many CGRAs require customized software stacks but have inadequate tool support, since they typically involve domain-specific languages (DSLs) and custom ISAs [114].

Finally, while CPUs and GPUs carry significant energy and area overheads compared to lean ASIC designs, they are the *de facto* choice for programmers as they provide high flexibility and abstracted programming semantics [12]. Although GPUs are efficient across many regular HPC applications, *i.e.* those exhibiting low control divergence, improving their effectiveness on irregular workloads remains a topic of research today [13, 84].

2.2 Taming the Diversity across Kernels

Many real-world workloads consist of multiple kernels that exhibit differing data access patterns and computational (arithmetic) intensities. In Fig. 2, we show the percentage execution times of key kernels that compose a set of ten workloads in the domains of ML, graph analytics, and signal/image/video processing. These workloads are derived from an ongoing multi-university program to study software-defined hardware.

The underlying kernels exhibit a wide range of arithmetic intensities, from $\frac{1}{1000}$ths to 100s of floating-point operations per byte, *i.e.* FLOPS/B (Fig. 1). We briefly introduce the kernels here. General (dense) matrix-matrix multiplication (GeMM) and matrix-vector multiplication (GeMV) are regular kernels in ML, data analytics and graphics [27, 32]. Convolution is a critical component in image processing [3] and convolutional neural networks [59]. Fast Fourier Transform (FFT) is widely used in speech and image processing for signal transformation [6, 79]. Sparse matrix-matrix multiplication (SpMM) is an important irregular kernel in graph analytics (part of GraphBLAS [54]), scientific computation [9, 24, 117], and problems involving big data with sparse connections [45, 93]. Another common sparse operation is sparse matrix-vector multiplication (SpMV), which is predominant in graph algorithms such as PageRank and Breadth-First Search [77], as well as ML-driven text analytics [5].

Takeaways. Fig. 2 illustrates that real-world applications exhibit diverse characteristics not only across domains, but also within an application. Thus, taming both the *inter-* and *intra*-application diversity efficiently in a *single piece of hardware* calls for an architecture capable of tailoring itself to the characteristics of each composing kernel.

2.3 Hardware Support for Disparate Patterns

Intuition dictates that the diverse characteristics of kernels would demand an equivalent diversity in hardware. We study the implications of some key hardware choices here.

2.3.1 On-Chip Memory Type: Cache vs. Scratchpad. Cache and scratchpad memory (SPM) are two well-known and extensively researched types of on-chip memory [8, 58, 110]. To explore their trade-offs, we performed experiments on a single-core system that employs these memories. We observed that:

- Workloads that exhibit low arithmetic intensity (*i.e.* are memory-intensive) but high spatial locality (contiguous memory accesses) perform better on a cache-based system.
- Workloads that are compute-intensive and have high traffic to disjoint memory locations favor an SPM *if* those addresses are known *a priori*. In this case, an SPM outperforms a cache because the software-managed SPM replacement policy supersedes any standard cache replacement policy.

Thus, caching is useful for kernels that exhibit high spatial locality and low-to-moderate FLOPS/byte, whereas SPMs are more efficient when the data is prone to thrashing, but is predictable and has sufficient reuse.

2.3.2 On-Chip Resource Sharing: Private vs. Shared. The performance of shared versus private on-chip resources is dependent on the working set sizes and overlaps across cores, *i.e.* inter-core data reuse. From our experiments we noted:

- When there is significant overlap between the threads' working sets, sharing leads to speedups exceeding 10× over privatization. This is owed to memory access coalescing and deduplication of data in the shared mode.
- When cores work on disjoint data, there is insignificant difference in performance with sharing over no-sharing, if the union of the threads' working sets fit on-chip.
- Regular kernels may exhibit strided accesses that can be hazardous for a shared multi-banked cache, due to conflicting accesses at the same bank. In this case, a private configuration delivers better performance.

2.3.3 Dataflow: Demand-Driven vs. Spatial. In this work, we refer to demand-driven dataflow as the dataflow used by GPPs, wherein cores use on-demand loads/stores to read/write data and communicate via shared memory. In contrast, spatial dataflow architectures (*e.g.* systolic arrays) are data-parallel designs consisting of multiple processing elements (PEs) with direct PE-to-PE channels. Each PE receives data from its neighbor(s), performs an operation, and passes the result to its next neighbor(s) [60]. If pipelined correctly, this form of data orchestration harnesses the largest degree of parallelism. However, it is harder to map and write efficient software for certain applications on spatial architectures [49].

Takeaways. The on-chip *memory type*, *resource sharing* and *dataflow* are three key hardware design choices that are each amenable to a different workload characteristic. This motivates the intuition that

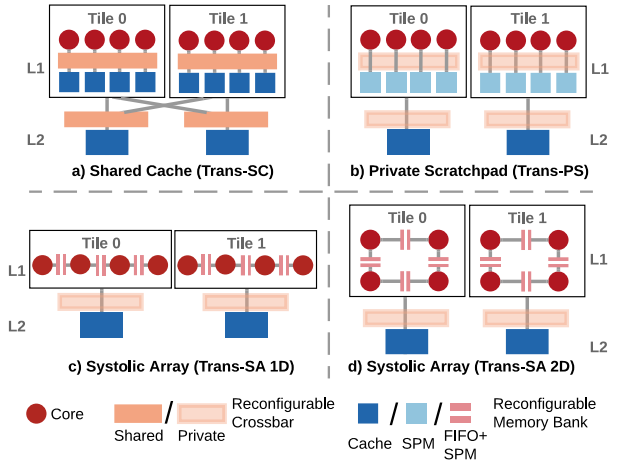

Figure 3: High-level Transmuter architecture showing the configurations evaluated in this work, namely a) Trans-SC (L1: shared cache, L2: shared cache), b) Trans-PS (L1: private SPM, L2: private cache), and c, d) Trans-SA (L1: systolic array, L2: private cache).

Table 1: Reconfigurable features at each level in Transmuter. In the "hybrid" memory mode, banks are split between caches and SPMs.

Dataflow	On-Chip Memory	Resource Sharing	# Modes
Demand-driven	Cache / SPM / Hybrid	Private / Shared	6
Spatial	FIFO + SPM	1D / 2D Systolic Sharing	2

an architecture that reconfigures between these designs can accelerate diverse workloads that exhibit a spectrum of characteristics.

3 HIGH-LEVEL ARCHITECTURE

The takeaways from the previous section are the fundamental design principles behind our proposed architecture, `Transmuter`. `Transmuter` is a tiled architecture composed of a massively parallel fabric of simple cores. It has a two-level hierarchy of crossbars and on-chip memories that allows for fast reconfiguration of the on-chip *memory type* (cache/scratchpad/FIFO), *resource sharing* (shared/private) and *dataflow* (demand-driven/spatial). The various modes of operation are listed in Tab. 1. The two levels of memory hierarchy, *i.e.* L1 and L2, supports 8 modes each. Furthermore, each `Transmuter` tile can be configured independently, however these tile-heterogeneous configurations are not evaluated in this work.

In this work, we identify three distinct `Transmuter` configurations to be well-suited for the evaluated kernels based on characterization studies on existing platforms (Sec. 2.2). These configurations are shown in Fig. 3 and discussed here.

- **Shared Cache (Trans-SC).** Trans-SC uses shared caches in the L1 and L2. The crossbars connect the cores to the L1 memory banks and the tiles to the L2 banks, respectively. This resembles a manycore system, but with a larger compute-to-cache ratio, and is efficient for regular accesses with high inter-core reuse.
- **Private Scratchpad (Trans-PS).** Trans-PS reconfigures the L1 cache banks into SPMs, while retaining the L2 as cache. The crossbars reconfigure to privatize the L1 (L2) SPMs to their corresponding cores (tiles). This configuration is suited for workloads with high intra-core but low inter-core reuse of data that is prone to cache-thrashing. The private L2 banks enable caching of secondary data, such as spill/fill variables.
- **Systolic Array (Trans-SA).** Trans-SA employs systolic connections between the cores within each tile, and is suited for highly data parallel applications where the work is relatively balanced between the cores. `Transmuter` supports both 1D and 2D systolic configurations. Note that the L2 is configured as a cache for the same reason as with Trans-PS.

We omit an exhaustive evaluation of all possible `Transmuter` configurations, given the space constraints of the paper. In the rest of the paper, we use the notation of $N_T \times N_G$ `Transmuter` to describe a system with N_T tiles and N_G worker cores per tile.

4 HARDWARE DESIGN

A full `Transmuter` system is shown in Fig. 4-a. A `Transmuter` chip consists of one or more `Transmuter` (TM) clusters interfaced to high-bandwidth memory (HBM) stack(s) in a 2.5D configuration, similar to modern GPUs [66]. A small host processor sits within the chip to enable low-latency reconfiguration. It is interfaced to a separate DRAM module and data transfer is orchestrated through DMA controllers (not shown) [31]. The host is responsible for executing serial/latency-critical kernels, while parallelizable kernels are dispatched to `Transmuter`.

4.1 General-Purpose Processing Element and local control processor

A general-purpose processing element (GPE) is a small processor with floating-point (FP) and load/store (LS) units that uses a standard ISA. Its small footprint enables `Transmuter` to incorporate many such GPEs within standard reticle sizes. The large number of GPEs coupled with miss status holding registers (MSHRs) in the cache hierarchy allows `Transmuter` to exploit memory-level parallelism (MLP) across the sea of cores. The GPEs operate in a MIMD/SPMD fashion, and thus have private instruction (I-) caches.

GPEs are grouped into tiles and are coordinated by a small control processor, the local control processor (LCP). Each LCP has private D- and ICaches that connect to the HBM interface. The LCP is primarily responsible for distributing work across GPEs, using either *static* (*e.g.* greedy) or *dynamic* scheduling (*e.g.* skipping GPEs with full queues), thus trading-off code complexity for work-balance.

4.2 Work and Status Queues

The LCP distributes work to the GPEs through private FIFO work queues. A GPE similarly publishes its status via private status queues that interface to the LCP (Fig. 4-c). The queues block when there are structural hazards, *i.e.* if a queue is empty and a consumer attempts a `POP`, the consumer is idled until a producer `PUSH`es to the queue, thus preventing wasted energy due to busy-waiting. This strategy is also used for systolic accesses, discussed next.

4.3 Reconfigurable Data Cache

`Transmuter` has two layers of multi-banked memories, called reconfigurable data caches, *i.e.* R-DCaches (Fig. 4 – b, c). Each R-DCache bank is a standard cache module with enhancements to support the following modes of operation:

- **CACHE.** Each bank is accessed as a non-blocking, write-back, write-no-allocate cache with a least-recently used replacement

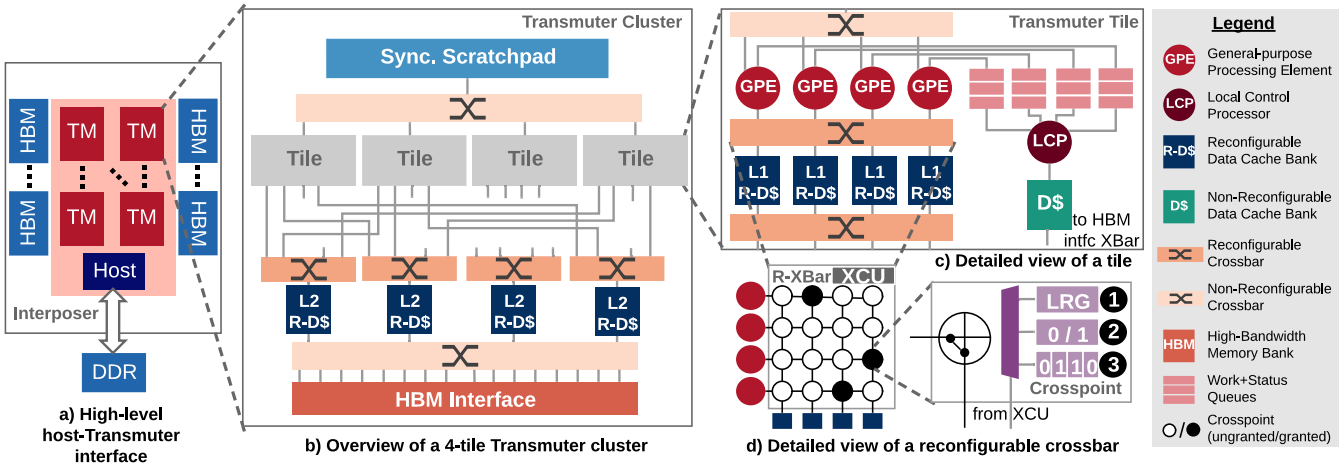

Figure 4: a) High-level overview of a host-Transmuter system. b) Transmuter architecture showing 4 tiles and 4 L2 R-DCache banks, along with L2 R-XBars, the synchronization SPM and interface to off-chip memory. Some L2 R-XBar input connections are omitted for clarity. c) View of a single tile, showing 4 GPEs and the work/status queues interface. Arbiters, instruction paths and ICaches are not shown. d) Microarchitecture of an R-XBar, with the circled numbers indicating the mode of operation: ①: ARBITRATE, ②: TRANSPARENT, ③: ROTATE.

policy. The banks are interleaved at a set-granularity, and a cache-line physically resides in one bank. Additionally, this mode uses a simple stride prefetcher to boost performance for regular kernels.
- **SPM.** The tag array, set-index logic, prefetcher and MSHRs are powered off and the bank is accessed as a scratchpad.
- **FIFO+SPM.** A partition of the bank is configured as SPM, while the remainder are accessed as FIFO queues (Fig. 5 – left), using a set of head/tail pointers. The queue depth can be reconfigured using memory-mapped registers. The low-level abstractions for accessing the FIFOs are shown in Fig. 5 (right). This mode is used to implement spatial dataflow in Trans-SA (Fig. 3).

4.4 Reconfigurable Crossbar

A multicasting $N_{src} \times N_{dst}$ crossbar creates one-to-one or one-to-many connections between N_{src} source and N_{dst} destination ports. `Transmuter` employs swizzle-switch network (SSN)-based crossbars that support multicasting [48, 99]. These and other work [2] have shown that crossbars designs can scale better, up to radix-64, compared to other on-chip networks. We augment the crossbar design with a crosspoint control unit (XCU) that enables reconfiguration by programming the crosspoints. A block diagram of a reconfigurable crossbar (R-XBar) is shown in Fig. 4-d. The R-XBars support the following modes of operation:

- **ARBITRATE.** Any source port can access any destination port, and contended accesses to the same port get serialized. Arbitration is done in a single cycle using a least-recently granted policy [99], while the serialization latency varies between 0 and $(N_{src} - 1)$ cycles. This mode is used in Trans-SC.
- **TRANSPARENT.** A requester can only access its corresponding resource, *i.e.* the crosspoints within the crossbar are set to 0 or 1 (Fig. 4-d). Thus, the R-XBar is transparent and incurs *no* arbitration or serialization delay in this mode. Trans-PS (in L1 and L2) and Trans-SA (in L2) employ TRANSPARENT R-XBars.
- **ROTATE.** The R-XBar cycles through a set of one-to-one port connections programmed into the crosspoints. This mode also has no crossbar arbitration cost. Fig. 6 illustrates how port multiplexing is used to emulate spatial dataflow in a 1D systolic array configuration (Trans-SA).

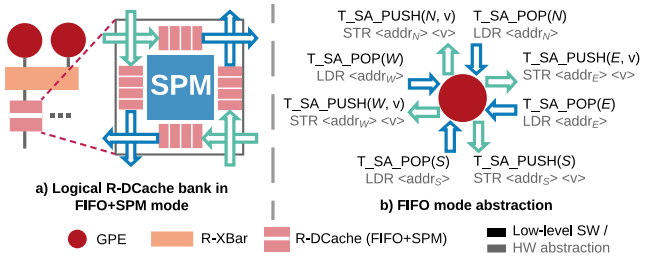

Figure 5: a) Logical view of an R-DCache bank in FIFO+SPM mode, showing 4 FIFO partitions, one for each direction in 2D. b) Loads and stores to special addresses corresponding to each direction are mapped to POP and PUSH calls, respectively, into the FIFOs.

There are two L1 R-XBars within a tile (Fig. 4-c). The upper R-XBar enables GPEs to access the L1 R-DCache, and the lower R-XBar amplifies on-chip bandwidth between the L1 and L2.

4.5 Synchronization

`Transmuter` implements synchronization and enforces happens-before ordering using two approaches. The first is *implicit*, in the form of work/status/R-DCache queue accesses that block when the queue is empty or full. Second, it also supports *explicit* synchronization through a global synchronization SPM for programs that require mutexes, condition variables, barriers, and semaphores. For instance, say that GPEs `0` and `1` are to execute a critical section (CS) in a program. With explicit synchronization, the programmer can instantiate a mutex in the synchronization SPM and protect the CS with it. The same can also be achieved through implicit synchronization, with the following sequence of events: ① both GPEs ← LCP, ② LCP → GPE`0`, ③ GPE`0` executes the CS, ④ GPE`0` → LCP, ⑤ LCP → GPE`1`, ⑥ GPE`1` executes the CS, ⑦ GPE`1` → LCP, where ← denotes `POP`-from and → is a `PUSH`-to the work or status queue.

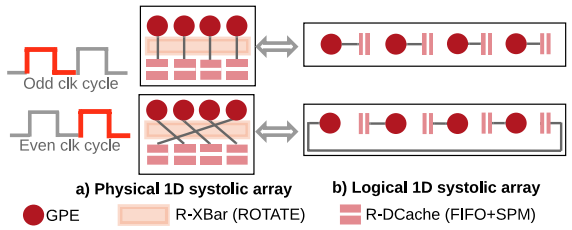

Figure 6: a) Physical and b) logical views of 1D systolic array connections within a Transmuter tile. Spatial dataflow is achieved by the R-XBar rotating between the two port-connection patterns.

Compared to traditional hardware coherence, these techniques reduce power through lower on-chip traffic [53, 87]. The synchronization SPM is interfaced to the LCPs and GPEs through a low-throughput two-level arbiter tree, as accesses to this SPM were not bottleneck for any of the evaluated workloads.

4.6 Miscellaneous Reconfiguration Support

The GPE LS unit is augmented with logic to route packets to the work/status queue, synchronization SPM, and the L1 or L2 R-DCache, based on a set of base/bound registers. Reconfiguration changes the active base/bound registers, without external memory traffic. LCPs include similar logic but do not have access to the L1 or L2. Lastly, the system enables power-gating individual blocks, *i.e.* cores, R-XBars, R-DCaches, based on reconfiguration messages. This is used to boost energy-efficiency for memory-bound kernels.

4.7 Reconfiguration Overhead

`Transmuter` can self-reconfigure at run-time (initiated by an LCP) if the target configuration is known *a priori*. Reconfiguration can also be initiated by the host using a command packet with relevant metadata. The programming interface used to initiate this is discussed in Sec. 6. Each step of the hardware reconfiguration happens in parallel and is outlined below.

- **GPE.** Upon receiving the reconfiguration command, GPEs switch the base/bound registers that their LS units are connected to (Sec. 4.6) in a single cycle.
- **R-XBar.** ARBITRATE ↔ TRANSPARENT reconfiguration entails a 1-cycle latency, as it only switches MUXes in the R-XBar (Fig. 4-d). The ROTATE mode uses set/unset patterns, which requires a serial transfer of bit vectors from on-chip registers (*e.g.* a 64×64 design incurs a 6-cycle latency[2]).
- **R-DCache.** Switching from CACHE to SPM mode involves a 1-cycle toggle of the scratchpad controller. The FIFO+SPM mode involves programming the head and tail pointer for each logical FIFO queue, which are transferred from control registers (4 cycles for 4 FIFO partitions).

Thus, the net reconfiguration time, accounting for buffering delays, amounts to *~10 cycles*, which is faster than FPGAs and many CGRAs (Sec. 2.1). For host-initiated reconfiguration, overheads associated with host-to-`Transmuter` communication leads to a net reconfiguration time of few 10s of cycles. We limit our discussions to self-reconfiguration in this work. Since `Transmuter` does not implement hardware coherence, switching between certain `Transmuter` configurations entails cache flushes from L1 to L2, from L2 to HBM, or both. The levels that use the SPM or FIFO+SPM mode do not need flushing. Furthermore, our write-no-allocate caches circumvent flushing for streaming workloads that write output data only once. Even when cache flushes are inevitable, the overhead is small (<1% of execution time) for the evaluated kernels in Sec. 8.

[2]Latency (in cycles) = ceil($N_{\text{rotate\_patterns}} \times N_{\text{dst}} \times \log_2(N_{\text{src}})$ / xfer_width)

5 KERNEL MAPPING

`Transmuter` is built using COTS cores that lend the architecture to be kernel-agnostic. Here, we present our mappings of the fundamental kernels in Sec. 2 on the selected `Transmuter` configurations. Code snippets for three of our implementations are listed in Appendix C. Additional kernels in the domain of linear algebra have been mapped and evaluated on a preliminary version of `Transmuter` for different resource sharing configurations [101].

We note that while executing memory-bound kernels, `Transmuter` powers-down resources within a tile to conserve energy.

5.1 Dense Matrix Multiplication and Convolution

`GeMM`. `GeMM` is a regular kernel that produces $O(N^3)$ FLOPS for $O(N^2)$ fetches and exhibits very high reuse [38]. It also presents contiguous accesses, thus showing amenability to a shared memory based architecture. Our implementation of `GeMM` on Trans-SC uses a common blocking optimization [69]. We similarly implement `GeMM` on Trans-PS but with the blocked partial results stored in the private L1 SPMs. Naturally, Trans-PS misses the opportunity for data sharing. For Trans-SA, the GPEs execute `GeMM` in a systolic fashion with the rows of A streamed through the L2 cache, and the columns of B loaded from the L1 SPM.

`GeMV`. `GeMV` is a memory-bound kernel that involves lower FLOPS/B — $O(N^2)$ FLOPS for $O(N^2)$ fetches — than `GeMM`, but still involves contiguous memory accesses [29]. The Trans-SC and Trans-PS implementations are similar to those for `GeMM`, but blocking is not implemented due to lower data reuse. On Trans-SA, the vector is streamed into each GPE through the L2 cache, while the matrix elements are fetched from the L1 SPM. Each GPE performs a MAC, and passes the partial sum and input matrix values to its neighbors. We avoid network deadlock in our `GeMM` and `GeMV` Trans-SA implementations by reconfiguring the FIFO depth of the L1 R-DCache (Sec. 4.3) to allow for sufficient buffering.

`Conv`. `Conv` in 2D produces $(2 \cdot F^2 \cdot N^2 \cdot IC \cdot OC)/S$ FLOPS, for an $F \times F$ filter convolving with stride S over an $N \times N$ image, with IC input and OC output channels. The filter is reused while computing one output channel, and across multiple images. Input reuse is limited to $O(F \cdot OC)$, for $S<F$. On Trans-SC, we assign each GPE to compute the output of multiple rows, to maximize the filter reuse across GPEs. For Trans-PS and Trans-SA, we statically partition each image into $B \times B \times IC$ sub-blocks, such that the input block and filter fit in the private L1 SPM. Each block is then mapped to a GPE for Trans-PS, and to a set of F adjacent GPEs of a 1D systolic array for Trans-SA using a row stationary approach similar to [17].

5.2 Fast Fourier Transform

`FFT`. `FFT` in 1D computes an N-point discrete Fourier transform in $\log(N)$ sequential *stages*. Each stage consists of $N/2$ *butterfly* operations. `FFT` applications often operate on streaming input samples,

and thus are amenable to spatial dataflow architectures [25, 46]. Our Trans-SA mapping is similar to pipelined systolic ASICs; each stage is assigned to a single GPE, and each GPE immediately pushes its outputs to its neighbor. The butterflies in each stage are computed greedily. To reduce storage and increase parallelism, Trans-SA uses run-time twiddle coefficient generation when the transform size is too large for on-chip memory, *e.g.* >256 for 2×8, with the trade-off of making the problem compute-bound. On Trans-SC, the butterfly operations are distributed evenly among GPEs to compute a stage in parallel. LCPs assign inputs and collect outputs from GPEs. All cores synchronize after each stage. For Trans-PS, the same scheduling is used and partial results are stored in the L1 SPM.

5.3 Sparse Matrix Multiplication

SpMM. SpMM is a memory-bound kernel with low FLOPS that decrease with increasing sparsity, *e.g.* $\sim 2N^3 r_M^2$, for uniform-random $N \times N$ matrices with density r_M. Furthermore, sparse storage formats lead to indirection and thus irregular memory accesses [65, 87]. We implement SpMM in Trans-SC using a prior outer product approach [87]. In the *multiply phase* of the algorithm, the GPEs multiply a column of A with the corresponding row of B, such that the row elements are reused in the L1 cache. In the *merge phase*, a GPE merges all the partial products corresponding to one row of C. Each GPE maintains a private list of sorted partial results and fills it with data fetched from off-chip. Trans-PS operates similarly, but with the sorting list placed in private L1 SPM, given that SPMs are a better fit for operations on disjoint memory chunks. Lastly, SpMM in Trans-SA is implemented following a recent work that uses sparse packing [41]. Both the columns of A and rows of B are packed in memory. The computation is equally split across the tiles.

SpMV. SpMV, similar to SpMM, is bandwidth-bound and produces low FLOPS ($\sim 2N^2 r_M r_v$ for a uniformly random $N \times N$ matrix with density r_M, and vector with density r_v). We exploit the low memory traffic in the outer product algorithm for sparse vectors, mapping it to Trans-SC and Trans-PS. The GPEs and LCPs collaborate to merge the partial product columns in a tree fashion, with LCP `0` writing out the final elements to the HBM. SpMV on 1D Trans-SA is implemented using inner product on a packed sparse matrix as described in [41]. The packing algorithm packs 64 rows as a slice, and assigns one slice to each 1×4 sub-tile within a tile. Each GPE loads the input vector elements into SPM, fetches the matrix element and performs MAC operations, with the partial results being streamed to its neighbor within the sub-tile.

Finally, for both SpMM and SpMV, we use dynamic scheduling for work distribution to the GPEs (Sec. 4.1), in order to exploit the amenability of sparse workloads to SPMD architectures [87].

6 PROTOTYPE SOFTWARE STACK

We implement a software stack for `Transmuter` in order to support good programmability and ease-of-adoption of our solution. The software stack has several components: a high-level Python API, and lower-level C++ APIs for the host, LCPs and GPEs. An outline of the software stack and a working `Transmuter` code example are shown in Fig. 7.

The highest level API, called `TransPy`, is a drop-in replacement for the well-known high-performance Python library `NumPy`, *i.e.*

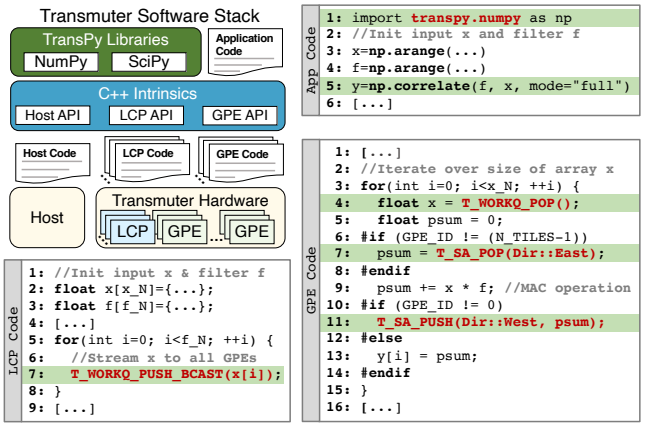

Figure 7: Transmuter software stack. Application code is written using Python and invokes library code for the host, LCPs and GPEs. The implementations are written by experts using our C++ intrinsics library. Also shown is an example of a correlation kernel on Trans-SA (host library code not shown). The end-user writes standard `NumPy` code and changes only the import package to `transpy.numpy` (App:L1). Upon encountering the library call (App:L5), the host performs data transfers and starts execution on Transmuter. The LCP broadcasts the vector `x` to all GPEs (LCP:L7). Each GPE pops the value (GPE:L4), performs a MAC using its filter value (`f`) and east neighbor's partial sum (GPE:L7), and sends its partial sum westward (GPE:L11). The last GPE stores the result into HBM. The host returns control to the application after copying back the result vector `y`.

the `TransPy` API *exactly* mirrors that of `NumPy`. In the code example in Fig. 7, note that only one change is needed to convert the `NumPy` program to `TransPy`. The `np.correlate` function is trapped in `TransPy`, dispatched to the `Transmuter` host layer, and a precompiled kernel library is invoked. We use `pybind11` [47] as the abstraction layer between Python and `C++`. `TransPy` also contains drop-in replacements for `SciPy`, `PyTorch`, `NetworkX`, and other libraries used in scientific computing, ML, graph analytics, *etc.*

`TransPy` invokes kernels that are implemented by library writers and expert programmers, with the aid of the `C++` intrinsics layer. A `Transmuter` SPMD kernel implementation consists of three programs, one each for the host, LCP and GPE. The host code is written in the style of OpenCL [104], handling data transfers to and from `Transmuter`, launching computation, initializing reconfigurable parameters (*e.g.* R-DCache FIFO depth), and triggering reconfiguration if needed. On the `Transmuter`-side, notable API methods include those associated with the queue interface, for accessing SPMs and FIFOs, triggering cache flushes, and reconfiguration. Synchronization is handled using intrinsics that wrap around POSIX threads functions [80]. These calls allow for synchronization at different granularities, such as globally, within tiles, and across LCPs. A set of these `C++` intrinsics is listed in Appendix A, and the code example in Fig. 7 reflects the use of some of these calls.

Thus, the `Transmuter` software stack is designed to enable efficient use of the `Transmuter` hardware by end-users, *without* the burden of reconfiguration and other architectural considerations. At the same time, the `C++` layer allows for expert programmers to write their own implementations, such as sophisticated heterogeneous implementations that partition the work between the host CPU and `Transmuter`. As an alternative to writing hand-tuned

Table 2: Microarchitectural parameters of Transmuter gem5 model.

Module	Microarchitectural Parameters
GPE/LCP	1-issue, 4-stage, in-order (MinorCPU) core @ 1.0 GHz, tournament branch predictor, FUs: 2 integer (3 cycles), 1 integer multiply (3 cycles), 1 integer divide (9 cycles, non-pipelined), 1 FP (3 cycles), 1 LS (1 cycle)
Work/Status Queue	4 B, 4-entry FIFO buffer between each GPE and LCP within a tile, blocks loads if empty and stores if full
R-DCache (per bank)	CACHE: 4 kB, 4-way set-associative, 1-ported, non-coherent cache with 8 MSHRs and 64 B block size, stride prefetcher of degree 2, word-granular (L1) / cacheline-granular (L2) SPM: 4 kB, 1-ported, physically-addressed, word-granular FIFO+SPM: 4 kB, 1-ported, physically-addressed, 32-bit head and tail pointer registers
R-XBar	$N_{src} \times N_{dst}$ non-coherent crossbar with 1-cycle response ARBITRATE: 1-cycle arbitration latency, 0 to (N_{src}-1) serialization latency depending upon number of conflicts TRANSPARENT: no arbitration, direct access ROTATE: switch port config. at programmable intervals Width: 32 address + 32 (L1) / 128 (L2) data bits
GPE/LCP ICache	4 kB, 4-way set-associative, 1-ported, non-coherent cache with 8 MSHRs and 64 B block size
Sync. SPM	4 kB, 1-ported, physically-addressed scratchpad
Main Memory	1 HBM2 stack: 16 64-bit pseudo-channels, each @ 8000 MB/s, 80-150 ns average access latency

Table 3: Specifications of baseline platforms and libraries evaluated.

Platform	Specifications	Library Name and Version
CPU	Intel i7-6700K, 4 cores/8 threads at 4.0-4.2 GHz, 16 GB DDR3 memory @ 34.1 GB/s, AVX2, SSE4.2, 122 mm^2 (14 nm)	MKL 2018.3.222 (GeMM/GeMV/SpMM/SpMV), DNNL 1.1.0 (Conv), FFTW 3.0 (FFT)
GPU	NVIDIA Tesla V100, 5120 CUDA cores at 1.25 GHz, 16 GB HBM2 memory at 900 GB/s, 815 mm^2 (12 nm)	cuBLAS v10 (GeMM/GeMV), cuDNN v7.6.5 (Conv), cuFFT v10.0 (FFT), CUSP v0.5.1 (SpMM), cuSPARSE v8.0 (SpMV)

kernels for Transmuter, we are actively working on prototyping a compiler to automatically generate optimized C++-level library code for Transmuter based on the Lift data-parallel language [103], the details of which are left for a future work.

7 EXPERIMENTAL METHODOLOGY

This section describes the methodology used to derive performance, power and area estimates for Transmuter. Tab. 2 shows the parameters used for modeling Transmuter. We compare Transmuter with a high-end Intel Core i7 CPU and NVIDIA Tesla V100 GPU running optimized commercial libraries. The baseline specifications and libraries are listed in Tab. 3. For fair comparisons, we evaluate two different Transmuter designs, namely **TransX1** and **TransX8**, that are each comparable in area to the CPU and GPU, respectively. TransX1 has a single 64×64 Transmuter cluster and TransX8 employs 8 such clusters. Both designs have one HBM2 stack/cluster to provide sufficient bandwidth and saturate all GPEs in the cluster.

7.1 Performance Models

We used the gem5 simulator [10, 11] to model the Transmuter hardware. We modeled the timing for GPEs and LCPs after an in-order Arm Cortex-M4F, and cache and crossbar latencies based on a prior chip prototype that uses SSN crossbars [88, 90]. Data transfer/set-up times are excluded for all platforms. Throughput is reported in FLOPS/s and only accounts for useful (algorithmic) FLOPS.

The resource requirement for simulations using this detailed gem5 model is only tractable for Transmuter systems up to 8×16. For larger systems, we substitute the gem5 cores with trace replay engines while retaining the gem5 model for the rest of the system. Offline traces are generated on a native machine and streamed through these engines. This allows us to simulate systems up to one 64×64 cluster. On average, across the evaluated kernels, the trace-driven model is pessimistic to 4.5% of the execution-driven model. For a multi-cluster system, we use analytical models from gem5-derived bandwidth and throughput scaling data (Sec. 8.2).

We implemented each kernel in C++ and hand-optimized it for each Transmuter configuration using the intrinsics discussed in Sec. 6. Compilation was done using an Arm GNU compiler with the -O2 flag. All experiments used single-precision FP arithmetic.

7.2 Power and Area Models

We designed RTL models for Transmuter hardware blocks and synthesized them. The GPEs and LCPs are modeled as Arm Cortex-M4F cores. For the R-XBar, we use the SSN design proposed in [99], augmented with an XCU. The R-DCaches are cache modules enhanced with SPM and FIFO control logic.

The crossbar and core power models are based on RTL synthesis reports and the Arm Cortex-M4F specification document. The R-XBar power model is calibrated against the data reported in [99]. For the caches and synchronization SPM, we used CACTI 7.0 [81] to estimate the dynamic energy and leakage power. We further verified our power estimate for SpMM on Transmuter against a prior SpMM ASIC prototype [88], and obtained a pessimistic deviation of 17% after accounting for the architectural differences. Finally, the area model uses estimates from synthesized Transmuter blocks.

We note that this work considers only the chip power on all platforms, for fair comparisons. We used standard profiling tools for the CPU and GPU, namely nvprof and RAPL. For the GPU, we estimated the HBM power based on per-access energy [86] and measured memory bandwidth, and subtracted it out. The power is scaled for iso-technology comparisons using quadratic scaling.

8 EVALUATION

We evaluate the Trans-SC, Trans-PS and Trans-SA configurations on the kernels in Sec. 5. We then compare the best-performing Transmuter to the CPU and GPU, and deep-dive into the evaluation of an application that exercises rapid reconfiguration. Lastly, we show comparisons with prior platforms and power/area analysis.

8.1 Performance with Different Configurations

Fig. 8 presents relative comparisons between Trans-SC, Trans-PS and Trans-SA in terms of performance. This analysis was done on a small 2×8 system to stress the hardware. The results show that the *best performing* Transmuter *configuration is kernel-dependent*, and in certain cases *also input-dependent*. Fig. 9 shows the cycle breakdowns and the work imbalance across GPEs.

For GeMM, Trans-SC achieves high L1 hit rates (>99%), as efficient blocking leads to good data reuse. Trans-PS suffers from capacity misses due to lack of sharing, noted from the large fraction of L2 misses. Further, Trans-SC performs consistently better than Trans-SA, as it does not incur the overhead of manually fetching data into the L1 SPM. For GeMV, Trans-SC and Trans-PS behave the same as GeMM. However, Trans-SA experiences thrashing (increasing with matrix size) in the private L2. For Conv, as with GeMM/GeMV, Trans-SC performs the best due to a regular access pattern with sufficient filter and input reuse. Across these kernels, stride prefetching in Trans-SC is sufficient to capture the regular access patterns.

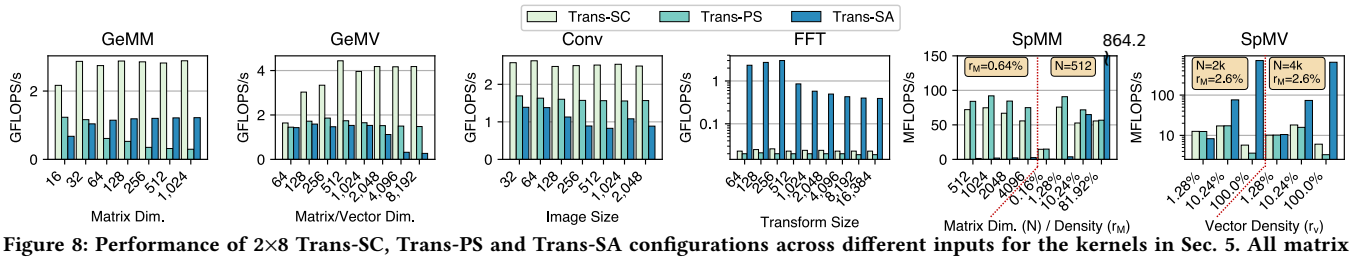

Figure 8: Performance of 2×8 Trans-SC, Trans-PS and Trans-SA configurations across different inputs for the kernels in Sec. 5. All matrix operations are performed on square matrices without loss of generality. Conv uses 3×3 filters, 2 input/output channels, and a batch size of 2.

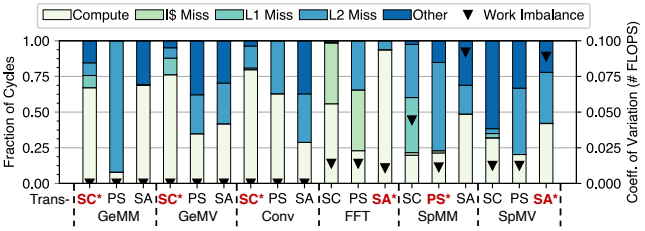

Figure 9: Cycle breakdown for the kernels in Sec. 5. * (red) indicates the best-performing configuration. "Other" comprises of stalls due to synchronization and bank conflicts. ▼: work imbalance across GPEs (σ/μ of # FLOPS). Inputs are: 1k (GeMM), 8k (GeMV), 2k (Conv), 16k (FFT), 4096, 0.64% (SpMM), 4k, 2.6%, dense vector (SpMV).

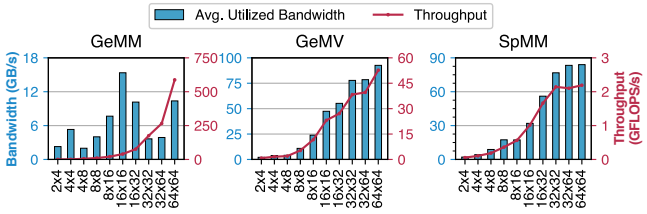

Figure 10: Effect of scaling tiles and GPEs per tile on performance and memory bandwidth for GeMM (Trans-SC), GeMV (Trans-SC) and SpMM (Trans-PS). Inputs are: 1k (GeMM), 8k (GeMV), 4096, 0.64% (SpMM).

For FFT, Trans-SA achieves significantly higher throughput because it benefits from the streaming inputs and exploits better data reuse, evidenced by ~10× less memory bandwidth usage compared to Trans-SC/Trans-PS. Inter-GPE synchronization and coherence handling at the end of each stage limit the performance for Trans-SC/Trans-PS. In addition, the control flow in the non-systolic code is branchy and contributes to expensive ICache misses. Trans-SA performs better for sizes <512 compared to other sizes, as the twiddle coefficients are loaded from on-chip rather than being computed.

For SpMM, the multiply phase of outer product is better suited to Trans-SC as the second input matrix rows are shared. The merge phase is amenable to Trans-PS since the private SPMs overcome the high thrashing that Trans-SC experiences while merging multiple disjoint lists. Trans-SA dominates for densities >~11%, however it performs poorly in comparison to outer product for highly-sparse matrices. Although ~50% of the time is spent on compute operations (Fig. 9), most of these are wasted on fetched data that are discarded after failed index matches. For SpMV, performance depends on the input matrix size, dimensions, as well as the vector density. Notably, Trans-SA benefits through the spatial dataflow for SpMV but not for SpMM, because the SpMV implementation treats the vector as dense, and thus can stream-in the vector elements efficiently into the GPE arrays. At sufficiently high vector sparsities, outer product on Trans-SC/Trans-PS outperforms Trans-SA by avoiding fetches of zero-elements. For higher densities, they suffer from the overhead of performing mergesort that involves frequent GPE-LCP synchronization, and serialization at LCP 0.

Takeaways. Demand-driven dataflow with shared caching outperforms other configurations for GeMM, GeMV and Conv due to sufficient data sharing and reuse. Streaming kernels such as FFT and SpMV (with dense vectors) are amenable to spatial dataflow. SpMM and high-sparsity SpMV show amenability to private scratchpad or shared cache depending on the input size and sparsity, with the systolic mode outperforming only for very high densities.

8.2 Throughput and Bandwidth Analysis

We investigate here the impact of scaling the number of tiles (N_T) and GPEs per tile (N_G) for an N_T×N_G Transmuter. Fig. 10 illustrates the scaling of Transmuter for GeMM, GeMV and SpMM. GeMM shows near-linear performance scaling with the GPE-count. The bandwidth utilization, however, does not follow the same trend as it is dependent on the data access pattern at the shared L2 R-DCache that influences the L2 hit-rate. GeMV exhibits increased bank conflicts in the L1 shared cache upon scaling up N_G, *e.g.* from 32×32 to 32×64. Thus, the performance scaling shows diminishing returns with increasing N_G, but scales well with increasing N_T. SpMM performance scales well until the bandwidth utilization is close to peak, at which point bank conflicts at the HBM controllers restrict further gains. SpMV follows the trend of GeMV, while FFT and Conv, show near-linear scaling with increasing system size (not shown).

We also discuss some takeaways from our cache bandwidth analysis for the best-performing Transmuter configuration. GeMM exhibits a high L1 utilization (20.4%) but low L2 utilization (2.7%), as most of the accesses are filtered by the L1. In contrast, SpMM and SpMV in Trans-PS and Trans-SA modes, respectively, have higher L2 utilizations of 68.5-90.5%. The linear algebra kernels show a relatively balanced utilization across the banks, with the coefficient of variation ranging from 0-10.1%. In contrast, both FFT and Conv have a skewed utilization, due to the layout of twiddle coefficients in the SPM banks for FFT, and the small filter size for Conv.

8.3 Design Space Exploration

We performed a design space exploration with the mapped kernels to select R-DCache sizes for Transmuter. Sizes of 4 kB per bank for both L1 and L2 show the best energy-efficiency for all kernels except SpMV. SpMV in Trans-SA benefits from a larger L2 private cache that lowers the number of evictions from fetching discrete packed matrix rows (recall that in Trans-SA, all GPEs in a tile access the same L2 bank). Other kernels achieve slim speedups with larger cache capacities. The dense kernels already exhibit good hit rates

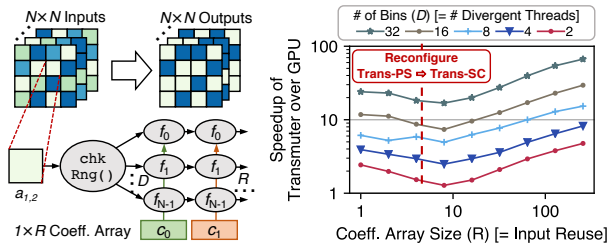

Figure 11: *Left:* A synthetic parallel application that launches threads to process $N \times N$ matrices. Each thread (*i*) reads the input value and bins it into one of D bins, (*ii*) applies R instances of function f_d unique to bin d and writes the result. Each element of a *coefficient* array feeds into f_d. Thus the input is reused R times and the degree of divergence scales with D. *Right:* Speedup of Transmuter with a uniform-random matrix (# GPEs = # GPU threads = 64). Transmuter reconfigures from Trans-PS to Trans-SC beyond $R = 4$.

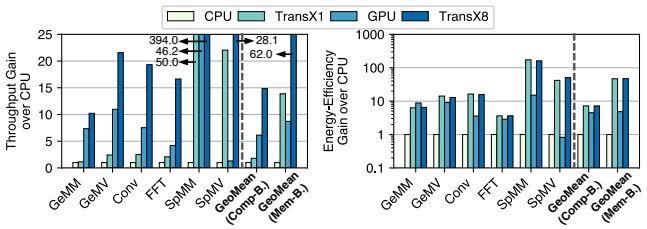

Figure 12: Throughput (left) and energy-efficiency (right) improvements of Transmuter over the CPU and GPU. Data is averaged across the inputs: 256-1k (GeMM), 2k-8k (GeMV), 512-2k (Conv), 4k-16k (FFT), 1k-4k, 0.64% (SpMM), and 2k-4k, 2.6% (r_M), 10.2%-100% (r_v) (SpMV). Geometric mean improvements for the compute-bound and memory-bound kernels are shown separately.

due to blocking and prefetching in Trans-SC. SpMM is bottlenecked by cold misses due to low reuse. FFT has a 3.0× speedup with 64 kB L1/L2, compared to 4 kB L1/L2, as the number of coefficients stored on-chip scales with L1 size. But, this is outweighed by a 6.4× increase in power. Other parameters such as work and status queue depths were chosen to be sufficiently large such that the GPEs are never idled waiting on the LCP.

8.4 Performance with Varying Control Divergence and Data Reuse

In Section 2.2, we characterized some fundamental kernels based on their *control divergence*, *data reuse* and *arithmetic intensity*. We now build an intuition around the architectural advantages of Transmuter over a GPU for applications with notable contrast in these characteristics. We implement a parallel microbenchmark on Transmuter and the GPU that allows independent tuning of the divergence and reuse. Fig. 11 (left) illustrates this application. The reuse (R) is controlled by the size of the coefficient array, while divergence (D) scales with the number of bins, since threads processing each input element apply functions unique to a bin.

While this is a synthetic application, it is representative of real-world algorithms that perform image compression using quantization. We execute this microbenchmark with a batch of 1,000 32×32 images on a 4×16 Transmuter design, and compare it with the GPU running 64 threads (2 warps, inputs in shared memory) to ensure fairness. Fig. 11 (right) presents two key observations:

- The speedup of Transmuter roughly doubles as the number of divergent paths double. This is because threads executing different basic blocks get serialized in the SIMT model (as they are in the same warp), whereas they can execute parallel in SPMD.
- Transmuter has the inherent flexibility to reconfigure based on the input size. In this example, Trans-PS is the best-performing until $R = 4$. Beyond that, switching to Trans-SC enables better performance – up to 7.4× over Trans-PS – as the benefit of sharing the coefficient array elements across the GPEs in Trans-SC outweighs its higher cache access latency.

Takeaways. The SPMD paradigm in Transmuter naturally lends itself well to kernels exhibiting large control divergence, and its ability to reconfigure dynamically allows it to perform well for very low- and high-reuse, and by extension mixed-reuse, workloads.

8.5 Comparison with the CPU and GPU

We now compare the best-performing Transmuter configuration with the CPU and GPU running optimized commercial libraries (Tab. 3). The throughput and energy-efficiency gains of Transmuter for each kernel in Sec. 5 are presented in Fig. 12. We compare TransX1 to the CPU and TransX8 to the GPU, as discussed in Sec. 7.

Compute-Bound Kernels (GeMM, Conv, FFT). TransX1 harnesses high data-level parallelism, and thus achieves performance improvements of 1.2-2.5× over the CPU, despite clocking at $\frac{1}{4}$th the speed of the deeply-pipelined CPU cores. The true benefit of Transmuter's simple cores and efficient crossbars appear in the form of energy-efficiency gains, ranging from 3.6-16.3×, which is owed largely to the high power consumption of the bulky out-of-order CPU cores. Over the GPU, TransX8 gets performance gains of 1.3-2.6× and efficiency improvements of 0.8-4.4× with an efficient implementation on Trans-SC for GeMM and Conv. The ~20% energy-efficiency loss for GeMM is explained by the amenability of GeMM to a SIMT paradigm; although the performance is similar between SIMT and SPMD, SPMD incurs slightly larger energy costs associated with higher control overhead over SIMT. On FFT, Transmuter sustains consistent performance scaling using the spatial dataflow of Trans-SA, with each tile operating on an independent input stream, thus leading to minimum conflicts. The gap between throughput gain (4.0×) and energy-efficiency gain (1.3×) over the GPU is explained by the cuFFT algorithm that is more efficient for batched FFTs.

Memory-Bound Kernels (GeMV, SpMM, SpMV). TransX1 on GeMV achieves 2.4× better throughput over the CPU, with the CPU becoming severely DRAM-bound (>98% bandwidth utilization) for input dimensions beyond 1,024. The 14.2× energy-efficiency gain of TransX1 stems from tuning down the number of active GPEs to curtail bandwidth-starvation, thus saving power.

On SpMM and SpMV, the performance of Transmuter is highly sensitive to the densities and sizes of the inputs, with improvements ranging from 4.4-110.8× over the CPU and 5.9-37.7× over the GPU. With SpMM, execution in Trans-PS enables overcomes the CPU's limitation of an inflexible cache hierarchy, as well as harnesses high MLP across the sea of GPEs. While Transmuter is memory-bottlenecked for SpMM, SpMV is bounded by the scheduling granularity of packing algorithm deployed on Trans-SA. Despite that, for SpMV, TransX1 outperforms both the CPU as well as the GPU that has 7.2× greater available bandwidth. In case of the GPU, while there are sufficient threads to saturate the SMs, the thread divergence in the SIMT model is the bottleneck. The GPU

Table 4: Estimated speedups for the end-to-end workloads in Fig. 2.

Speedup	DANMF	LSTM	Marian	MaxCut	MFCC
TransX1 *vs.* CPU	4.1×	1.1×	2.2×	6.2×	1.7×
TransX8 *vs.* GPU	3.5×	3.8×	2.1×	7.2×	1.6×

	NBSGD	RolePred	SemSeg	Sinkhorn	VidSeg
TransX1 *vs.* CPU	3.5×	2.7×	2.4×	3.1×	2.2×
TransX8 *vs.* GPU	2.8×	2.3×	2.5×	3.0×	2.8×

achieves just 0.6% and 0.002% of its peak performance, respectively for SpMM and SpMV, impaired by memory and synchronization stalls. In comparison, SPMD on Transmuter reduces synchronization, resulting in 21-42% time spent on useful computation (Fig. 9). For SpMM, the outer product implementation demonstrates ASIC-level performance gains of 5.9-11.6× [87] over the GPU, by minimizing off-chip traffic and exploiting the asynchronicity between GPEs. As with GeMV, disabling bandwidth-starved resources contributes to the energy-efficiency gains.

Effect of Iso-CPU Bandwidth. TransX1 uses one HBM stack that provides 125 GB/s peak bandwidth, about 3.6× greater than the DDR3 bandwidth to the CPU. If given the bandwidth of the DDR3 memory, TransX1 still achieves performance gains averaging 17.4× and 6.3× for SpMM and SpMV, respectively. For GeMV, TransX1 remains within a modest 6-8% of the CPU with this low bandwidth.

8.6 End-to-End Workload Analysis

We report the estimated speedups of Transmuter over the CPU and GPU for the end-to-end workloads (Fig. 2) in Tab. 4. File I/O and cross-platform (*e.g.* CPU→GPU) data transfer times are excluded for all platforms. Overall, Transmuter achieves speedups averaging 3.1× over the CPU and 3.2× over the GPU.

Next, we elucidate how rapid reconfiguration enables efficient execution of workloads that involve mixed sparse-dense computation in an inner loop. We make a case study on a representative mixed-data application, namely *Sinkhorn*, that performs iterative computation to determine the similarity between documents [63, 97]. Sinkhorn computation typically involves large, sparse matrices in conjunction with dense matrices. We implement the algorithm described in [18]; see Appendix B. The inner loop has two major kernels: a GeMM operation masked by a sparse weight matrix (M-GeMM), and a dense matrix - sparse matrix multiplication (DMSpM).

The mapping on Transmuter is shown in Fig. 13. M-GeMM uses a variation of blocked-GeMM, wherein only rows/columns of the dense matrices that generate an element with indices corresponding to non-zeros in the weight matrix are fetched and multiplied. DMSpM uses a simplified outer product algorithm similar to SpMM (Sec. 5.3) that splits the kernel into DMSpM-Multiply and DMSpM-Merge.

We show the analysis of Sinkhorn on different Transmuter sizes in Fig. 14. As observed, M-GeMM and DMSpM-Multiply exhibit the best performance in Trans-SC configuration, due to good data reuse across GPEs. In contrast, DMSpM-Merge has optimal performance on Trans-PS, exhibiting a 84.9-98.3% speedup (not shown in figure) over Trans-SC. Therefore, the optimal Sinkhorn mapping involves *two reconfigurations* per iteration: Trans-SC → Trans-PS before the start of DMSpM-Merge, and Trans-PS → Trans-SC at the end of it, for the next M-GeMM iteration. Recall from Sec. 4.7 that the reconfiguration time is ~10 cycles, and hence does not perceptibly impact the performance or energy. Cache flushing (net 0.2% of the total execution time) is required for M-GeMM but not DMSpM, as DMSpM uses

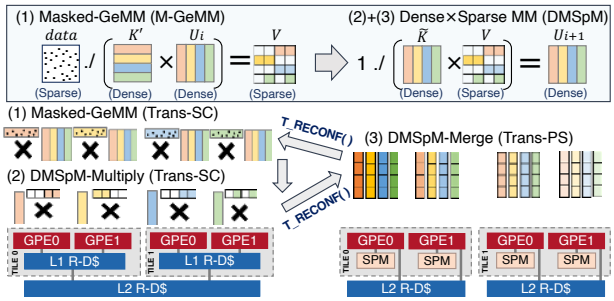

Figure 13: Mapping of a multi-kernel, mixed data application, Sinkhorn, on Transmuter. Computation iterates between M-GeMM and DMSpM, with Trans-SC ↔ Trans-PS reconfiguration before and after DMSpM-Merge. DMSpM-Merge benefits from the private SPMs in Trans-PS, since each GPE works on multiple disjoint lists.

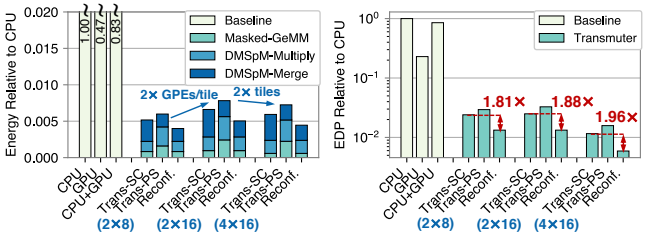

Figure 14: Per inner-loop iteration energy (left) and EDP (right) comparing Trans-SC, Trans-PS and Reconf. (Trans-SC ↔ Trans-PS) for Sinkhorn normalized to CPU. Input matrix dimensions and densities are — *query*: (8k×1), 1%, *data*: (8k×1k), 1%, *M*: (8k×8k), 99%.

a streaming algorithm. Overall, dynamic reconfiguration results in 47.2% and 96.1% better performance and energy-delay product (EDP), respectively, over Trans-SC-only for the 4×16 Transmuter. A heterogeneous solution is also compared against, where M-GeMM is done on the CPU and DMSpM on the GPU, but this implementation is bottlenecked by CPU → GPU data transfers. As derived from Figure 14, the 4×16 Transmuter achieves 38.8× and 144.4× lower EDP than the GPU and heterogeneous solutions, respectively.

8.7 Comparison with Other Platforms

Tab. 5 shows the estimated energy-efficiency improvements of Transmuter over recent FPGA, CGRA and ASIC implementations. The efficiencies reported in prior work are scaled quadratically for iso-technology comparisons with Transmuter. Overall, Transmuter achieves average efficiency gains of 3.4× and 2.0× over FPGAs and CGRAs, respectively, and is within 9.3× (maximum 32.1×) of state-of-the-art ASICs for the evaluated kernels.

8.8 Power and Area

Tab. 6 details the power consumption and area footprint of a 64×64 Transmuter cluster in 14 nm. Most of power is consumed by the network and memory, *i.e.* L1 R-XBars, R-DCaches and ICaches, while the cores only consume 20.8%. This is consistent with a growing awareness that the cost of computing has become cheaper than the cost to move data, even on-chip [42]. GPEs and L1 R-XBars, the most frequently switched modules, consume 84.2% of the total dynamic power. The estimated power for a single Transmuter cluster is 13.3 W in 14 nm with an area footprint within 1.7% of the CPU's area. The estimated worst-case reconfiguration overhead is 74.9 nJ.

Table 5: Energy-efficiency improvements (black) and deteriorations (red) of Transmuter over prior FPGAs, CGRAs and ASICs.

Platform	GeMM	GeMV	Conv	FFT	SpMM	SpMV
FPGA	2.7× [34]	8.1× [64][3]	2.7× [119]	2.2× [34]	3.6× [35]	3.0× [23]
CGRA	2.2× [95]	3.0× [19]	1.2× [19]	1.0× [52][4]	1.9× [19]	2.9× [19]
ASIC	(32.1×) [91]	(10.5×) [98]	(13.8×) [109] (7.6×) [98]	(18.1×) [92] (17.0×) [26]	(3.0×) [88] (4.1×) [120]	(3.9×) [87]

[3]Performance/bandwidth used as power is N/A. [4]Estimated for floating-point based on [108].

Table 6: Power and area of a 64×64 Transmuter cluster in 14 nm.

Module	Power (mW)			Area (mm^2)
	Static	Dynamic	Total	
GPE Cores	361.3	2380.5	2741.7	28.9
LCP Cores	5.6	22.5	28.1	0.4
Sync. SPM	0.6	0.1	0.6	0.1
All ICaches	2566.6	373.6	2940.1	25.7
LCP DCaches	39.5	0.9	40.4	0.5
L1 R-DCaches	2527.1	204.0	2731.0	30.7
L2 R-DCaches	37.4	18.3	55.7	0.5
L1 R-XBars	1757.8	2149.3	3907.1	30.3
L2 R-XBars	36.9	14.8	51.7	0.8
MUXes/Arbiters	581.9	87.6	669.5	0.7
Memory Ctrls.	47.5	129.0	176.4	5.5
Total	**8.0 W**	**5.4 W**	**13.3 W**	**124.1 mm^2**

9 RELATED WORK

A plethora of prior work has gone into building programmable and reconfigurable systems in attempts to bridge the flexibility-efficiency gap. A qualitative comparison of our work over related designs is shown in Tab. 7. `Transmuter` differentiates by supporting two different dataflows, reconfiguring faster at a coarser granularity, and supporting a COTS ISA/compiler.

Reconfigurability. A few prior work reconfigure at the sub-core level [19, 44, 55, 76, 95] and the network-level [37, 56, 83, 107]. In contrast, `Transmuter` uses native in-order cores and the reconfigurablity lies in the memory and interconnect. Some recent work propose reconfiguration at a coarser granularity [4, 19, 70, 95]. PipeRench [36] builds an efficient reconfigurable fabric and uses a custom compiler to map a large logic configuration on a small piece of hardware. HRL [33] is an architecture for near-data processing, which combines coarse- and fine-grained reconfigurable blocks into a compute fabric. The Raw microprocessor [107] implements a tiled architecture focusing on developing an efficient, distributed interconnect. Stream Dataflow [83] and SPU [19] reconfigure at runtime, albeit with non-trivial overheads to initialize the Data-Flow Graph (DFG) configuration. `Transmuter`, on the other hand, relies on flexible memories and interconnect that enable fast on-the-fly reconfiguration, thus catering to the nature of the application.

Flexibility. Prior work has also delved into efficient execution across a wide range of applications. Plasticine [95] is a reconfigurable accelerator for parallel patterns, consisting of a network of Pattern Compute/Memory Units (custom SIMD FUs/single-level SPM) that can be reconfigured at compile-time. Stream Dataflow [83] is a new computing model that efficiently executes algorithms expressible as DFGs, with inputs/outputs specified as streams. The design comprises a control core with stream scheduler and engines, interfaced around a custom, pipelined FU-based CGRA. SPU [19] targets data-dependence using a stream dataflow model on a reconfigurable fabric composed of decomposable switches and PEs that split networks into finer sub-networks. The flexibility of `Transmuter` stems from the use of general-purpose cores and the reconfigurable memory subsystem that morphs the dataflow and on-chip memory, thus catering to both inter- and intra-workload diversity.

Table 7: Qualitative comparison with prior work [19, 39, 83, 95, 107].

Architecture	PE Compute Paradigm	Dataflow	Compiler Support	Reconfig. Granularity	On-chip Memory
Plasticine	SIMD	Spatial	DSL	Pipeline-level, compile-time	SPM
Stream Dataflow	SIMD	Stream	ISA extn.	Network-level, run-time	SPM+FIFO
SPU	SIMD	Stream	ISA extn.	Network-/ Sub-PE-level, run-time	Compute-enabled SPM+FIFO
Ambric	MIMD/ SPMD	Demand-driven	Custom	Network-level, run-time	SPM+FIFO
RAW	MIMD/ SPMD	Demand-driven	Modified COTS	Network-level, run-time	Cache
`Transmuter` [this work]	**MIMD/ SPMD**	**Demand-driven/ Spatial**	**COTS**	**Network-/ On-chip-memory-level, run-time**	**Reconfig. Cache/SPM/ SPM+FIFO**

Programmability. There have been proposals for programmable CGRAs that abstract the low-level hardware. Some work develop custom programming models, such as Rigel [53] and MaPU [112]. Others extend an existing ISA to support their architecture, such as Stitch [105] and LACore [102]. Plasticine [95] uses a custom DSL called Spatial [57]. Ambric [39] is a commercial system composed of asynchronous cores with a software stack that automatically maps Java code onto the processor-array. `Transmuter` distinguishes itself by using a standard ISA supported by a simple library of high-level language intrinsics and a COTS compiler, thus alleviating the need for ISA extensions or a DSL.

10 CONCLUSION

This work tackled the important challenge of bridging the flexibility-efficiency gap with `Transmuter`. `Transmuter` consists of simple processors connected to a network of reconfigurable caches and crossbars. This fabric supports fast reconfiguration of the memory type, resource sharing and dataflow, thus tailoring `Transmuter` to the nature of the workload. We also presented a software stack comprised of drop-in replacements for standard Python libraries. We demonstrated `Transmuter`'s performance and efficiency on a suite of fundamental kernels, as well as mixed data-based multi-kernel applications. Our evaluation showed average energy-efficiency improvements of 46.8× (9.8×) over the CPU (GPU) for memory-bound kernels and 7.2× (1.6×) for compute-bound kernels. In comparison to state-of-the-art ASICs that implement the same kernels, `Transmuter` achieves average energy-efficiencies within 9.3×.

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A LOW-LEVEL PROGRAMMING INTERFACE

Table 8: Critical host- and Transmuter-side C++ intrinsics used to write optimized kernel libraries (TID = Tile ID, GID = GPE ID). Note that the API is depicted for a single-cluster design, for simplicity.

Host-side Intrinsic Signature	Description
H_INIT()	Initialize host-Transmuter interface
H_LAUNCH()	Trigger Transmuter to start executing the kernel
H_FINISH()	Wait (block) until Transmuter finishes executing
H_SEND_DATA(&dst,&src,size)	Mem-copy from external DRAM to HBM
H_RETR_DATA(&dst,&src,size)	Mem-copy from HBM to external DRAM
H_SET_†_ARG(argID,&arg,TID,[GID])	Copy an argument to an LCP or GPE
H_COMPILE_BIN(path_to_bin,flags)	Dynamically compile GPE/LCP code
H_LD_BIN_†(&bin,TID,[GID])	Stream compiled GPE/LCP binary into the HBM
H_SYNC_ALL()	Synchronize with all LCPs and GPEs
H_RECONF(en_flag,TID,[GID])	Dynamically enable/disable GPE/LCP
H_RECONF<level>(config)	Trigger R-DCache/XBar reconfiguration
H_CLEANUP()	Teardown host interface and deallocate structures
Transmuter-side Intrinsic Signature	**Description**
T_LD_WORD(addr)	Read a word from SPM; addr determines the bank
T_ST_WORD(addr,val)	Write a word into SPM; addr determines the bank
T_SA_POP(direction)	Pop data from systolic neighbor GPE
T_SA_PUSH(direction,val)	Push data to systolic neighbor GPE
T_+Q_PUSH(val,[GID])	Push data to work/status queue
T_+Q_POP([GID])	Pop data from work/status queue
T_FREE_WORKQ_PUSH(val)	Push to the work queue of a free GPE
T_WORKQ_PUSH_BCAST(val)	Broadcast to all work queues in the tile
T_FLUSH<level>(bank)	Flush dirty data from to the next level
T_SPM_BOT<level,config>()	Get a pointer to bottom of R-DCache/Sync. SPM
T_SPM_TOP<level,config>()	Get a pointer to top of R-DCache/Sync. SPM
T_SYNC_LCPS()	Synchronize with all LCPs in Transmuter
T_SYNC_TILE()	Synchronize with all GPEs and LCP in the tile
T_SYNC_ALL()	Synchronize with all LCPs, GPEs and host
T_SLEEP()	Put self into sleep to conserve power
T_RECONF<level>(self_flag,config)	Self-reconfigure R-DCache/XBar / wait for host

†: LCP/GPE +: WORK/STATUS

B SINKHORN ALGORITHM

Algorithm B.1 Sinkhorn Distance (MATLAB syntax)

function SINKHORN(query, data, M, γ, ϵ)
▷ M: distance matrix, γ: regularization parameter, ϵ: tolerance
  $o = \text{size}(M, 2)$;
  $H = \text{ones}(\text{length}(query), o)/\text{length}(query)$;
  $K = \exp(-M/\gamma)$; $\tilde{K} = \text{diag}(1./query)K$;
  $err = \infty$; $U = 1./H$;
  while $err > \epsilon$ **do**
    $V = data./(K'U)$; ▷ Masked-GeMM
    $U = 1./(\tilde{K}V)$; ▷ DMSpM
    $err = \text{sum}((U - U_{prev})^2)/\text{sum}((U)^2)$;
  end while
  $D = U. * ((K. * M)V)$;
return sum(D) ▷ Sinkhorn Distance between query and data
end function

C SELECTED KERNEL IMPLEMENTATIONS

Algorithm C.1 GeMV on Transmuter in Trans-SC configuration

function GEMV_LCP($start$, end, N_G)
▷ $start$: start row index, end: end row index, N_G: num. GPEs per tile
  $gid = 0$;
  for $row \leftarrow start$ to end **do**
    T_WORKQ_PUSH(gid, row);
    $gid = (gid == N_G - 1)\ ?\ 0 : (gid + 1)$;
  end for
  T_WORKQ_PUSH_BCAST(-1);
end function
function GeMV _GPE($A, B, C, N, \alpha, \beta$) ▷ $C = \alpha \cdot A * B + \beta \cdot C$, N: matrix dim.
  while (row = T_WORKQ_POP()) != -1 **do**
    $psum = 0$;
    for $col \leftarrow 0$ to $N - 1$ **do**
      $psum += A[row][col] * B[col]$;
    end for
    $C[row] = \beta * C[row] + \alpha * psum$;
  end while
end function

Algorithm C.2 SpMV on Transmuter in Trans-SA configuration

function SPMV_LCP( )
  T_WORKQ_PUSH_BCAST(1);
end function
function SPMV_GPE($A_{rowID}, A_{colID}, A_{val}, A_{part}, B, B_{part}, C, N, P$)
▷ $C = A * B$, N: matrix/vector dim., N_G: num. GPEs per tile, N_T: num. tiles
  T_WORKQ_POP();
  $parts_{per\_tile} = \text{ceil}(N/N_T)$; ▷ partitions per tile
  $i = A_{part}[gid * N_T * N_G + tid]$
  for $part \leftarrow tid * parts_{per\_tile}$ to $(tid + 1) * parts_{per\_tile}$ **do**
    $b_{start} = B_{part}[part][gid]$; ▷ tid: tile ID, gid: GPE ID
    $b_{end} = B_{part}[part][gid + 1]$;
    $sp = sp_{start}$ = T_SPM_BOT<Lev::L1, Conf::systolic_array_1d>();
    for $j \leftarrow b_{start}$ to b_{end} **do**
      T_ST_WORD(sp++, $B[j]$);
    end for
    $sp_{sum} = sp$;
    for $row \leftarrow part * P$ to $(part + 1) * P$ **do** ▷ P: row partition per tile
      $psum = 0$;
      while $A_{rowID}[i] == row$ **do**
        b = T_LD_WORD($sp_{start} + A_{colID}[i]$);
        $psum += A_{val}[i$++$] * b$;
      end while
      T_ST_WORD(sp++, $psum$);
    end for
    for $row \leftarrow 0$ to P **do**
      $popped$ = (gid != 0) ? T_SA_POP(Dir::West) : 0;
      $sum = popped$ + T_LD_WORD($sp_{sum} + row$);
      if $gid == N_G - 1$ **then**
        $C[part * P + row] = sum$;
      else
        T_SA_PUSH(Dir::East, sum);
      end if
    end for
  end for
end function

Algorithm C.3 FFT on Transmuter in Trans-SA configuration

function FFT_LCP($input$, $output$, N, is_input, is_output)
▷ N: FFT size, $\log_2(N)$: num. FFT stages
  if is_input **then**
    for $i \leftarrow 0$ to $N - 1$ **do**
      T_WORKQ_PUSH(0, $input[i]$);
    end for
  end if
  if is_output **then**
    for $i \leftarrow 0$ to $N - 1$ **do**
      $output[i]$ = T_STATUSQ_POP($\log_2(N) - 1$);
    end for
  end if
end function
function FFT_GPE($input$, $output$, N_G, N, S, P)
▷ N_G: num. GPEs per tile, S: step size, P: next step size
  $id = gid + tid * N_G$;
  sp = T_SPM_BOT<Lev::L1, Conf::systolic_array_1d>();
  for $i \leftarrow 0$ to $N/2$ **do**
    in_1 = (id == 0) ? T_WORKQ_POP() : T_SA_POP(Dir::West);
    in_2 = (id == 0) ? T_WORKQ_POP() : T_SA_POP(Dir::West);
    out_1, out_2 = compute_butterfly(in_1, in_2);
    if $id == \log_2(N) - 1$ **then**
      T_STATUSQ_PUSH(out_1); T_STATUSQ_PUSH(out_2);
    else
      T_ST_WORD($sp + i, out_1$); T_ST_WORD($sp + i + S, out_2$);
      if $i > P - 1$ **then**
        T_SA_PUSH(Dir::East, T_LD_WORD($sp + i - P$));
        T_SA_PUSH(Dir::East, out_1);
      end if
    end if
  end for
  for $i \leftarrow 0$ to P **do**
    T_SA_PUSH(Dir::East, T_LD_WORD($sp + S + i$));
    T_SA_PUSH(Dir::East, T_LD_WORD($sp + S + P + i$));
  end for
end function