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# Transparent and Flexible Carbon Nanotube Transistors

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## ABSTRACT

**We report the fabrication of transparent and flexible transistors where both the bottom gate and the conducting channel are carbon nanotube networks of different densities and Parylene N is the gate insulator. Device mobilities of 1 $cm^2\ V^{-1}\ s^{-1}$ and on/off ratios of 100 are obtained, with the latter influenced by the properties of the insulating layer. Repetitive bending has minor influence on the characteristics, with full recovery after repeated bending. The operation is insensitive to visible light and the gating does not influence the transmission in the visible spectral range.**

The quest for flexible and transparent transistors has recently resulted in several noteworthy achievements. Transparent transistors have been fabricated using both polymers[1−3] and inorganic oxides.[4,5] These advances, notable in the emerging technology arena that is generally called "plastic electronics", have received wide publicity. Both, nevertheless, have significant deficiencies. The former have low mobility and the latter do not have the desired flexibility and are not easily manufacturable. These factors severely limit the application potential of the devices. Our method introduces a transistor architecture that potentially includes only two materials: carbon nanotubes (NTs) and a polymeric gate insulator. This simplicity of structure would ensure a simple manufacturing process.

Carbon nanotubes, because of their excellent electronic properties, have been explored for applications as active electronic devices. Field effect transistors (FETs) with NT conducting channels have been fabricated[6,7] and their properties and operation explored.[8−10] Subsequently, it has been shown[11,12] that a random network of nanotubes with an appropriate density can also act as a conducting channel in a FET configuration. This has opened up the avenue for a manufacturable device architecture. Room-temperature fabrication techniques enabling flexible transistors[13] have also been explored. It has been shown that, due to the high mobility of carbon nanotubes, a network with low sheet resistance is also transparent in the visible spectral range.[14,15] We have fabricated, using an extremely simple spray technology, field effect transistors where carbon nanotube networks of different densities provide both the gate and the conducting channel. We find that the devices are highly transparent, that the mobility is superior to that of organic transistors, and that repeated bending does not lead to a substantial effect on the transistor characteristics. The transistor architecture, aside from having a possible impact on a new technology, represents a further step in the advancement of carbon nanotube based transistors.

A schematic illustration of the FET devices that have been fabricated is shown in Figure 1 together with an optical image of one of the transistors. The devices were prepared on a sheet of polyester (PE), using purified, single walled HipCO nanotubes from CNI (used as received). Because nanotubes are hydrophobic, they stick well to the hydrophobic surface of the PE. The PE sheets used were simple plastic sheets normally used as transparency slides, although any plastic with a similar surface hydrophobicity can be used as the substrate. To form the gate layer of the FET, a suspension of SWNTs was sprayed onto the PE substrate forming a dense nanotube network.[16] The suspension consisted of a concentration of 1 mg/mL of nanotubes in a 1% solution of aqueous sodium dodecyl sulfate (SDS). The suspension was sonicated for 1 h at 40 W using a probe sonicator and then centrifuged at 14000 rpm for 20 min. After centrifugation, the suspension was decanted so that only the supernatant of the centrifuged material was included in the final suspension. Centrifuging and decanting removes large, heavier bundles from the suspension. The suspension was then sprayed onto the PE substrate while the substrate was heated to 100 °C. Heating the substrate prevents droplets from forming on the surface, thus inhibiting flocculation of the nanotubes. After several layers of NT are sprayed onto the PE, the substrate

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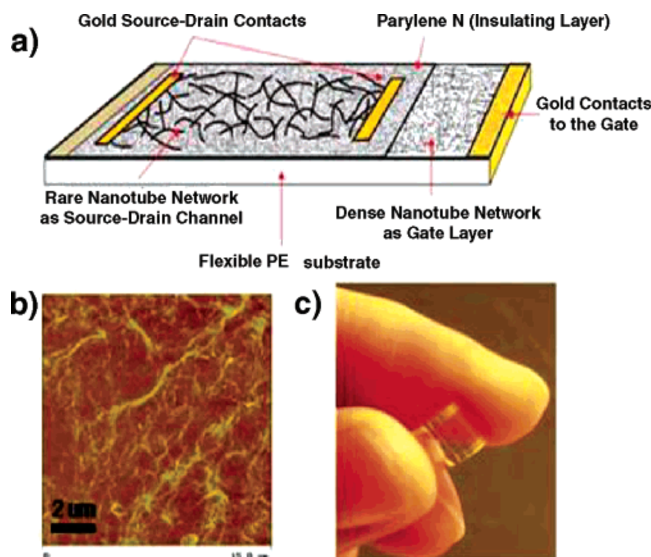


**Figure 1.** (a) Schematic layout of the transistor architecture. (b) AFM image of the NT network which acts as the gate layer. (c) Optical image of the transistor being flexed. The gold lines are used to contact the gate through the back of the device. (The source−drain contacts have not yet been applied.)

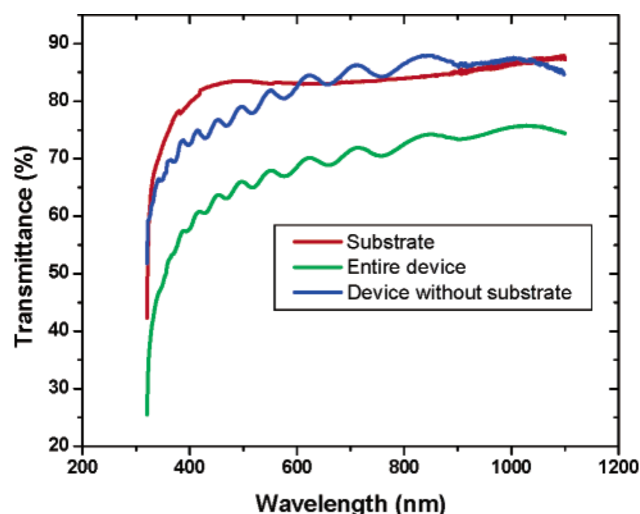


**Figure 2.** Optical transmission versus wavelength of a typical device. The graph displays the transmission of the substrate, the device, and the architecture of the device after dividing out the substrate. Devices with different densities in the conducting channel do not have substantially different transmission spectra, as the conducting channel is much more transparent than the NT network which forms the gate layer. The gate, insulating layer, and conducting channel has a combined 80% transparency in the visible range.

is rinsed in distilled water to remove the SDS. Thin strips of gold were evaporated at opposite edges of the substrate on top of the NT network and silver paint was used to connect the gold strips to the back of the substrate. This way, the gate could be contacted through the back of the device.

The insulating layer in our devices consisted of a 1.5 $\mu$m thick layer of Parylene N which was evaporated directly onto the dense NT layer. Although there are transparent and flexible dielectrics that have better insulating properties, Parylene N forms a pinhole-free layer and thus insulates well despite the uneven surface of the dense NT network. Parylene can also be deposited at room temperature, ensuring that the PE substrate will not be damaged in the deposition process.

A similarly prepared suspension of NT in 1% SDS at a concentration of 0.35 mg/mL was used to deposit the NT network for the source−drain channel. To get a thin, homogeneous network for the source−drain channel, the NTs were adsorbed onto the parylene. A single drop of the suspension is placed on the parylene and then blown off using an air gun. The device is then rinsed in water to remove the SDS. This process is repeated drop-by-drop until the desired source−drain channel network density is reached. Gold contacts are then evaporated onto the NT network to form the source and the drain. The devices had a channel ratio width/length of approximately 1.

AFM images (Figure 1b) show that the NT network in the gate layer consists mostly of bundles with an average diameter of 20 nm and fairly homogeneous coverage. The average sheet resistance of the gate layer is 2.4 k$\Omega$/sq, which corresponds to approximately 12 NT bundles/um$^2$ using the data from Hu et al.[15] Because the purpose of the gate layer is to apply an electric field, and not to pass current, it is not necessary to achieve a low sheet resistance in this layer. The source−drain channel network is composed of similarly sized bundles, though it is much less dense (density around 1 NT bundle/um$^2$), with sheet resistances ranging from 30 to 150 M$\Omega$/sq.

The optical transmittance of the devices was measured using a Beckman Coulter DU 640 spectrophotometer. The transistor characteristics were measured using a Keithley 2400 sweeping the gate voltage from $\pm$35 V at a rate of 14 V/s and a source−drain bias of 500 mV. Comparing the transistor characteristics of three devices with NT networks of different densities in the source-drain channel reveals that a denser network channel leads to overall higher conduction, but a correspondingly lower on/off ratio. Of the forty devices we fabricated that were not shorted through the gate layer, devices intentionally fabricated to have the same conducting channel density had identical transistor characteristics to within 10%. Because the density of the nanotube network in the conducting channel can be tuned by controlling the number of drops of nanotube suspension adsorbed, it is much easier to get reproducible devices than with CVD methods.

The optical transparency of a typical device, shown in Figure 2, is displayed in the visible to NIR spectral range. At 550 nm, the transparency of the entire device was found to be approximately 68%, weakly dependent on the wavelength. The interference pattern in the optical data is due to reflection within the parylene layer, which is of the same order thickness as the wavelengths studied. Because a different, more transparent plastic substrate may be used in further developments of the technology, it is interesting to consider the transmittance of the active components of the device. Dividing out the substrate yields a transparency of the gate, insulating layer, and source−drain channel of 81%. Although this approach is not a fully consistent description

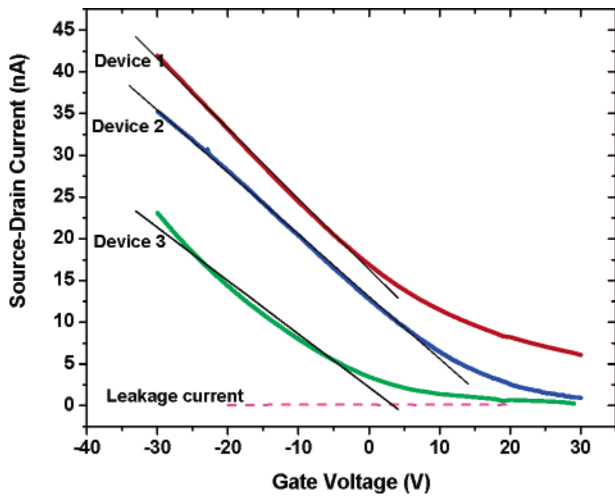


**Figure 3.** Source−drain current at $V_{sd} = 500$ mV versus the drain voltage for three devices with different nanotube network densities in the conducting channel. Device 1 has the most dense network, while Device 3 has the least dense network. The behavior is representative of a p-type field-effect transistor response. Fits to the linear portion accompany each curve. The dashed line displays the leakage current for a typical device, and this leakage current is roughly independent of voltage.

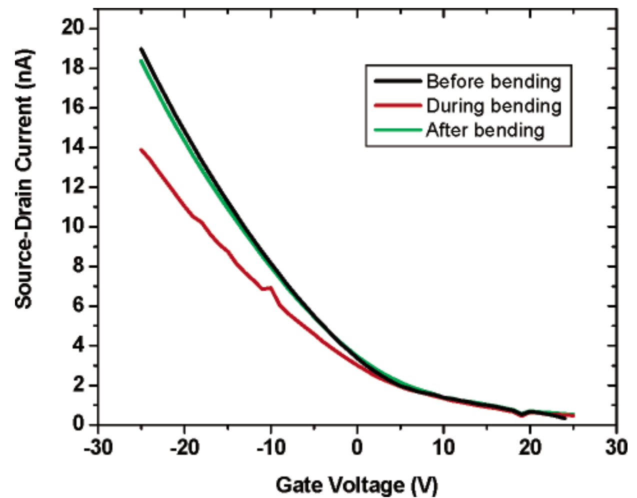


**Figure 4.** Transistor characteristics upon bending to almost 180° and after the bending force was removed.

of the optical properties of the system, which consists of three layers and may include internal reflection at the different material boundaries, it gives a good first order approximation of the transparency of the nanotube networks. Using this same approximation, we found the NT network acting as the gate to have a transparency of 85%, the parylene layer to have a transparency of 95%, and the NT network in the source−drain channel to have a transparency of approximately 100%.

The transistor characteristics of three typical devices are displayed in Figure 3. The three devices have identical gate networks but networks of different densities in the source−drain channel. Device 1 has the most dense network, with a sheet resistance of 30 MΩ/sq. Device 2 has a less dense network with a sheet resistance of 39 MΩ/sq, and Device 3 has the least dense network with a sheet resistance of 144 MΩ/sq. Plotted with each device characteristic is a fit to the linear portion of the data. The leakage current of a typical device is also shown, and this leakage current is roughly independent of the applied gate voltage.

Although the devices do not reach saturation in the "on" state, the on/off ratio for the applied voltage range can still be estimated. Device 3 has an on/off ratio of approximately 90. Device 2 has an on/off ratio around 70, while Device 1, with the most dense NT network, has an on/off ratio around 7. It is expected that the device with the rarest NT network will have a higher on/off ratio because this device will have fewer all-metallic paths which remain conducting even when the device is in the "off" state. Furthermore, the leakage current through the dielectric is on the order of the "off" current in this device, and so using a better dielectric in order to decrease the leakage current could improve the on/off ratio even more. If we subtract the leakage current from the off current, the on/off ratio for the rarest device improves to around 400.

Using a standard expression for mobility,

$$\mu = \frac{l}{w}\frac{dI_{sd}}{dV_g}\frac{d}{k\epsilon_0}\frac{1}{V_{sd}} \tag{1}$$

the mobilities of the devices were estimated. In this expression, $l$ represents the length of the channel (i.e., the distance between the source and the drain contacts), $w$ is the width of the channel, $d$ is the thickness of the dielectric layer, $k$ is the dielectric constant of the dielectric (approximately 3 for Parylene N), and $V_{sd}$ is the source-drain voltage bias at which the transfer characteristics were measured. To estimate $dI_{sd}/dV_g$, we measured the slope of the $I-V_g$ curve in the linear region. Though the slopes of the three plots appear similar in Figure 3, the source−drain channel geometries were slightly different in the different devices, resulting in different estimated mobilities.

The device with the least dense NT network in the source−drain channel, Device 3, has an estimated mobility of 0.5 $cm^2\ V^{-1}\ s^{-1}$. Device 2 has an estimated mobility of 0.6 $cm^2\ V^{-1}\ s^{-1}$. The device with the more dense NT network, Device 1, has an estimated mobility of 1 $cm^2\ V^{-1}\ s^{-1}$. It is understandable that the device with a more dense NT network would have a higher mobility[17] because in a dense NT network there are more paths through which the electrons may travel.

To test the devices' flexibility, transistor characteristic measurements were taken before, during, and after bending the device to a radial angle of 160°. Figure 4 displays the results. Although the current is reduced slightly while the device is bent, the device recovers completely afterward.

We have demonstrated the possibility of a flexible and transparent transistor architecture where different components are fabricated using carbon nanotube networks. While certain parameters of the devices are comparable to transistors fabricated using room-temperature processes, significant improvements are expected with improved nanotube network characteristics. As is evident form Figure 1b, and also from

the high sheet resistances, bundles of nanotubes − with current most likely flowing at the outer regions of the bundles − dominate the transport process. Better dispersion on the surface, together with improved starting material and a better dielectric, will lead to improved device performance, approaching those found in devices fabricated using chemical vapor deposition methods.[11,12] The fabrication of the transistor architecture demonstrates the versatility of carbon nanotube networks transparent enough to allow applications in areas ranging from active matrix displays to smart windows. While our architecture is based on surface-supported networks, composites[18] and self-assembled networks[19] of carbon nanotubes can also be used for fabricating devices as described. Furthermore, with source and drain potentially also fabricated using carbon nanotube networks, the architecture opens up the avenue toward simple electronic device fabrication, including potentially only two types of materials: carbon nanotubes and a polymeric insulating layer.

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