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FEATURE ARTICLE

Transparent metal oxide nanowire transistors

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With the features of high mobility, a high electric on/off ratio and excellent transparency, metal oxide nanowires are excellent candidates for transparent thin-film transistors, which is one of the key technologies to realize transparent electronics. This article provides a comprehensive review of the state-of-the-art research activities that focus on transparent metal oxide nanowire transistors. It begins with the brief introduction to the synthetic methods for high quality metal oxide nanowires, and the typical nanowire transfer and printing techniques with emphasis on the simple contact printing methodology. High performance transparent transistors built on both single nanowires and nanowire thin films are then highlighted. The final section deals with the applications of transparent metal oxide nanowire transistors in the field of transparent displays and concludes with an outlook on the current perspectives and future directions of transparent metal oxide nanowire transistors.

1. Introduction

Transparent electronics with invisible electronic components, which is emerging as an essential technology for the next generation of electronic and optoelectronic devices, has attracted numerous research efforts due to its great potential to make significant commercial impact in a wide variety of areas, such as transparent displays, photodetectors, sensors, Li-ion batteries, solar cells, *etc.*[1–17] Transparent thin-film transistors (TFTs) are the fundamental building blocks in realizing the potential applications of transparent electronics.[18–28] The suitable transparent TFTs for transparent electronics should have excellent transparency, high device mobility, a high electric on/off ratio, moderate carrier concentrations, low threshold voltages, and steep sub-threshold slopes.

Until now, several kinds of semiconductors have been widely used as active channel materials for TFTs, including amorphous silicon (α-Si), polycrystalline silicon, organic semiconductors, and metal oxides.[18–50] α-Si is one of the most reliable materials for

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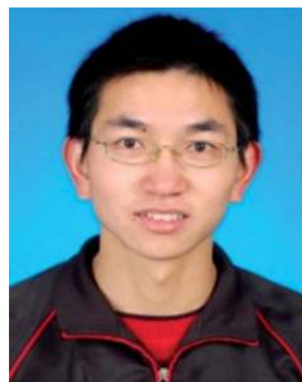

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TFTs and is currently widely used in liquid crystal displays (LCDs). However, a high processing temperature is required to fabricate the TFTs and the device usually has a low mobility of about 1 $cm^2 V^{-1} s^{-1}$. To improve the mobility, polycrystalline silicon was then developed, which exhibited a mobility of around 150 $cm^2 V^{-1} s^{-1}$. This field developed very fast and TFTs built on polycrystalline Si became widely used in active matrix organic light emitting diode (AMOLED) displays. Unfortunately, a high processing temperature is still required, and polycrystalline Si is opaque, which makes it unsuitable for transparent electronic applications.

TFTs fabricated on organic semiconductors have been widely studied in the past years. Organic semiconductors have good transparency, wide material variation and are compatible with plastic substrates. Pentacene-related materials are the most popular ones among semiconducting organics. However, organic TFTs have quite low mobility ($\sim$0.1 to 1 $cm^2 V^{-1} s^{-1}$) and are very sensitive to the atmosphere, so very good device packaging is required, which prevents their wider application.

Among semiconductors, metal oxides stand out as one of the most versatile materials owing to their diverse properties and functionalities. They are widely used as piezoelectric devices, chemical and biosensors, photodetectors, in memory applications and in many kinds of transistors, including CMOS transistors, ambipolar transistors, transparent transistors, and flexible transistors. Transistors built on metal oxides usually show much higher device mobilities when compared with α-Si, polycrystalline Si and organic semiconductors. For instance, using rf magnetron sputtering synthesized amorphous indium zinc oxide (IZO) as the active channels, Fortunato *et al.* fabricated transparent TFTs with a high mobility of 22.7 $cm^2 V^{-1} s^{-1}$ and an on/off ratio of 7×10^7. Olziersky *et al.* studied the Ga_2O_3–In_2O_3–ZnO channel composition on the performance of TFTs and obtained a high mobility of 51.7 $cm^2 V^{-1} s^{-1}$.

Metal oxides have another feature of easily tuned semiconducting properties. People are able to synthesize both p-type and n-type oxides by fine-tuning the introduction of proper dopants or by forming them into heterostructures.[51–53] This means that metal oxide thin-films are able to make both n-type TFTs and p-type TFTs. Furthermore, it is easy for wide band gap metal oxide thin-films to form Ohmic contacts with metal electrodes. To improve the stability and performance of metal oxide TFTs, surface passivation and optimized insulators are the most popular approaches. Surface passivation tunes the surface defect states of metal oxides, thus improving the mobility, on/off ratio and sub-threshold slope. Choosing optimized insulators improves the gate capacitance, thus also improving the device performance in terms of increased mobility, on/off ratio, *etc.*

Besides metal oxide thin-films, recently extensive work was done on carbon nanotube-based transparent transistors with significantly improved mobilities.[54–63] For example, using transfer printed aligned carbon nanotubes as the active channel materials, we fabricated fully transparent TFTs on both glass and PET substrates. The as-fabricated devices have mobilities higher than 1300 $cm^2 V^{-1} s^{-1}$. They can be used as the driving circuitry to control commercial GaN-based LEDs. Other research on carbon nanotube-based transparent TFTs were also performed. However, a critical drawback for the carbon nanotube-based transparent TFTs is that it is hard to control the semiconducting properties of carbon nanotubes because semiconducting carbon nanotubes usually co-exist with metallic carbon nanotubes (Table 1).

In contrast, metal oxide nanowires exhibit excellent semiconducting behavior and they have attracted significant interest for their use as active channel materials for transparent

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TFTs.[15,16] The ability to decouple high temperature material growth processes from device fabrication makes metal oxide nanowires very attractive for high performance transparent TFTs with high transparency, high carrier mobilities, low threshold voltages and steep sub-threshold slopes. A typical fabrication process includes the synthesis of high quality crystalline metal oxide nanowires *via* vapor or solution methods, usually at a high temperature, followed by direct transfer or printing the as-grown nanowires to transparent glass or organic substrates at a low temperature, and then the lithograph-assisted process to complete the total transparent TFT fabrication.

In this article, we provide a comprehensive review of high performance transparent transistors with metal oxide nanowires as the key material set. This article begins with a brief introduction to the methodologies developed for the synthesis of high quality metal oxide nanowires, including vapor phase methods and solution-based methods. Nanowire transfer and printing are then discussed, with a focus on the simple contact printing method, which is very useful for nanowire alignments for future device fabrication and integration. Metal oxide nanowire-based transparent single nanowire transistors and nanowire-thin-film transistors are then discussed in detail. The final section of this paper deals with the important applications of transparent metal oxide nanowire transistors as driving circuits for next-generation transparent displays. We conclude this paper with certain perspectives and an outlook on the future developments in the transparent metal oxide nanowire transistors field.

2. Nanowire synthesis

Metal oxide nanowires have been synthesized by a variety of chemical or physical methods based on the vapor phase or solution phase processes.[64–103]

2.1 Vapor phase methods

Vapor phase methods include thermal evaporation, metal organic chemical vapor deposition (MOCVD), laser-ablation CVD, *etc.* Basically, all these methods are governed by two typical categories: the vapor–liquid–solid (VLS) mechanism and the vapor–solid (VS) mechanism.[54–60] For a typical VLS process, which was first proposed for the growth of silicon whiskers, metal nanoparticles are used as the catalysts to direct the nanowire growth. Such a process involves the formation of catalyst droplets at a high temperature, the adsorption and dissolution of gaseous precursors, and the precipitation of solid nanowires after saturation. Clear evidence for the VLS process is the existence of metal nanoparticles attached to the tips of the formed nanowires. During this process, the diameters of the final nanowires can be easily controlled by the size of the catalyst nanoparticles. Fig. 1a shows an SEM image of ZnO nanowires synthesized from a VLS process by using gold nanoparticles as the catalysts. Typical ZnO nanowires have diameters of around 100 nm and lengths of up to several hundred microns. Another example for the VLS process is the production of SnO_2 nanobelts, which have diameters of 100–300 nm and lengths of tens of microns, as shown in Fig. 1c. In fact, the VLS process is a very powerful method for synthesizing many metal oxide nanowires, such as binary metal oxides

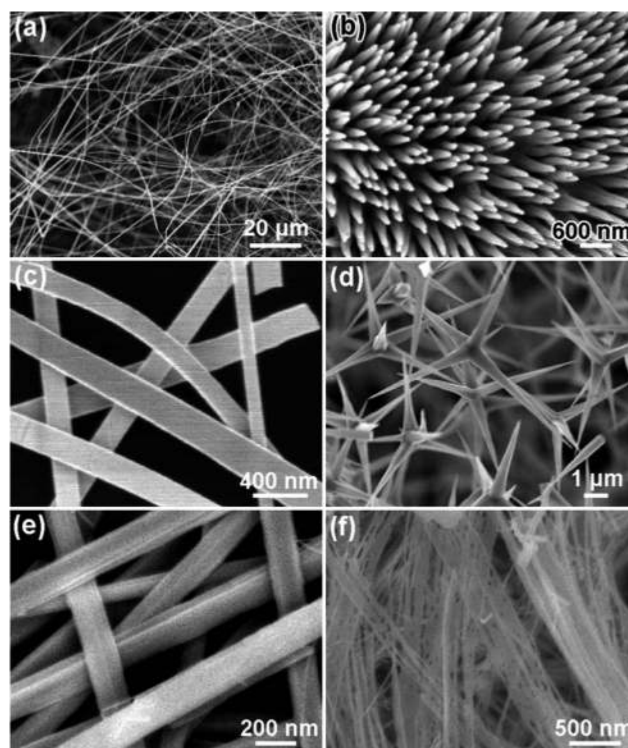

Fig. 1 1-D nanostructures synthesized from (a–d) vapour phase method and (e and f) solution-based method. (a) In_2O_3 nanowires; (b) ZnO nanowires; (c) SnO_2 nanobelts; (d) ZnO tetrapods; (e) InOOH nanobelts; and (f) porous In_2O_3 nanobelts.

Table 1 Advantages and disadvantages of different semiconducting materials for TFT applications[a]

Materials	Advantages	Disadvantages
α-Si	Excellent stability Used in LCDs	High processing T Low μ ($\sim$1 cm^2 V^{-1} s^{-1})
Poly-Si	High μ (150 cm^2 V^{-1} s^{-1}) Used in AMOLEDs	High processing T Not transparent
Organic	Low processing T Flexible and transparent	Low μ ($\sim$1 cm^2 V^{-1} s^{-1}) Sensitive to T/moisture
Metal oxide NWs	High μ (>500 cm^2 V^{-1} s^{-1}) Low processing T Flexible and transparent	Uniformity (shape and properties) Assembly and yield

[a] μ-mobility; T-temperature.

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ZnO, SnO_2, In_2O_3, Ga_2O_3, and ternary metal oxides $ZnGa_2O_4$, Zn_2GeO_4, $In_2Ge_2O_7$, *etc.*[73–87]

In contrast to the VLS process, the VS process does not require any metal catalysts to promote the nanowire growth. The growth of the nanowires *via* the VS process is mainly governed by the crystallographic nature of the nanowire material. In such a process, nanowires usually grow along the direction in which the crystal plane has the lowest energy. Fig. 1b is an SEM image of the ZnO nanowire arrays grown on a silicon substrate by the thermal evaporation of zinc powders at 550 °C. The as-grown nanowires have an average diameter of about 150 nm and lengths of several microns. These nanowires have uniform growth directions along the (0001) planes of the hexagonal ZnO phase. It is well known that the (0001) crystal plane of ZnO is the most densely-packed plane with the lowest energy, so the nanowires tend to grow along these planes. The shapes of metal oxide nanostructures produced *via* the VS process can also be finely tuned by varying the reaction parameters, such as temperature, source material, pressure, *etc.* Fig. 1d is an SEM image of the ZnO tetrapods produced by thermal evaporation of Zn powders at 850 °C.

2.2 Solution phase methods

Thermal evaporation methods tend to produce high quality single crystalline metal oxide nanowires with excellent crystallinity. However, the yield of nanowires is usually not very high and the high reaction temperature prevents it, in some cases, from being widely used for large scale applications. In contrast, solution-based methods have the advantages of high nanowire yield, low cost and easy fabrication. Among solution methods, the hydro/solvothermal methods are the most frequently used ones. For example, Fig. 1e shows an SEM image of InOOH nanobelts produced in a hydrothermal process. Typical InOOH nanobelts have diameters of 10–200 nm, and lengths of several tens to hundred microns with a very small thickness.[82] By annealing the InOOH nanobelts in air at a high temperature, they were easily converted to single-crystalline porous In_2O_3 nanowires, which can be used as high performance chemical sensors with improved sensitivities. By using solution-based methods, many metal oxide nanowires, including ZnO, SnO_2, In_2O_3, VO_2, Fe_2O_3, Cu_2O, *etc.* are easily synthesized with very high yields. Compared with the vapor phase methods, the main drawback of the solution-based methods is that the nanowires produced from solution methods always show low levels of crystallinity, which affects the performance of the subsequently fabricated transistors.

Besides the most popular hydro/solvothermal methods, solution methods assisted by hard or soft templates to confine the material growth are also widely used to get metal oxide nanowires. The most popular templates used include carbon nanotubes, porous membranes, surfactants, microemulsions and edges of surface steps or cracks, *etc.* A good example is the synthesis of porous In_2O_3 nanowires by using carbon nanotubes as the hard templates:[88] carbon nanotubes were first treated with polyelectrolytes and then immersed in $InCl_3$ and a citric acid solution, followed by dipping in $NaBH_4$ and calcination at a high temperature. The as-obtained porous nanowires were used as ammonia sensors, exhibiting improved performance at room temperature. Other solution-based methods include electrochemical deposition, sol–gel deposition and sonochemical methods. All of them are useful for synthesizing metal oxide nanowires.

3. Nanowire transfer and printing

Based on the quality of the nanowires produced *via* vapor phase methods and solution phase methods, it could be concluded that the nanowires synthesized from vapor phase methods are better candidates for the subsequent transparent transistor applications in terms of high device mobility, high electric on/off ratio, moderate carrier concentrations, low threshold voltages, and steep sub-threshold slopes. In the following sections, we will focus on metal oxide nanowires produced *via* the vapor phase methods.

To make transparent transistors, the metal oxide nanowires grown on the deposition substrate should be transferred to a secondary transparent substrate, usually glass or a transparent organic material, for eventual device fabrication. The most widely used method to date is the dip-coating method, which involves first the removal of the as-grown nanowires from the deposition substrate by means of ultrasonic sonication in organic solution, and then drop-by-drop coating of the detached nanowires to the transparent substrates. This method has been proved to be useful in making transparent transistors built on In_2O_3 nanowires and ZnO nanowires. However, the nanowires are heavily damaged during ultrasonic sonication in an organic solution, and the nanowires dipped on the transparent substrate are far from uniform. It is also hard to precisely control the nanowire density.

Recently, we developed a simple physical transfer method by directly peeling the as-grown In_2O_3 nanowire mats from the silicon substrate to a glass substrate.[104] The process starts with the growth of In_2O_3 nanowire mats *via* a laser-ablation assisted chemical vapor deposition method. After synthesis, we can directly peel the nanowire mats by using sharp tips, such as AFM tips or tweezers. Fig. 2a shows an SEM image of the interface between the nanowires before and after being peeled off. A high-magnification SEM image is shown in Fig. 2b, where it can be seen that almost all the nanowires are successfully peeled off the silicon substrate. By putting the peeled nanowire mats on a glass substrate, highly transparent thin-film transistors were then fabricated.

During this process, it is important to investigate why the nanowire mats can be directly peeled off the substate. Fig. 2c–e show the higher-magnification SEM and TEM images of the as-grown nanowires. From these images, we found that almost all of the as-grown nanowires are of interesting branched morphology instead of single nanowires. Numerous bipod, tripod and tetrapod junctions are formed within the nanowires, which results in the formation of a close-packed cross-linked structure. When peeling off a single nanowire, the others tend to be peeled off together. It should be noted that currently only nanowire mats with a small size (5 mm × 5 mm) can be peeled off, though this process is quite simple and efficient to make transparent transistors. With proper tuning of the synthetic process and transfer technique, we believe such a direct transfer method may

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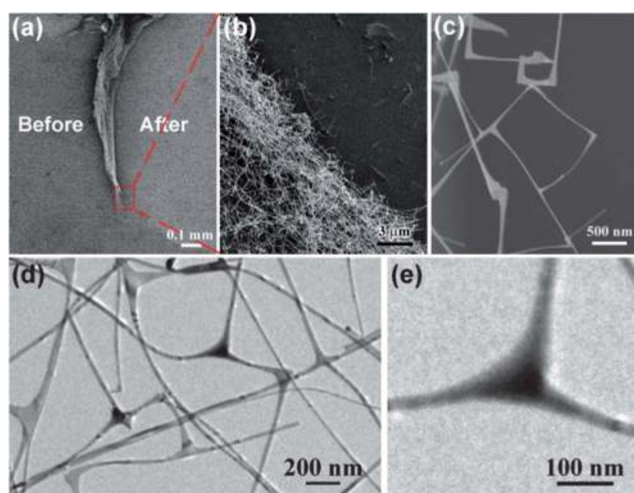

Fig. 2 Directly transferable In_2O_3 nanowire mats. (a and b) SEM images showing the interface between nanowires before and after transfer. (c) High-magnification SEM image and (d and e) TEM images revealing the formation of branched nanowires. Reprinted with permission from ref. 104. Copyright 2011 Wiley-VCH.

be extended to transfer other metal oxide nanowire mats to make highly reliable transparent transistors.

The controlled assembly of nanowires on substrates with high uniformity over large areas and with high alignment of these nanowires presents a major challenge. Over the past several years, many strategies have been developed, including flow-assisted alignment methods, electric-field directed deposition, the Langmuir–Blodgett assembly technique, and surface-programmed assembly, all of which involve the suspension of the nanowires in organic solvent by ultrasonic sonication followed by their transfer to the receiver substrate.[89–106] Although the above methods have been explored with varying degrees of success, they are not well adapted to the fabrication of high-density networks at larger scales.

Very recently, an efficient method that has received great attention is direct contact printing.[107–110] It is based on the direct transfer of nanowires from the growth substrate to the receiver substrate through shear force. Such a method has been proved to be one of the best demonstrated and simplest techniques for the scalable assembly of parallel nanowire arrays with high uniformity.

Fig. 3a shows a schematic demonstration of the typical contact printing of nanowires, starting from the donor substrate with randomly aligned nanowires grown on it, which was then used for the contact printing of the nanowires to the receiver substrate by directional sliding of the donor substrate, resulting in the formation of aligned nanowire arrays on the receiver substrate. During this process, the van der Waal's forces of attraction and some other chemical binding interactions between the donor substrate and the transferred nanowires allow the nanowires to attach well to the substrate. The density of the nanowires is determined by the as-grown nanowires and can be efficiently increased by repeated contact printing. Fig. 3b shows an SEM image of the contact printed SnO_2 nanowires, which were grown on a silicon substrate *via* a thermal evaporation method. Contact printing yields highly aligned nanowires with densities of about

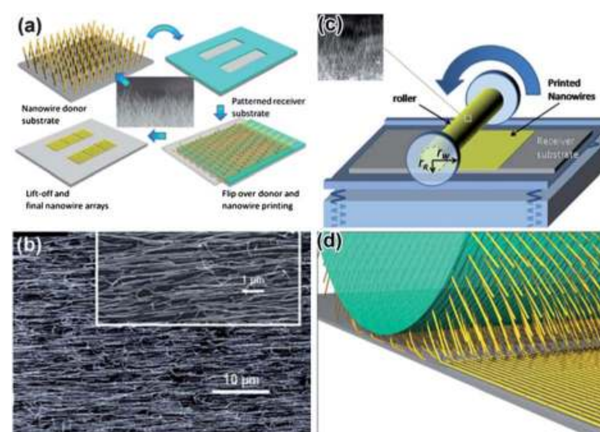

Fig. 3 Schematic illustration of nanowire contact printing involving (a and b) planar and (c and d) cylindrical growth substrates. Reprinted with permission from ref. 105 and 106. Copyright 2011 Wiley-VCH and 2011 American Chemical Society.

0.3 nanowires per μm^2. The good alignment of these nanowires indicates that the contact printing method is a powerful tool for the alignment of nanowires.

By growing nanowires on a cylindrical substrate instead of flat substrate, the contact printing method can be combined with the roll-to-roll printing method to be used as a highly scalable way to print aligned nanowires. Fig. 3c shows the printing process by using nanowires grown on a cylindrical quartz rod as the printing source. Rolling the quartz rod with some force along a unique direction resulted in the printing of aligned nanowire arrays on the receiver substrate, as indicated in Fig. 3d. Although the current printing speed is far from what is desired for manufacturing, this technique still shows great potential for printable nanowire electronics.

4. Transparent nanowire transistors

Metal oxide nanowires have several advantages *versus* other materials used for transparent transistor applications, such as good optical transparency, high mobility, and excellent mechanical flexibility. In addition, the electronic properties of metal oxide nanowires can be tuned by controlled doping or forming heterostructures during the nanowire growth process. High performance transparent transistors have been built on single nanowires and nanowire thin films.

Until now, the most widely used metal oxide nanowires for fabricating transistors are the three mentioned above (ZnO, SnO_2 and In_2O_3), due to their wide band gap, high transparency and high mobilities. ZnO is promising for optoelectronic devices due to its wide band gap of 3.37 eV at room temperature and its large exciton binding energy of 60 meV. In particular, ZnO is believed to be a material with the richest variety of morphologies among all metal oxides. Researchers can easily assemble ZnO into nanowires, nanorods, nanobelts, nanorings, nanosprings, nanoflowers and many other morphologies, which make it possible to make high performance electronic and optoelectronic devices even for some special applications, such as nanogenerators. However, ZnO is a typical n-type semiconductor and

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it is hard to get stable p-type ZnO by doping, which limits its further device applications.

In_2O_3 has a wide bang gap of 3.6 eV at room temperature. Compared with ZnO, In_2O_3 has limited morphologies. However, transistors made on In_2O_3 nanowires usually have higher mobilities than ZnO transistors. Recently, we found that transistors built on As-doped In_2O_3 nanowires by using an organic self-assembled nanodielectric (SAND) layer as the dielectric layer exhibited an improved mobility as high as 2560 $cm^2 V^{-1} s^{-1}$, which is the highest among all metal oxide nanowires. With high conductivity and excellent transparency, indium tin oxide is now widely used in a rapidly increasing number of OLEDs, electroluminescent displays and other products, which is likely to lead to a serious shortage of rare indium. People may have to consider exploring the use of other metal oxide nanowires to make transparent transistors.

SnO_2 is quite attractive for low-cost transparent electronics: it is an n-type semiconductor with a band gap of 3.6 eV. With high transparency, low growth cost compared with other metal oxides, and ease of forming Ohmic contacts, SnO_2 has been widely used to fabricate high performance transistors, gas sensors, li-ion batteries, *etc.*

In the following section, we will provide a detailed discussion of transparent transistors, both single nanowire transistors and TFTs built on the above three metal oxide nanowires.

4.1 Transparent single nanowire transistors

4.1.1 Nanowire transistors. Ju *et al.* fabricated transparent single nanowire transistors by using ZnO and In_2O_3 nanowires as the active channels because both materials are transparent and mechanically robust/flexible.[111] Fig. 4a shows the cross-sectional view of the fully transparent metal oxide nanowire transistors on a glass substrate, which includes nanowire channels, ITO source and drain electrodes, and an IZO gate electrode. Fig. 3b shows the I_{ds}–V_{gs} characteristics of a single ZnO nanowire transistor. From these curves, we can see that the ZnO nanowire device exhibited a threshold voltage of about 0.3 V dec^{-1} and an electric on/off ratio of 1×10^6 with mobilities in the range of 70–96 $cm^2 V^{-1} s^{-1}$ over the gate bias range of 0–3 V. Fig. 4c shows the drain current *versus* drain-source voltage (I_{ds}–V_{ds}) characteristics of the transparent ZnO nanowire transistor, which exhibits a typical enhancement mode long-channel FET behavior. The optical transmission spectra of the ZnO and In_2O_3 nanowire transistors are depicted in Fig. 4d. Both devices exhibited an optical transparency of around 90% in the visible light region, indicating the excellent transparency of these devices. The inset in Fig. 4d is a digital photograph of the real device, where the background figure can be easily seen through the device, confirming the excellent device transparency.

Using metal oxide nanowires, fully transparent and flexible transistors were also fabricated using a polyethylene terephthalate (PET) plastic substrate. Fig. 4e is the corresponding cross-sectional view of the fully transparent and flexible In_2O_3 nanowire transistors, which use all transparent components. Fig. 4f is a digital photograph of the corresponding device, exhibiting excellent transparency and flexibility. The devices have an electric on/off ratio of 1×10^5 with device mobilities of 120–167 $cm^2 V^{-1} s^{-1}$.

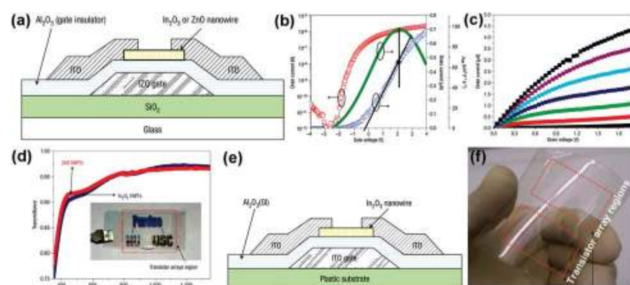

Fig. 4 (a) Cross-sectional view of a fully transparent metal nanowire transistor and its corresponding (b) I_{ds}–V_{gs} curve, (c) I_{ds}–V_{ds} curve and (d) optical transmission spectra. (e) Cross-sectional view of a fully transparent and flexible nanowire transistor and its corresponding digital image. Reprinted with permission from ref. 111. Copyright 2007 Nature Publishing Group.

4.1.2 Doped nanowire transistors. As we mentioned in the above section, the electronic properties of metal oxide nanowires can be easily tuned by choosing the correct dopant. Recently, Zhang *et al.* fabricated fully transparent and flexible transistors by using Zn-doped In_2O_3 nanowires as the active channels.[112] Fig. 5a shows the SEM image of the Zn-doped In_2O_3 nanowires *via* a VLS process, which have diameters of 80–100 nm and lengths of 20–50 μm. The corresponding device consists of an ITO-coated PET substrate, an SiN_x gate insulator and ITO source and drain electrodes. A digital photograph of the device is shown in Fig. 5b. The device shows over 90% optical transmittance in the visible light region and the image beneath the device is clearly visible through it.

Fig. 5c shows the corresponding I_{ds}–V_{ds} curves of the transparent Zn-doped In_2O_3 nanowire device, exhibiting typical n-type transistor characteristics. The threshold voltage was calculated to be around 0.07 V and the device mobilities are determined to be 631 $cm^2 V^{-1} s^{-1}$ in the linear operation region

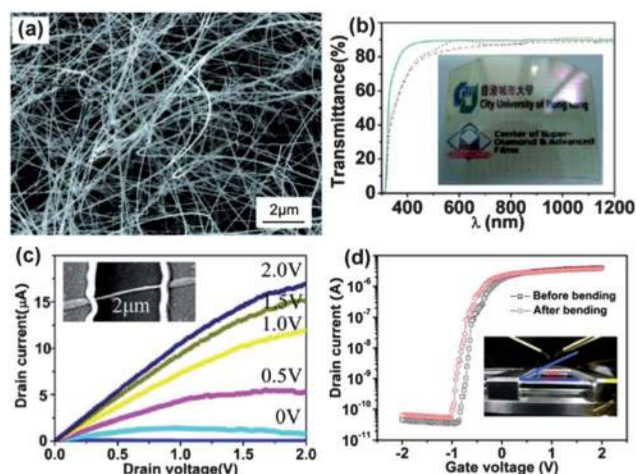

Fig. 5 (a) SEM image of CVD synthesized Zn-doped In_2O_3 nanowires. (b) Optical transmission spectrum of the transparent and flexible nanowire devices. (c) Typical I_{ds}–V_{ds} curves of the device. (d) Transistor characteristics of the device before and after bending. Reprinted with permission from ref. 112. Copyright 2009 American Institute of Physics.

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using the equation $\mu_e = g_m L^2/CV_{ds}$. The flexibility of the device was investigated by measuring the I_{ds}–V_{gs} curves under different degrees of bending. Fig. 5d shows the corresponding I_{ds}–V_{ds} curves of the device before and after being bent to an angle of about 30°. No obvious performance degradation was observed from these curves, indicating the good mechanical flexibility of the nanowire transistors.

4.2 Transparent nanowire thin-film transistors

Besides the transparent single nanowire transistors, transparent nanowire thin-film transistors were also designed because they are very important for future scale-up circuits and device integrations.

4.2.1 Nanowire TFTs. Ultrathin one-dimensional nanostructures with diameters less than 10 nm have gained great attention in recent years since they have a significantly increased surface area, which is very important for their applications as high performance sensors, catalysts, electronic and optoelectronic devices.[113–120]

Recently, we successfully synthesized ultrathin In_2O_3 nanowires with diameters below 4 nm by using the laser-ablation CVD method.[121] Fig. 6a shows the SEM image of the synthesized ultrathin In_2O_3 nanowires, which existed as ultrathin branches of hierarchical In_2O_3 nanostructures. The inset TEM image clearly shows that the diameters of these ultrathin nanowires are below 4 nm. Using these ultrathin In_2O_3 nanowires as active channels, we fabricated transparent TFTs consisting the nanowires, a glass substrate, an ITO gate, source and drain electrodes, and an Al_2O_3 insulating layer, as shown in Fig. 6b. The background image is easily seen, demonstrating the excellent optical transparency. Fig. 6c and d depict the structure of the device, where hierarchical nanowires were found to be gated by two electrodes. Due to the hierarchical structures, the nanowires formed smooth nanowire thin-films, which make the device fabrication process simpler than for single nanowire devices and the device yield was found to be nearly as high as 100%.

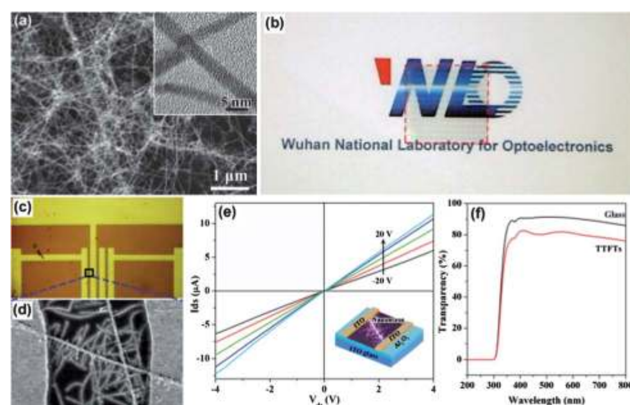

Fig. 6 (a) SEM image of ultrathin In_2O_3 nanowires synthesized from a laser-ablation CVD method. (b) Photograph, (c and d) device structures, (e) I_{ds}–V_{ds} curves and (f) transmittance spectra of the transparent In_2O_3 nanowire transistors. Reprinted with permission from ref. 121. Copyright 2011 American Chemical Society.

Fig. 6c shows the I_{ds}–V_{ds} curves of the transparent nanowire TFTs by sweeping the gate voltage from −20 to 20 V with a step of 10 V. We found that the transistor exhibited typical n-type transistor characteristics. The conductance is measured to be around 10.8 μS at $V_g = 0$ V and 5.9 μS at $V_g = 20$ V, which is 1–2 orders of magnitude higher than conventional single nanowire transistors. The greatly enhanced conductance makes such TFTs more suitable for high performance devices than single nanowire transistors. The transmittance of the transparent TFTs was also measured and the corresponding spectrum is shown in Fig. 6f. It can be seen that the as-fabricated transparent TFTs on the glass substrate show about 80% optical transmittance in the visible light range, indicating good transparency.

Transparent TFTs were also fabricated by using the directly transferable In_2O_3 nanowire mats as the active channels.[104] Fig. 7a is the SEM image of the as-obtained transferable In_2O_3 nanowire mats. Typical nanowires are of a single crystalline nature with diameters of 20–30 nm and lengths of the order of tens of microns. Fig. 7b shows the optical microscopy image of the fabricated transparent TFTs; between the ITO electrodes are the nanowire mats (Fig. 7c). One feature of the nanowire mats is that we do not need to use any alignment technique to predetermine the location of the ITO electrodes since the In_2O_3 nanowires form a smooth thin film on the substrate. A digital photograph of the final device is shown in Fig. 7d, revealing its excellent transparency. The transmittance was measured to be around 80% in the visible light range.

The structure of the transparent TFTs is shown in Fig. 7e and consists of a transparent ITO-coated glass substrate, an Al_2O_3 insulating layer, ITO source and drain electrodes, and between the electrodes are the nanowire mats. Fig. 7f and g are the measured I_{ds}–V_{ds} and I_{ds}–V_{gs} curves of the transparent device, showing typical n-type channel transistor characteristics. A threshold voltage of $V_T = 0.49$ V is derived from the curves with an on/off ratio of about 10^5. The small V_T, close to zero, is critical to minimize the power consumption for further applications. In addition, the device mobility, calculated from the linear region, is around 243 cm^2 V^{-1} s^{-1}, which is comparable to the In_2O_3 nanowire FET on a silicon substrate. The directly transferable In_2O_3 nanowire mat structure exhibited potential for scalable device fabrication and integration, though the transfer process efficiency is far from what is desired for manufacturing.

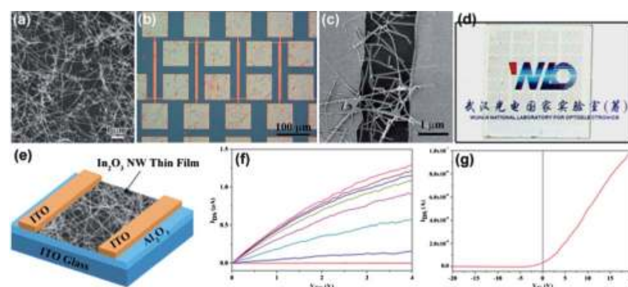

Fig. 7 (a) SEM image of the transferable In_2O_3 nanowire mats, (b–g) Characterizations of the transferable In_2O_3 nanowire mats based transparent TFTs. Reprinted with permission from ref. 104. Copyright 2011 Wiley-VCH.

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4.2.2 Doped nanowire TFTs. Nanowire thin-film transistors with doped metal oxide nanowires as the active channels were also fabricated in order to further improve the device performance. We recently synthesized arsenic doped indium oxide nanowires using a method similar to the above transferable In_2O_3 nanowire mats.[122] The growth of the As-doped In_2O_3 nanowires is governed by the VLS mechanism and the nanowires are single crystals with the growth direction along the (020) plane of hexagonal In_2O_3 phase. Fig. 8a is an SEM image of the corresponding nanowire structures, which have diameters of 15–30 nm and lengths of 5–10 μm. Using the dip coating method, transparent TFTs were successfully fabricated and the corresponding structure of the device is shown in Fig. 8b. An optical photograph of the device is shown in Fig. 8c, with the background image clearly visible through the transistor regions. The transmittance spectrum is about 81%, indicating excellent transparency.

The electronic transport properties of the As-doped In_2O_3 nanowires were derived by measuring single nanowire transparent TFTs, as shown in Fig. 8d and e. The As-doped In_2O_3 nanowire devices display an I_{on}/I_{off} of 5.7×10^6, a peak subthreshold slope (S) of 88 mV dec^{-1}, and threshold voltage (V_T) of 0.5 V. An important issue related to the As-doped In_2O_3 nanowires when compared with the pure In_2O_3 nanowires is that the mobility varies from 1080 to 1490 cm^2 V^{-1} s^{-1}. This value is much higher than that of pure In_2O_3 nanowires with the highest mobility being around 500 cm^2 V^{-1} s^{-1}. The incorporation of arsenic into the In_2O_3 nanowires efficiently increased the carrier concentration, thus increasing the mobilities.

4.2.3 Nanowire TFTs based on printed nanowires. Fig. 9 shows the application of the contact printing approach to SnO_2 nanowires to form transparent aligned SnO_2 nanowire TFTs.[123] Compared with other metal oxide nanowires, SnO_2 nanowires have high transparency, low growth cost and it is easy to obtain Ohmic contacts with conventional transparent conductive electrodes, which enable them to be excellent candidates for integration into high performance transparent TFTs. Fig. 9a shows the SEM image of gold catalysts synthesized SnO_2 nanowires deposited on a silicon substrate. The as-grown SnO_2 nanowires have a mean diameter of 55 nm with lengths of tens of microns. The image also reveals that the as-grown nanowires are randomly distributed across the whole substrate. Electronic transport characterizations revealed that the SnO_2 nanowires showed average mobilities of about 156 cm^2 V^{-1} s^{-1}, with the electron on/off ratio being larger than 10^5.

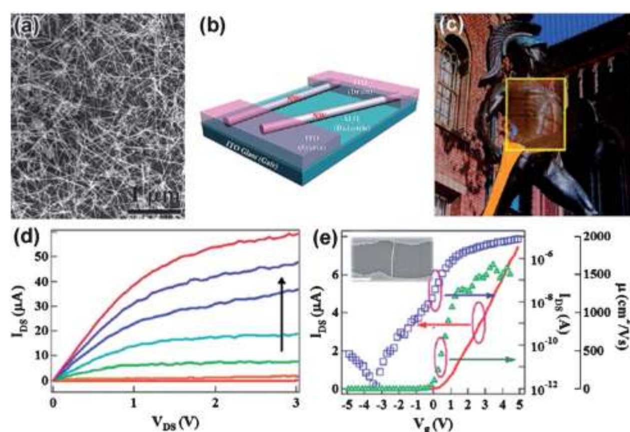

Fig. 8 (a) SEM image of As-doped indium oxide nanowires. (b) Schematic diagram of the As-doped In_2O_3 nanowire TTFTs on an ITO glass substrate. (c) Optical photograph of the fully transparent TFTs. (d) I_{ds}–V_{ds} and (e) I_{ds}–V_{gs} curves of the corresponding transparent TFTs. Reprinted with permission from ref. 122. Copyright 2011 American Chemical Society.

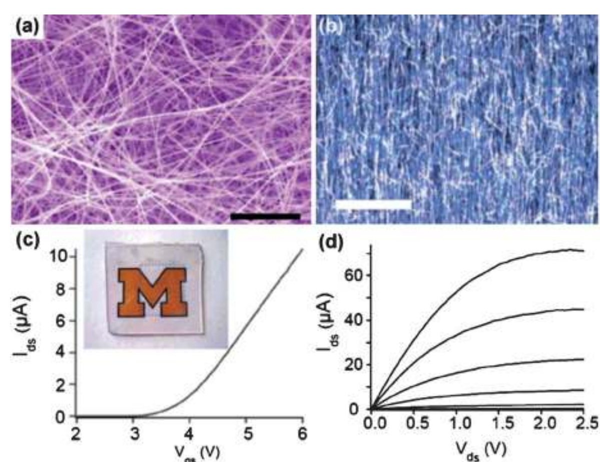

Fig. 9 (a) SEM image and (b) dark-field optical microscope image of the SnO_2 nanowire film before and after contact printing. (c) I_{ds}–V_{gs} and (d) I_{ds}–V_{ds} curves of the transparent TFTs with contact printed nanowires. Reprinted with permission from ref. 123. Copyright 2007 American Chemical Society.

By using the contact printing process, randomly distributed nanowires are forced into highly ordered aligned nanowire arrays, as revealed in Fig. 9b. Following the contact printing process, conventional sputter, photolithography and liftoff processes were used to pattern the transparent TFTs structure. The inset in Fig. 9c is an optical photograph of the fabricated devices, indicating very good transparency with a transmittance of ~70%, including the pyrex glass substrate. The corresponding I_{ds}–V_{gs} and I_{ds}–V_{ds} curves were demonstrated in Fig. 9c and d. The devices display enhancement-mode n-type transistor behavior, with clear linear and saturation regions. A large on current of 71 μA, a transconductance of 49 μS, and an on/off ratio of 10^3 can be obtained within a small V_{dd} bias window of 2.5 V. Contact printing of highly aligned nanowires for transparent TFTs leads to large scale applications of transparent nanowire electronics on diverse substrates.

5. Applications of transparent nanowire transistors

The ability to fabricate high performance transparent metal oxide TFTs has enabled further exploration of transparent circuit applications, which is essential for next-generation visual technologies and portable electronics.[124,125] In the following section, we demonstrated several applications of transparent metal oxide transistors as circuits to control OLEDs as well as transparent AMOLED displays.

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5.1 Fully transparent OLED driving circuitry

The inset of Fig. 10a shows the circuit diagram of an OLED driven by a transparent As-doped In_2O_3 nanowire transistor, where one transparent TFT is connected to an external OLED, and V_{dd} is applied to the drain of the transistor. By controlling V_{in}, the voltage drop across the OLED can be controlled. During this process, V_{in} provides a gate voltage for the transistor with fixed V_{dd}. Fig. 10a shows the current that flows through the OLED, which is modulated *via* V_{in} by a factor of $\sim$300. It can efficiently control the OLED light intensity, as can be seen in Fig. 10b. Fig. 10c shows the corresponding optical images of the OLED under fixed V_{in} with values of -3, 0, 3 V. From the above results, an off-state/on-state light intensity ratio of about 5 was obtained using the transparent nanowire TFT circuit. The performance is believed to be able to be further improved with optimized experimental sets.

5.2 Transparent AMOLED display circuitry

Besides the simple OLED driving circuitry mentioned above , transparent metal oxide nanowire transistors have also been used as circuitry for relatively complicated transparent AMOLED displays. Fig. 11 is a representative example of the transparent As-doped In_2O_3 nanowire transistors circuitry. Fig. 11a is the equivalent circuit diagram of the seven-segment AMOLED display circuitry. Among these structures, each OLED pixel consists of one switching nanowire transistor, one driving nanowire transistor, and one storage capacitor. Fig. 11b shows an optical image of an AMOLED display substrate before OLED deposition, with a size of 1 in × 1 in. The background picture is clearly seen through the display region, indicating the excellent transparency of the device. The optical transmittance spectra of the device before and after OLED layer deposition were also measured and the corresponding values are 81% and 35%, respectively in the visible region. Though the value after OLED layer deposition is not high enough for fully transparent display applications, the value should be readily increased by using optimized device design including both the driving transistor circuits and the OLED design. By fine tuning the driving transistors, the displays can efficiently show different numerical digits at different data line voltages with different scan line voltages and fixed V_{dd} values. For example, Fig. 11c displays numbers 1, 3, and 6, respectively. It should be mentioned that the number looks non-uniform, which is believed to be caused by the fact that the driving metal oxide nanowire transistors were fabricated by initially dip coating the nanowires onto a glass substrate, which usually results in uncontrolled nanowire densities. We believe that the performance should be largely improved if the contact printing method is used to pattern aligned nanowires on the glass substrate.

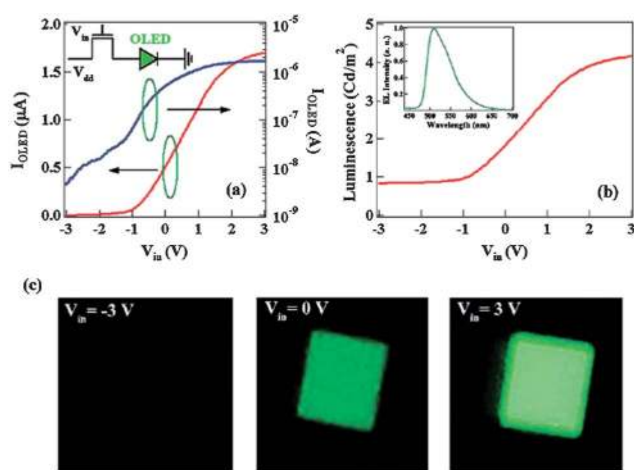

Fig. 10 Application of the transparent As-doped In_2O_3 nanowire transistors as OLED driving circuitry. Reprinted with permission from ref. 122. Copyright 2009 American Chemical Society.

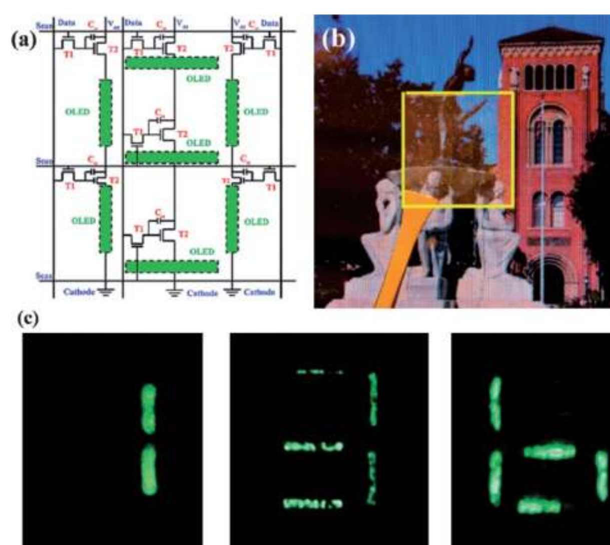

Fig. 11 Application of the transparent As-doped In_2O_3 nanowire transistors circuitry to drive a seven-segment AMOLED display. Reprinted with permission from ref. 122. Copyright 2009 American Chemical Society.

Ju *et al.* designed more complicated AMOLED displays driven by metal oxide nanowire electronics.[126] Fig. 12a shows the top and cross-sectional views of the transparent nanowire transistors and a pixel electrode for a single pixel. Each pixel contains at least one switching transistor, one driving transistor, and a storage capacitor with appropriate scan and data lines, aiming to selectively address the pixel. The SEM image depicted in Fig. 12b gives a clearer view of the nanowire transistor electronics design. The pixel electrode, driving transistor, switching transistor and capacitor can be easily seen in the image. It was found that the efficiency of the nanowire transistor driven AMOLED display is about 11 cd A^{-1} and the luminance is about 1630 cd m^{-2} within the active pixel area. The values correspond to an average luminance of about 300 cd m^{-2} for the overall device. Fig. 12c shows the optical images of the displays at various values of the data line voltages, corresponding to three brightness levels.

Ju *et al.* also designed transparent AMOLED displays driven by metal oxide nanowire electronics by using a very thin Al cathode. Fig. 12d shows the optical image of the fully transparent nanowire-AMOLED substrate. The good transparency can be derived from the fact that the background image can be seen through the display regions. The transmittance before and after the OLED deposition was measured to be around 72% and 35%,

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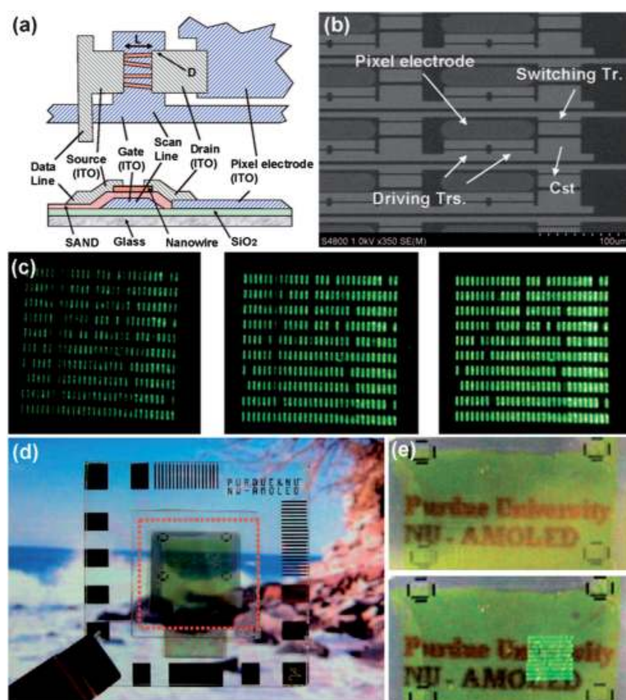

Fig. 12 Demonstration of transparent AMOLED displays using transparent metal oxide nanowire transistors circuitry. (a) Top and cross-sectional views of the driving nanowire transistors. (b) SEM image of several 54 × 176 μm pixels within 2 × 2 mm nanowire transistor arrays. (c) Optical microscopy image of a 2 × 2 mm AMOLED display under different bias conditions. (d) Optical image of a fully transparent nanowire-AMOLED substrate containing three 2 × 2 mm AMOLED pixel arrays. (e) Optical images of a region containing a 2 × 2 mm array. Reprinted with permission from ref. 126. Copyright 2007 American Chemical Society.

respectively, without correction for the transmission coefficient of the glass substrate. Fig. 12e shows the optical images of a 2 × 2 mm transparent metal oxide nanowire AMOLED array in the off-state and on-state, respectively.

6. Conclusions and outlook

Metal oxide nanowires are excellent candidates for transparent thin-film transistors with high mobility, a high electric on/off ratio and excellent transparency. In this paper, we provide a state-of-the-art review of the current achievements regarding the studies of metal oxide nanowires as high performance transparent transistors and their fascinating applications for next-generation transparent displays.

Metal oxide nanowires have been extensively studied for more than ten years. While encouraging progress has been achieved in this field, the use of metal oxide nanowires as the active channel materials to make transparent transistors has attracted researchers' attention only in very recent years. There is still much room for exploration, and we believe that the following directions should be further exploited.

First, the fabrication of transparent transistors starts from the synthesis of high quality single crystalline metal oxide nanowires. Though metal oxide nanowires produced from vapor phase methods have been proven to be excellent candidates for transparent transistor applications, the yield of nanowires is still far from that required for scalable device fabrication and integration. We believe that developing an efficient vapor phase methodology to improve the yield of nanowires is the most fundamental issue facing transparent electronics applications. Besides, control of nanowire uniformity, not only in its shape but also its electronic transport properties, is another critical issue for further device applications. Researchers have made great efforts to control the shape, size, and composition of metal oxide nanowires. However, nanowires with excellent shapes do not guarentee their uniformity in chemical or physical properties, especially the electronic transport properties, which is one of the most important properties for their application in fabricating transparent transistors with uniform performance.

One efficient way to improve the electronic transport properties is to synthesize doped metal oxide nanowires by choosing proper dopants. Another way to improve the electronic transport properties is to form heterostructured nanowires. Unfortunately, such a topic is seldom explored. There are mainly three types of heterostructured nanowires; core–shell, segmented and hierarchical heterostructured nanowires. Such a group of nanostructures could provide a new and wide playground for both fundamental properties studies and device applications.

Second, large scale printing and assembly of metal oxide nanowires are essential to further broaden their spectrum of applications. The contact printing method utilizes shear force to effectively align the nanowires. The process is very attractive because it is performed at ambient temperatures and is compatible with a wide range of substrates, including paper and plastic. Much work should be continued to be done on directly printing metal oxide nanowires on transparent substrates. Other issues for the contact printing of metal oxide nanowires include printing nanowires with controlled density, printing nanowires with specific patterns, printing nanowire superstructures, and achieving continuous printing. All these issues are key factors for further scalable device fabrication and integration.

Third, to make transparent metal oxide nanowire transistors, the lithography-based micro-fabrication process is the most commonly used one, which is complicated, time-consuming and uneconomical. Developing practical, low cost routes is thus needed to progress the transparent electronics field. One efficient way to achieve this is to integrate device printing with nanowire printing. For example, aligned nanowire arrays were first printed, and following this process the device fabrication proceeds by printing the source/drain, and gate electrodes.

Forth, though metal oxide transparent transistors have been developed to act as the driving circuits for transparent displays. The total transparency of the final displays is still not quite high enough after depositing the OLED layer. An efficient way should be found to ensure both high performance and good transparency, and to this end new device structures must be designed. Currently, all reported displays are still far from uniform, as can be found in the above discussions, largely due to the non-uniformity of the nanowires. We believe that this obstacle could be overcome by fine-tuning the electric transport properties and controlling the printing alignment of the metal nanowires.

Last, besides the application of transparent metal oxide nanowire transistors for transparent displays, it is important to

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explore other possible applications. For example, developing self-powered transparent chemical sensors and photodetectors by integrating the transistors with the sensing components using the contact printing process. Since transparent transistors are usually built on transparent polymer substrates, such as PET, we should pay more attention to the working conditions when the transistors are used as chemical sensors. Developing room temperature chemical sensors is thus highly desired.

With the rapid development of nanotechnology and increasing attention from industry, it is expected that commercial applications of transparent metal nanowire transistors will be realized soon.

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